Intel® Atom™ Processor D2000 and N2000 Series

Datasheet – Volume 2 of 2

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Revision History

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001	• Initial Release	September 2011
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1 Processor Configuration Registers

This is Volume 2 of the *Intel® Atom™ Processor D2000 series and N2000 Series External Design Specification (EDS)*, and is intended to be distributed as part of the complete document. This document provides register information for the processor.

1.1 Related Documents

Document Title	Document Number / Location[1]
Intel® Atom™ Processor D2000 series and N2000 series External Datasheet – Volume 1 of 2	326136
Intel® Atom™ Processor D2000 Series and N2000 Series Specification Update	326140

1.2 Register Terminology

The following table shows the register-related terminology that is used in this document.

Item	Definition
RO	**Read Only bit(s).** Writes to these bits have no effect. These are static values only.
RO/P	**Read Only/Sticky bit(s).** Writes to these bits have no effect. These are status bits only. Bits are not returned to their default values by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
RS/WC	**Read Set/Write Clear bit(s).** The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect.
RW	**Read/Write bit(s).** These bits can be read and written by software. Hardware may only change the state of this bit by reset.
R/WC	Read/Write Clear bit(s). These bits can be read. Internal events may set this bit. A software write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.

Item	Definition
R/WC/L	Read/Write Clear/Lockable bit(s). These bits can be read. Internal events may set this bit. A software write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WC/P	Read/Write Clear/Sticky bit(s). These bits can be read. Internal events may set this bit. A software write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).
R/W/B	Read/Write/Blind bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit.
R/W/B/L	Read/Write/Blind/Lockable bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/K	Read/Write/Key bit(s). These bits can be read and written by software. Additionally this bit, when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).
R/W/L	Read/Write/Lockable bit(s). These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/L/P	Read/Write/Lockable/Sticky bit(s). These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only). Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).
R/W/L/K	Read/Write/Lockable/Key bit(s). These bits can be read and written by software. Additionally this bit is a Key bit that, when set, prohibits this bit field and/or some other specified bit fields from being writeable (bit fields become Read Only).
R/W/P	Read/Write/Sticky bit(s). These bits can be read and written by software. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the PCI Express spec).

Item	Definition
R/W/P/B	Read/Write/Sticky/Blind bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/W/SC	Read/Write/Self Clear bit(s). These bits can be read and written by software. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent software read could retrieve a ‘1’.
R/W/SC/L	Read/Write/Self Clear/Lockable bit(s). These bits can be read and written by software. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent software read could retrieve a ‘1’. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/SC/L/P	Read/Write/Self Clear/Lockable/Sticky bit(s). These bits can be read and written by software. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent software read could retrieve a ‘1’. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only). Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/W/SS/L/P	Read/Write/Self Set/Lockable/Sticky bit(s). These bits can be read and written by software. When the bit is ‘0’, hardware may clear the bit to ‘1’ based upon internal events, possibly sooner than any subsequent software read could retrieve a ‘0’. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only). Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/WO	Write Once bit(s). Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset. If there are multiple R/WO fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.
R/WO/P	Write Once/Sticky bit(s). Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset. If there are multiple R/WO fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
W	Write Only. These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.
R/W/1/0	Write Logic 1 Once bit(s). Once written to logic 1 by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset.

1.3 System Address Map

The Intel Atom Processor D2000 series and N2000 Series SoC supports 64GB (36 bit) of addressable memory space and 64 KB+3 of addressable I/O space. Addressing of greater than 4 GB is allowed on the DMI Interface as well as by the Intel Atom Processor D2000 series and N2000 Series GFX, Video, and Display units. The Intel Atom Processor D2000 series and N2000 Series SoC supports a maximum of 4GB of DRAM. There is no hardware lock to stop someone from inserting more memory than is addressable.

1.4 Intel Atom Processor D2000 series and N2000 Series Address Spaces

1.4.1 Physical Address Space

This is the full 64GB (36bit) range of memory address space used by the CPU and devices. This is the address space accessible by memory reads, writes, and is the set of addresses as presented to the GMCH or devices from either the CPU or devices.

This address spaces has three sub-types depending on the final destination of the request and the mapping registers within CDV:

- **Memory Mapped IO (MMIO) Ranges** – These are ranges in physical address space that accept loads/stores from the CPU and generally map those request to devices (registers or on-device memory) rather than system DRAM. These ranges must not be programmed to overlay each other. Request to these addresses ranges should only come from IA code (the CPU) and not from devices on Intel Atom Processor D2000 series and N2000 Series or from DMI.
- **DRAM Ranges –** These are ranges in physical address space that accept loads/stores from the CPU or Devices (both on Intel Atom Processor D2000 series and N2000 Series and from DMI) that map to System DRAM.
- **Bad Memory Ranges –** These are ranges in physical address space that the BIOS must tag as unusable by the OS. This may be due to a lack of hardware support for the range or it may be that the range has been “stolen” for hardware private use.

Intel Atom Processor D2000 series and N2000 Series memory protection/security and coherency checking is performed in Physical Address Space. This includes IMRs, HMBOUND, HMBOUNDHI and ME UMA protection.

1.4.2 System DRAM Address Space

This is the range of addresses presented to the memory controller after all security checks and reclaiming has been done. The memory controller is aware of the total amount of populated DRAM and addresses above this range are considered invalid – writes will be dropped and reads will return all 1’s.

In truth, memory controllers including Intel Atom Processor D2000 series and N2000 Series have options to swizzle which System DRAM Address Space address bits map to banks, rows, columns to increase performance. For purposes of this discussion, this mapping is assumed to 1 to 1.

System DRAM Stolen Memory Ranges – These are portions of physical System DRAM held in reserved by Intel Atom Processor D2000 series and N2000 Series for internal purposes. The BIOS is responsible for not exposing these areas of DRAM to the Operating System and ensuring that stolen memory ranges don't overlap.

1.4.3 IO Space

These are IO address ranges presented to the CPU. These are "IO" ranges in that they have a dedicated addressing space of 64KB+3 only accessible by the CPU using IN/OUT instructions. There is no relationship to memory space or PCI config space. These ranges must not be programmed to overlap each other. These requests never map to system DRAM and are not part of this discussion.

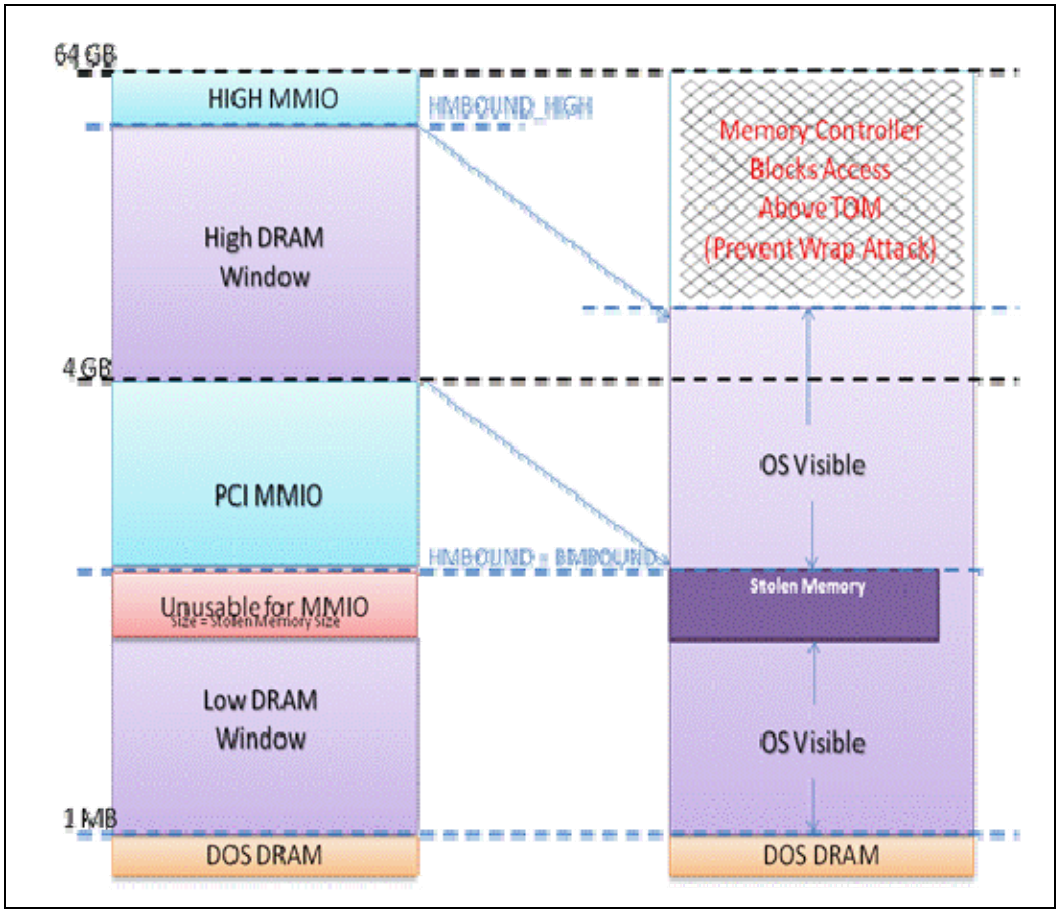
1.4.4 PCI Config Space

PCI Config space is used to access many device register on and off CDV. This space is only accessible from the CPU. Intel Atom Processor D2000 series and N2000 Series converts special IN/OUT instructions from the CPU (or an optional MMIO Range) into PCI Config Space. Other than mentioning the MMIO range used for this, PCI Config Space is not part of this discussion.

1.5 Physical to DRAM Address Space Mapping

Memory Mapping is defined has how Intel Atom Processor D2000 series and N2000 Series translates from Physical Address Space (as seen by the CPU and devices) to DRAM Address Space (as seen by the memory controller).

Figure 1-1. Physical to DRAM Address Map



1.5.1 Intel Atom Processor D2000 series and N2000 Series Memory Mapping Registers

Intel Atom Processor D2000 series and N2000 Series uses only two main registers to control this mapping: HMBOUND and HMBOUNDHI:

Table 1-1 Intel Atom Processor D2000 series and N2000 Series Memory Mapping Registers

TBD

1.5.1.1 HMBOUND

This register sets a Physical Address Space location between 0 - 4GB. With few exceptions, request >= HMBOUND (but < 4GB) map to the device/DMI side if from the CPU and are rejected if from devices. Request < HMBOUND map to the memory controller with a 1:1 mapping from Physical Address Space to DRAM Address Space.

HMBOUND has a granularity of 256MB. It only matches the upper address bits and anything that matches or is greater will go to MMIO space. Since HMBOUND compares address bits [31:27], the highest physical it can be set is 0xF800_0000h. Therefore, all address in 0xF8000_0000h <= address < 0xFFFF_FFFFh always map to PCI MMIO.

The DOS Legacy portion of Physical Address space is below HMBOUND, but has a few ranges than can be programmed to map to devices/DMI instead of System DRAM. These are covered later in this section.

Because systems generally need a 1-2 GBytes of Physical Address Space for MMIO, HMBOUND was typically set to a value such as 3GB (3GB available to the OS for DRAM, 1GB of address space available for MMIO). In order to avoid wasting any DRAM above 3GB, all Physical Addresses > 4GB are offset down such that the 4GB Physical Address Space address maps to the HMBOUND address in DRAM Address Space (4GB would map to 3GB in this example). This prevents wasting any DRAM.

1.5.1.2 HMBOUNDHI

This register sets a Physical Address Space location between 4GB and 64GB.

Request < HMBOUNDHI (but >= 4GB) map to the memory controller but with a negative offset mapping from Physical Address Space to DRAM Address Space. This negative offset reclaims the portion of DRAM behind the PCI MMIO Range that would otherwise be unusable.

Request >= HMBOUNDHI from the CPU may to the device/DMI side for access to MMIO for 64bit devices. Request above HMBOUNDHI from devices attempt to map to the memory controller, but are rejected if above the amount of programmed DRAM.

HMBOUNDHI has a granularity of 4GB. This will often cause a HMBOUNDHI to be set higher than desired and a range of memory just below HMBOUNDHI will need to be set to “BAD” by the BIOS since it is unusable. See the programming examples.

1.6 Intel Atom Processor D2000 series and N2000 Series Memory Map Register Programming Examples

1.6.1 Case 1: 2GB DRAM. Min 1 GB PCI MMIO

HMBOUND needs to be <= 3GB to make room for 1GB of PCI MMIO between HMBOUND and 4GB.

HMBOUND could be set to 3GB, but any Physical Address Space request from 2GB – 3GB will exceed available DRAM and this range will need to be marked as unavailable by the BIOS to the OS (“bad”). Instead, it’s better to leave this 2GB – 3GB Physical Address Space range available for MMIO devices. Setting HMBOUND to 2GB makes all 2 GB of DRAM available and gives 2 GB of PCI MMIO space.

Since available DRAM is < 4GB, HMBOUNDHI should be set to 4GB, allowing all of the 4GB – 64GB address space to be used for 64bit PCI MMIO.

1.7 Internal Device Memory Ranges

The Intel Atom Processor D2000 series and N2000 Series Address Map includes a number of programmable ranges for both Device 0 (Host) and Device 2 (GFX/Video/Display). The three main ranges discussed here are MMIO, Stolen DRAM, and IO Space. All are described in section **Intel Atom Processor D2000 series and N2000 Series Address Spaces.**

The rules for programming these ranges are:

- ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designers' responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
  - Accesses to overlapped ranges may produce indeterminate results.
  - In the case of overlapping ranges with memory, the memory decode will be given priority. This is a Intel® Trusted Execution Technology (Intel® TXT) requirement. It is necessary to get Intel TxT protection checks, avoiding potential attacks. Note that although the behavior conforms to Intel TxT requirement, the Intel TxT technology is NOT SUPPORTED in Intel Atom Processor D2000 series and N2000 Series .
  - There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
- Intel Atom Processor D2000 series and N2000 Series does not support peer-decode. It is not possible to have a DMI upstream request (or a request from a Intel Atom Processor D2000 series and N2000 Series internal device), target anything other than system memory. Intel Atom Processor D2000 series and N2000 Series does not decode memory or I/O accesses and re-direct them. For example, a PORT write from DMI to cause an INIT does not work. The only exception to this is the Intel Atom Processor D2000 series and N2000 Series PMU will fetch its initialization code from DMI during cold boot or return from S3.
- Memory reads/writes or I/O PORT IN/OUTs that are not captured by Intel Atom Processor D2000 series and N2000 Series are sent to the ICH via the DMI interface. If the ICH doesn't support the operation, it can either a) drop writes and return 1's for reads or b) return an UNSUPPORTED_REQUEST (UR) response. If the ICH supports that type of operation (always true for memory reads/writes) and the operation targets a location not captured/supported by the ICH, the ICH can either a) drop writes and return 1's for reads or b) return an ABORT response.
- If Intel Atom Processor D2000 series and N2000 Series receives an ABORT response on DMI, it must still complete the operation back to the CPU, returning all 1's for reads, to avoid a hang.
- For all Memory Mapped IO, the memory type must be uncacheable (UC or WC). Intel Atom Processor D2000 series and N2000 Series does NOT allow any accesses from the CPU to DMI to be cacheable. Implicit Writebacks for example may hang the system.
- For each MMIO or IO location, there may be separate behavior for reads and writes. For example, see the Section 1.6.3.4 PAM region descriptions.

CDV does not support the PHOLD feature. It is not possible to lock that pathway from the CPU all the way to a device connected to the ICH.

1.7.1 Device 0 (0/0/0) Memory Map

These are the MMIO, Stolen, and IO ranges reserved by CDV's internal PCI Device 0 (0/0/0 = Bus:0, Device: 0, Function: 0).

Table 1-2. Intel Atom Processor D2000 series and N2000 Series Device 0 Memory Map

Register	Type	Size	Base	64bit (OK in High MMIO)	Description
HMISC2	Fix Mem	64KB	Fixed: 0xF0_0000	N	PAM_F. System BIOS (Upper) Fixed: 0xF0_0000 – 0xFF_FFFF
HMISC2	Fix Mem	64KB	Fixed: 0xE0_0000	N	PAM_E. Extended System BIOS (Lower) Fixed: 0xE0_0000 – 0xEF_FFFF
PinStraps (TBD)	Mem	28KB	00 – 0xFFFE_0000 (default) 01 – 0xFFFD_0000 10 – 0xFFFC_0000 11 – 0xFFFB_0000	N	Intel Atom Processor D2000 series and N2000 Series PMU Firmware location in NAND (fetched from DMI)
AEC/HEC (PCIEXBAR)	MMIO	256MB	Between HMBOUND and 4GB	N	Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and Extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (256MB).
None. Stored internally after being provided by BIOS.	Stolen	28KB	Anywhere below HMBOUND. Set via IOSF-SB message to "Power Management Control (PMU)"	N	Intel Atom Processor D2000 series and N2000 Series PMU Firmware location in System DRAM
HSMMCTL	Stolen CPU SMM addressable	Programmable in HSMMCTL	Anywhere below HMBOUND	N	System Management Memory (SMM). 1MB aligned. Register is lockable.
PMBA	IO range	16	Private IO range. Not expressed in 0:0:0 PCI Cfg Bases	N/A	Power Management This corresponds to the P_BLK and should be programmed to match the

Register	Type	Size	Base	64bit (OK in High MMIO)	Description
					same locations in the ICH.
-	Fixed IO	8B		N/A	ONLY DWORD Accesses are captured. CF8 = CONFIG_ADDRESS CFCh = CONFIG_DATA

Intel Atom Processor D2000 series and N2000 Series does **not** have these ranges found on Intel® Atom TM Processor D500 and D400 Series.

- PXPEPBAR – Used on PNV for setting up VC1 as isoch.
- MCHBAR – For internal MCH registers such as DRAM controller.
- DMIBAR – Configuration of DMI.

1.7.2 Device 2 (0/2/0) Memory Map

These are the MMIO, Stolen, and IO ranges reserved by CDV's internal PCI Device 2 (0/2/0 = Bus:0, Device: 2, Function: 0). This includes support for GFX, Video Decode, and Display.

Table 1-3 Intel Atom Processor D2000 series and N2000 Series Device 2 Memory Map

Register	Type	Size	Base	64bit (OK in High MMIO)	Description
GVD.MMADR	MMIO BAR	1 MB	PCI: 0/2/10h	N	Access to Gfx, VED, Disp Registers
DISPLAY_CONTROLLER.MSR GVD.MGGC GVD.PCICMDSTS Other regs as well.	MMIO	128 KB	FIXED: 0xA_0000 – 0xB_FFFFh	N	Legacy Video. CPU Must map as UC.
GVD.PGTBL_CTL	Stolen	See GVD.GTTADR	GVD.MMADR+ 2020h	N	Pointer to GTLB Stolen Mem. Software access is via GVD.GTTADR in Section 1.11 MMIO Space
GVD.BSM	Stolen	1 MB	PCI: 0/2/5Ch	N	VGA Stolen Memory.
GVD.IO_BAR	IO BAR	8B	PCI: 0/2/14h	N/A	Indirect Register Access. **Note**: This allows accessing the same

Register	Type	Size	Base	64bit (OK in High MMIO)	Description
					registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.
DISPLAY_CONTROLLER.MSR GVD.PCICMDSTS Other regs as well.	IO	12B	FIXED: 3B0 – 3BBh	N/A	VGA. See GVD.MGGC
DISPLAY_CONTROLLER.MSR GVD.PCICMDSTS Other regs as well.	IO	32B	FIXED: 3C0 – 3DFh	N/A	VGA. See GVD.MGGC

All Device 2 MMIO ranges can reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of memory (TOLUD) and below 4GB so they do not steal any physical DRAM memory space.

1.7.2.1 Graphics Register Ranges

This section provides a high-level register map (register groupings per function) for the integrated graphics. The memory and I/O maps for the graphics registers are shown in Figure 5, except PCI Configuration registers, which are described in the following chapter. The VGA and Extended VGA registers can be accessed via standard VGA I/O locations as well as via memory-mapped locations. In addition, the memory map contains allocation ranges for various functions. The memory space address listed for each register is an offset from the base memory address programmed into the MMADR register (PCI configuration offset 10h). The same memory space can be accessed via dwords accesses to IOBAR. Through the IOBAR, IO registers MMIO_index and MMIO_data are written.

1.7.2.1.1 VGA and Extended VGA Control Registers (00000h–00FFFh)

These registers are located in both I/O space and memory space. The VGA and Extended VGA registers contain the following register sets: General Control/Status, Sequencer (SRxx), Graphics Controller (GRxx), Attribute Controller (ARxx), VGA Color Palette, and CRT Controller (CRxx) registers. Detailed bit descriptions are provided in the VGA and Extended VGA Register Chapter. The registers within a set are accessed using an indirect addressing mechanism as described at the beginning of each section. Note that some of the register description sections have additional operational information at the beginning of the section.

1.7.2.1.2 Instruction, Memory, and Interrupt Control Registers (01000h–02FFFh)

The Instruction and Interrupt Control registers are located in main memory space and contain the following types of registers:

1.7.2.1.3 Instruction Control Registers

Ring Buffer registers and page table control registers are located in this address range. Various instruction status, error, and operating registers are located in this group of registers. For debug purposes, an Instruction DMA FIFO port is provided.

1.7.2.2 IO mapped access to Device 2 MMIO space

If Device 2 is enabled, and Function 0 within device 2 is enabled, then IGD registers can be accessed using the IOBAR.

MMIO_Index: MMIO_INDEX is a 32-bit register. An IO write to this port loads the address of the MMIO register that needs to be accessed. IO Reads returns the current value of this register.

MMIO_Data: MMIO_DATA is a 32 bit register. An IO write to this port is redirected to the MMIO register pointed to by the MMIO-index register. An IO read to this port is redirected to the MMIO register pointed to by the MMIO-index register.

Note: GTT table space writes (GTTADR) are supported through this mapping mechanism.

1.7.2.3 Trusted Graphics Ranges

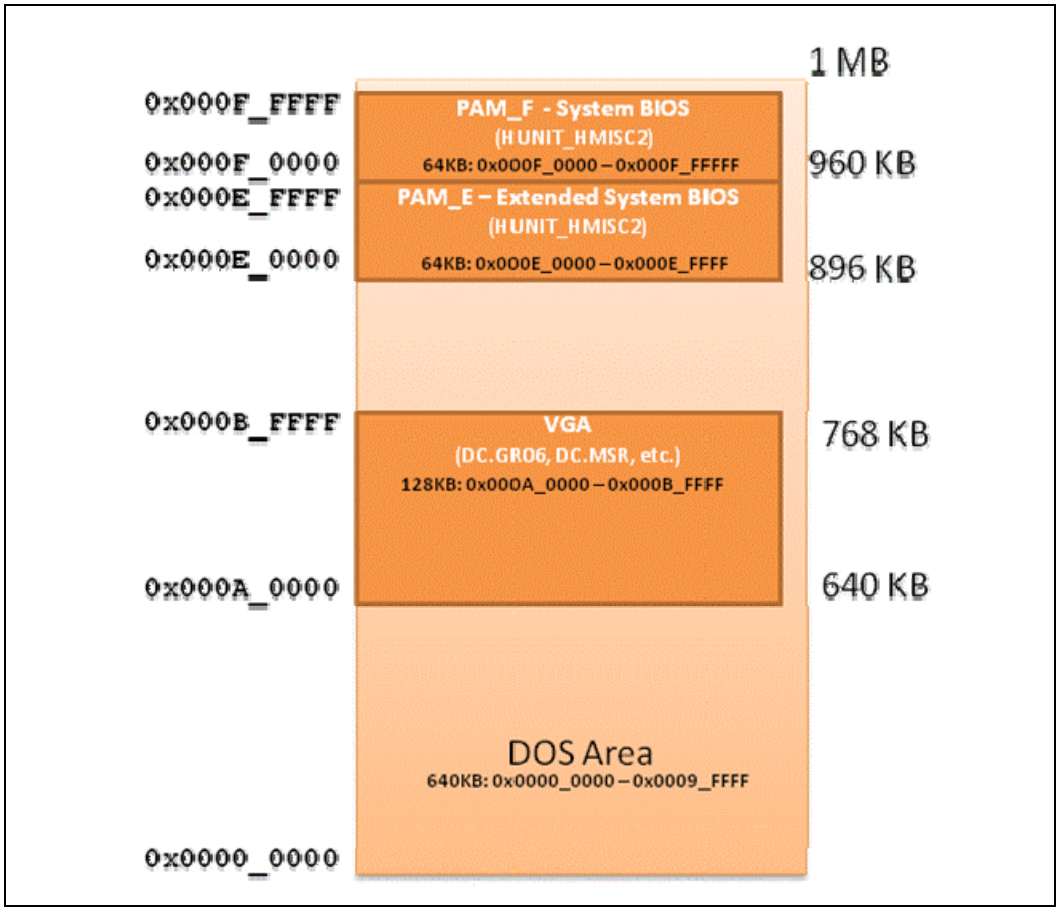
No trusted graphics ranges are supported on Intel Atom Processor D2000 series and N2000 Series .

1.7.3 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB DOS Area
- 640 – 768 KB Legacy Video Buffer Area
- 896 – 960 KB PAM_E – Extended System BIOS Area
- 960 – 1024 KB PAM_F – System BIOS Area

Figure 1-2. Legacy DOS Address Range



1.7.3.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the MCH.

1.7.3.2 Legacy Video Area (A_0000h-B_FFFFh)

The legacy 128KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD (Device #2) and/or to the DMI Interface. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The MCH always decodes internally mapped devices first. Internal to the MCH, decode precedence is always given to IGD. The MCH always positively decodes internally mapped device, namely the IGD. Subsequent decoding of regions mapped to the DMI Interface depends on the Legacy VGA configuration bits (VGA Enable).VGA range accesses are required to be QW in size or less. Cfg and VGA space must be UC.

Accesses to the VGA memory range are directed to IGD depend on the configuration. The configuration is specified by:

- Internal Graphics Controller in Device #2 function 0 is enabled (DEVEN0.D2F0EN=1)

- Internal Graphics VGA in Device #0 function 0 is enabled through register GGC bit 1.
- IGD's Memory accesses (PCICMD2 04 – 05h, MAE bit 1) in Device #2 are enabled.
- VGA Compatibility Memory accesses (VGA MSR Register, bit 1) are enabled.
- Software sets the proper value for VGA Memory Map Mode Register (VGA GR06 Register, bits 3-2). See the following table "IGC Frame Buffer Accesses" for translations.

Table 1-4. IGD Frame Buffer Accesses

Mem Access→ GR06(3:2)	A0000h – AFFFFh	B0000h - B7FFFh MDA	B8000h-BFFFFh
00	IGD	IGD	IGD
01	IGD	DMI Interface	DMI Interface
10	DMI Interface	IGD	DMI Interface
11	DMI Interface	DMI Interface	IGD

Note: Additional Qualification within IGD comprehends internal MDA support. The VGA and MDA enabling bits detailed below control segments not mapped to IGD.

- VGA I/O range is defined as addresses where A[15:0] are in the ranges 03B0h to 03BBh, and 03C0h to 03DFh. VGA I/O accesses are directed to IGD depends on the following configuration.
- Internal Graphics Controller in Device #2 function 0 is enabled through register DEVEN bit 4.
- Internal Graphics VGA in Device #0 function 0 is enabled through register GGC bit 1.
- IGD's I/O accesses (PCICMD2 04 – 05h, IOAE bit 0) in Device #2 are enabled.
- VGA I/O decode for IGD uses 16 address bits (15:0) there is no aliasing. Note that this is different when compared to a bridge device (Device #1) that used only 10 address bits (A 9:0) for VGA I/O decode.

Table 1-5. IGD VGA I/O Mapping

IO Access → MSRb0	3CX	3DX	3B0-3BB	3BC-3BF
0	IGD	DMI Interface	IGD	DMI Interface
1	IGD	IGD	DMI Interface	DMI Interface

NOTE: Additional Qualification within IGD comprehends internal MDA support. The VGA and MDA enabling bits detailed below control ranges not mapped to IGD.

For regions mapped outside of the IGD (or if IGD is disabled), the legacy VGA memory range A0000h-BFFFFh are mapped to the DMI Interface. The same register controls

mapping VGA I/O address ranges. VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded).

Summary of decode priority:

1. Internal Graphics VGA , if enabled, gets:
   03C0-03CF: always
   03B0-03BB: if MSR[0]=0 (MSR is I/O register 03C2)
   03D0-03DF: if MSR[0]=1

Note: 03BC-03BF never decodes to IGD; 3BC-3BE are parallel port I/Os, and 3BF is only used by true MDA devices, apparently.

2. Else, if ISA Enable=1, DMI gets: upper 768 bytes of each 1K block

1.7.3.2.1 Legacy VGA and Compatible Mode SMM

In the past, some system allowed SMM mode request to this area to go to DRAM while non-SMM CPU request go to integrated VGA (if enabled) or DMI. Intel Atom Processor D2000 series and N2000 Series does **NOT** support legacy SMM mapping of SMM-mode CPU accesses to the DOS legacy range including behind the Legacy Video Area. Instead, SMM must use the HSMMCTL register to setup a range in system memory between 1MB and HMBOUND.

1.7.3.2.2 Monochrome Adapter (MDA) Range (B_0000h-B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD or the DMI Interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the MCH must decode cycles in the MDA range (000B_0000h - 000B_7FFFh) and forward either to IGD or to the DMI Interface. This capability is controlled by a VGA steering bits. In addition to the memory range B0000h to B7FFFh, the IMC decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD and/or the DMI Interface.

1.7.3.3 Expansion Area (C_0000h-D_FFFFh)

Intel Atom Processor D2000 series and N2000 Series does **NOT** Support ISA Expansion region. This area always maps to system DRAM.

1.7.3.4 PAM Memory Area (E_0000h-F_FFFFh)

The range from 768 KB to 1024 KB is known as the PAM Memory Area. It is divided into two sections, used for BIOS access, and shadowing.

Because writes to the PAM area always target DRAM, Intel Atom Processor D2000 series and N2000 Series supports Implicit Writebacks (IWBs) to this area. The CPU can map this area as cacheable using the MTRRs once BIOS shadowing has taken place. Note: CPU request that target DMI should never be mapped as cacheable. There should never be an IWB to DMI.

1.7.3.4.1 Extended System BIOS Area (E_0000h-E_FFFFh)

This 64 KByte area (000E_0000h – 000E_FFFFh) is generally used for the BIOS. Writes to this area always target DRAM. Reads to this area target DMI unless HMISC2[READ_ESEG_FROM_DRAM] is set, in which case reads target DRAM.

This basic scheme allows BIOS to copy or shadow BIOS code from DMI (slow) to DRAM (fast) by reading from this range, and then writing the same thing back to this range with HMISC2[READ_ESEG_FROM_DRAM] = 0. Once the copy is performed, BIOS code will set HMISC2[READ_ESEG_FROM_DRAM] = 1 and now, the reads will be from DRAM.

1.7.3.5 System BIOS Area (F_0000h-F_FFFFh)

This 64 KByte area (000F_0000h – 000F_FFFFh) is generally used for the BIOS. Writes to this area always target DRAM. Reads to this area target DMI unless HMISC2[READ_FSEG_FROM_DRAM] is set, in which case reads target DRAM.

This basic scheme allows BIOS to copy or shadow BIOS code from DMI (slow) to DRAM (fast) by reading from this range, and then writing the same thing back to this range with HMISC2[READ_FSEG_FROM_DRAM] = 0. Once the copy is performed, BIOS code will set HMISC2[READ_FSEG_FROM_DRAM] = 1 and now reads will be from DRAM.

1.7.4 Main Memory Address Range (1 MB - HMBOUND)

Prior MCHs allowed all accesses in the range from 1MB to the Top of Low Usable DRAM (TOLUD) to target DRAM, but then excluded the optional TSEG, ISA Hole, and IGD stolen VGA memory.

Intel Atom Processor D2000 series and N2000 Series makes this more explicit by adding the HMBOUND register. The Main Memory Address Range is defined as from 1 MB to the address given in the HMBOUND register. All accesses in this range will be sent to DRAM (subject to permission checking performed by the IMR registers).

1.7.4.1 ISA Hole (15 MB-16 MB)

A hole can be created at 15 MB-16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI Interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB-16 MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used by validation and customer SV teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15-16 MB window.

Intel Atom Processor D2000 series and N2000 Series Does **NOT** support the ISA Hole Feature.

1.7.4.2 TSEG (SMMRange – HSMMCTL)

TSEG is below IGGTT stolen memory, which is at the top of Low Usable physical memory (TOLUD).

SMM-mode CPU accesses to enabled TSEG access the physical DRAM at the same address which requires that it is located in the Main Memory Range (below HMBOUND).

- DMI, GFX, VED request to SMM Range. There is no protection other than the IMRs.

1.7.4.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< BMBOUND) are created for SMM-mode, legacy VGA graphics compatibility, and GFX GTT stolen memory. It is the responsibility of BIOS to properly initialize these regions.

1.7.5 PCI* Memory Address Range (HMBOUND - 4 GB)

This address range, from HMBOUND to 4 GB is normally mapped to the DMI Interface.

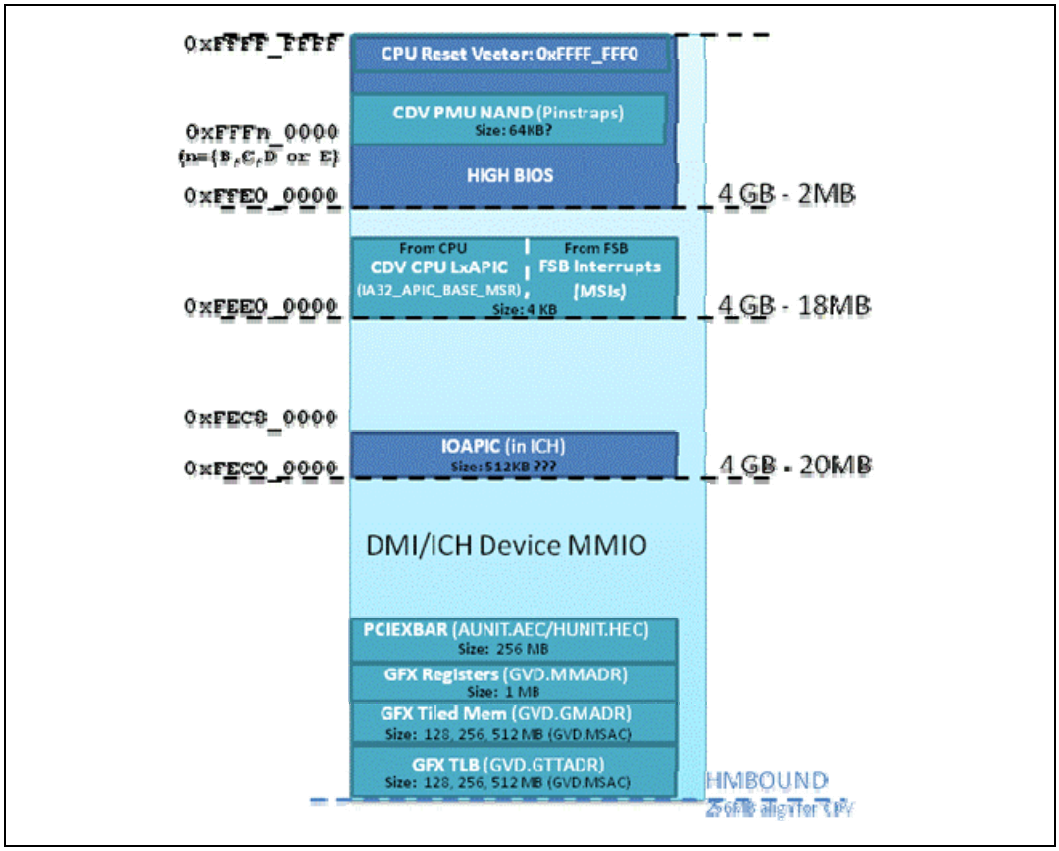
Exceptions to this include:

- The Device 0 MMIO ranges documented in Device 0 (0/0/0) Memory Map
- The Device 2 MMIO ranges documented in Devise 2 (0/2/0) Memory Map
- APIC Related Ranges documented below.

Note: PNV indicated the range from TOLUD – 4GB, but they excluded the stolen memory ranges

All Intel Atom Processor D2000 series and N2000 Series MMIO Bars may be mapped to this range.

Figure 1-3.PCI MMIO Memory Address Range (HMBOUND – 4 GB)



1.7.5.1 IO APIC Configuration Space (FEC0_0000h-FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the PCH portion of the chipset, but may also exist as stand-alone components like PXH.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FECF_FFFFh) are always forwarded to DMI.

1.7.5.2 CPU Local APIC (FEE0_0000h – FEE0_3FFFh – CPU Only)

The CPU Local APIC base address is found in the IA32_APIC_BASE_MSR. It defaults to 0xFEE0_0000. While it is relocatable to resolve address conflicts, there really is no need to do this in a Intel Atom Processor D2000 series and N2000 Series system. From the CPU Core side, this range must be mapped as uncacheable. Each thread sees a unique set of LAPIC registers at this address that are not accessible from other threads.

1.7.5.3 High BIOS Area

The top 2 MB (FFE0_0000h -FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset (physical address FFFF_FFF0h). This region is mapped to DMI Interface so that the upper subset of this region aliases to 16 MB-256 KB range. The actual address space required for the BIOS is less than 2 MB but the minimum CPU MTRR range for this region is 2 MB so that full 2 MB must be considered.

1.7.6 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM.

1.7.6.1 SMM Space Definition

SMM space is defined by its addressed SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. The table below describes three unique address ranges:

These abbreviations are used later in the table describing SMM Space Transaction Handling.

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

Intel Atom Processor D2000 series and N2000 Series Only support SMM to the HSMMCTL region. Because it must be addressable by the CPU (when in SMM mode) is must below HMBOUND.

1.7.6.2 BIOS Programming Restriction

See the BIOS Writer's Guide Vol2 for more details.

1.7.7 Intel Atom Processor D2000 series and N2000 Series Internal Enforcement of SMM Protection

Note: Intel Atom Processor D2000 series and N2000 Series will automatically filter CPU request from threads that are not in SMM mode that hit the SMM range. Writes will be dropped and reads will return all 1's.

Note: Access to the SMM area of physical address space from agents other than the CPU including ICH/PCH devices from DMI and Intel Atom Processor D2000 series and N2000 Series internal devices including the GFX TLB, but be prevented. It is the responsibility of BIOS to use an IMR for this functionality.

1.7.7.1 CPU WB Transaction to an Enabled SMM Address Space

CPU Writeback transactions (REQa[1]# = 0) to enabled SMM Address Space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

It is the responsibility of BIOS to ensure that the SMM physical address range is not exposed to the operating system or used for any other function.

BIOS must also program the SMRR register in the CPU(s) to prevent a cache based security risk.

1.7.8 I/O Address Space

The MCH generates DMI Interface bus cycles for all CPU I/O accesses that it does not claim. Within the host bridge, the MCH contains two internal registers in the CPU I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement configuration space access mechanism.

The CPU allows 64K+3 bytes to be addressed within the I/O space. The MCH propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when CPU bus HA_16 address signal is asserted. HA_16 is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA_16 is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics IO decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI Interface bus. I/O writes are NOT posted. Memory writes to PCH are posted.

The MCH responds to I/O cycles initiated on DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If they do, they are dropped in the Intel Atom Processor D2000 series and N2000 Series DMI controller.

PNV mechanism: If one does occur, the request will route as a read to Memory address 000C_0000h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with an UR completion status. << They appears to count on this for error handling in a few places including here and SMM violations. Should Intel® Atom™ Processor D2000 series and N2000 Series use this generic completion mechanism (reads go here with UR completion and writes go here with BE=0? >>

For IA-based processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the CPU as 1 transaction. The MCH will break this into 2 separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the CPU.

1.7.8.1 DMI Interface Decode Rules

The full description of CDV's DMI support is found in section DMI in EDS Vol 1.

Intel Atom Processor D2000 series and N2000 Series Rules

- Read and write DMI request >64GB will be handed as unsupported request.
- Snooped VCm and VC1 request (non_snooped==0) will be handled as unsupported request.
- MSI request (mem_wr with address[31:20] = ='hFEE) with DW len != 1 or VC!=0 will be drop (VC!=0 is new condition since the A unit can't handle them)
- All requests between HMBOUND and 4GB will be treated as an IMR violation.
- I/O cycles and configuration cycles are not supported in the upstream direction.
- All other protection is provided by the IMRs and the VC3Protect.
- The MCH does not support transactions that cross device boundaries. This should never occur because PCI Express transactions are not allowed to cross a 4KB boundary.
- For reads, the MCH will provide separate completion status for each naturally-aligned 64 byte block.
- VC0 (enabled by default)
- Snoop port and Non-snoop Asynchronous transactions are supported.
- MSI can occur.
- VCp (optionally enabled) – priority snooped traffic.
- ½ linked to VC0. See DMI section Vol1.
- MSI on VCP is not supported.
- VC1 (optionally enabled) – Supports non-snooped transactions only.
- The snoop not required (SNR) bit must be set. Any transaction with the SNR bit not set will be treated as an unsupported request.

1.8 IO (PORT IN/OUT) Space

1.8.1 IO (PORT IN/OUT) Space

The CPU allows 64K+3 bytes to be addressed within the I/O space. This occurs whenever an I/O access is made to:

- 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh.
- bytes from address 0FFFFh.

BIOS is responsible for making sure that no I/O device on cDMI uses I/O addresses 0FFFDh, 0FFFEh, or 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access – CF8h, CFCh) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

I/O writes are NOT posted. Memory writes to Intel Atom Processor D2000 series and N2000 Series internal devices or cDMI are posted.

The I/O map is divided into separate types. Fixed ranges cannot be moved, but in some cases can be disabled. Variable ranges can be moved and can also be disabled.

1.8.2 Fixed I/O Address Ranges

Below are the Fixed I/O decode ranges from the CPU.

Start	End	Read Target	Write Target	Can Disable?
3B0h	3BBh	VGA	VGA	Yes. DISPLAY_CONTROLLER. MSR
3C0h	3DFh	VGA	VGA	Yes. DISPLAY_CONTROLLER. MSR
CF8h*	CFBh	PCI Config Index Register	PCI Config Index Register	No
CFCh	CFFh	PCI Config Data Register	PCI Config Data Register	No

*DWord (32bit) accesses only.

1.8.3 Variable I/O (PORT) Address Blocks

All I/O PORT ranges should be natively aligned (a 16Byte range should begin on a 16Byte boundary). Each range has an enable bit.

Range Name	Register	Size (Bytes)	Description
APMBA	APMBA	16	Active Power Management (APM) I/O Base Address

Range Name	Register	Size (Bytes)	Description
GFX_IOBAR	GVD.GFX_IOBAR	8	Graphics/Video Indexed Register Access
OSPMBA	OSPMBA	64	OS Power Management I/O Base Address
PMBA	PMBA	16	Power Management I/O Base Address
PSMIBA	PSMIBA	16	PSMI I/O Base Address

1.8.4 IO Space registers

Base	Offset	Description
APMBA	00h	**APM_CMD:** Active Power Gate Control Register; This register indicates the configuration of the voltage islands for the various blocks that the “Power Management Controller (PMU)” controls. This register is updated by the software driver to request power up/power down of the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island. Each island is controlled by a 2-bit field. The upper bit (bit 1) is used by software to request power up, and the lower bit (bit 0) is used by software to request power down. At reset/power up, all the Islands comes up enabled (00) indicating that software is not requesting power up/down.. The register fields are set by software via the Message Bus interface. Hardware clears the bits when the request is serviced.
APMBA	04h	**APM_STS:** Power Gate Status; This register indicates the status of the voltage islands for the various blocks that the “Power Management Controller (PMU)” controls. This register is updated by hardware. 2 bits are used to indicate power up/power down status of each the islands: viz. the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island as shown in the table below. At reset/power up, all the Islands comes up enabled (D0).
APMBA	0Ch	**APM_IE:** Power Gate Interrupt Enable; This register indicates the interrupt enables for the power islands for the various blocks that the “Power Management Controller (PMU)” controls. The software driver sets this bit to trigger an interrupt when the particular island is brought back to D0. There is one bit for each of the islands: viz. the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island as shown in the table below. . At reset/power up, all IE comes up as 0, indicating interrupts are not enabled
GFX_IOBAR	00h	**GVD.MMIO_INDEX:** GVD MMIO Index Register: A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed by the GMCH but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver. This register must not be accessed via the IOSF bus and the message bus at the same time as the results will be unpredictable. Access

Base	Offset	Description
		through the message bus is only for save/restore and debug purposes.
GFX_IOBAR	04h	**GVD.MMIO_DATA:** GVD MMIO Data Register: A 32 bit IO write to this port is re-directed to the MMIO register/GTT location pointed to by the MMIO-index register. A 32 bit IO read to this port is re-directed to the MMIO register address pointed to by the MMIO-index register regardless of the target selection in MMIO_INDEX[1:0]. 8 or 16 bit IO writes are completed by the GMCH and may have un-intended side effects, hence must not be used to access the data port. 8 or 16 bit IO reads are completed normally. Note that if the target field in MMIO Index selects
OSPMBA	00h	**PM_STS:** PMU Status
OSPMBA	04h	**PM_CMD:** PM Command Register
OSPMBA	08h	**PM_ICS:** PM Interrupt Control and Status Register
OSPMBA	20h	**PM_SSC:** PM Subsystem Configuration
OSPMBA	30h	**PM_SSS:**
PMBA	00h	**PCNT:** Processor Control
PMBA	04h	**LVL2:** Level 2 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C2 request
PMBA	05h	**LVL3:** Level 3 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C3 request. If software simultaneously reads LVL2 and LVL3, SCH performs a C2 transition.
PMBA	06h	**LVL4:** Level 4 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C4 request. If software simultaneously reads LVL2, LVL3, and LVL4, SCH performs a C2 transition.
PMBA	07h	**LVL5:** Level 5 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C5 request. If software simultaneously reads LVL2, LVL3, LVL4 and LVL5, SCH performs a C2 transition.
PMBA	08h	**LVL6:** Level 6 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C6 request
PMBA	0Ch	**C6C:** C6 Control Register; This is a read only register. It provides information on the last C-state entered and residency in the last entered C-state. This register is not expected to be saved across AOAC Standby, since Lincroft will return to C0 on a wakeup event. For residency information across AOAC Standby, information is provided by residency counter registers in Langwell.
PSMIBA	00h	**PSMI_PREP:** PSMI PREPARE REGISTER; This is not a real register. Reading it triggers the "Power Management Controller (PMU)" to perform "Power Management Controller (PMU)" to prepare to save for PSMI. The "Power Management Controller (PMU)" actually returns all zeros to transfer control back to PSMI handler. DO NOT WRITE TO THIS REGISTER

Base	Offset	Description
PSMIBA	04h	**PSMI_SAVE:** PSMI SAVE REGISTER; This is not a real register. Reading it triggers the “Power Management Controller (PMU)” to perform save routine to save registers into memory. The “Power Management Controller (PMU)” actually returns all zeros to transfer control back to PSMI handler. DO NO WRITE TO THIS REGISTER
PSMIBA	08h	**PSMI_RESTORE:** PSMI RESTORE REGISTER; This is not a real register. Reading it triggers the “Power Management Controller (PMU)” to perform restore routine. The “Power Management Controller (PMU)” actually returns all zeros to transfer control back to PSMI handler. DO NOT WRITE TO THIS REGISTER
PSMIBA	0Ch	**PSMI_SAVE_BASE_ADDR:** PSMI SAVE BASE ADDRESS REGISTER; This is a 32-bit R/W register. It stores the base address of the DRAM location where state information is saved for PSMI.

1.9 MMIO Space

1.9.1 MMIO Space

The following table shows (from the CPU perspective) the non-DRAM memory ranges that Intel Atom Processor D2000 series and N2000 Series GMCH will decode. Non-DRAM cycles that are not directed to any of the internal memory targets will be sent down DMI to the ICH.

See the Memory Map section 1.4 of this document for a description of how Intel Atom Processor D2000 series and N2000 Series determines if an address maps to DRAM or is available for MMIO claiming.

This section describes only the internal registers that are accessible from MMIO. The Memory Map section 1.4 has a full description of all the MMIO ranges that are decoded including those that don’t have registers.

1.9.2 MMIO Space Registers

Base	Offset	Description
MMADR	00 70410h	**DISPLAY_CONTROLLER.SWFXX:** These 32 bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.
MMADR	02020h	**GVD.PGTBL_CTL:** Page Table Control. The PGTBL_CTL register is provides the starting physical memory address of the Graphics Translation Table (GTT). ; Once a GTT is established, software must use the GTTADR space to update entries in the GTT. GTTADR is a 256KB space claimed by graphics device during PCI enumeration. This allows the device to ; The GTT must be 4KByte aligned. The GTT must reside in unsnooped Main Memory and must be contiguous 256KBs.
MMADR	02024h	**GVD.PGTBL_ER:** Page Table Error. The PGTBL_ER Debug register stores information indicating the source of an error associated with GM

Base	Offset	Description
		mapping via GTT. XX_INVALID_GTE_PTE: Translated Page Table Entry (PTE) is marked as not valid. Implemented by all streams. Detected at translation time.
MMADR	02028h	**GVD.CLAIM_ER:** Claim Error Counter - counts the RM claim error (no RM claim) reported at CLAIM_ERROR field of EIR.
MMADR	02050h	**GVD.MISR4:** MISR4
MMADR	02060h	**GVD.GFX_GVD_CG_DIS:** GFX/GVD Clock Gating Disable
MMADR	02064h	**GVD.VED_CG_DIS:** VED Clock Gating Disable
MMADR	02084h	**GVD.IIR_RW:** Alternate means to access the IIR register. This address provides software RW access to the IIR register. Write/Restore to the IIR register using this address will not trigger an interrupt to the CPU.
MMADR	02098h	**GVD.GVD_ECO:** Spare Register for HW ECOs
MMADR	0209Ch	**GVD.SCPD0:** Scratch Pad 0 Register
MMADR	020A0h	**GVD.IER:** IER: Interrupt Enable Register. The IER register contains an interrupt enable bit for each interrupt bit in the Interrupt Identity Register (IIR) register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources. The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set.
MMADR	020A4h	**GVD.IIR:** IIR: Interrupt Identity Register. The IIR register contains the persistent values of the interrupt bits that are unmasked by the IMR and thus can generate a CPU interrupt (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Bits set in this register will remain set until the interrupt condition is cleared by software. Writing a 1 into the appropriate bit position within this register clears interrupts. ; Programming Note: Prior to clearing a Display Pipe-sourced interrupt (e.g., Display Pipe A VBLANK) in the IIR, the corresponding interrupt (source) status in the PIPEASTAT register (e.g., Pipe A VBLANK Interrupt Status bit of PIPEASTAT) must first be cleared.
MMADR	020A8h	**GVD.IMR:** IMR: Interrupt Mask. The IMR register is used by software to control which ISR bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and therefore cannot generate CPU interrupts.
MMADR	020ACh	**GVD.ISR:** Interrupt Status The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts. The User Interrupt bit in this register is a short pulse therefore software should not expect to use this register to sample these conditions.
MMADR	020B0h	**GVD.EIR:** Error Identity. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register (ISR). In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.

Base	Offset	Description
MMADR	020B4h	**GVD.EMR:** Error Mask. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.
MMADR	020B8h	**GVD.ESR:** Error Status. This register contains the non-persistent values of all hardware-detected error condition bits.
MMADR	020C8h	**GVD.DISP_CLK_FREQ:** Encoding of Display clock and Core clock frequency as determined by CCK unit.
MMADR	020CCh	**GVD.GM_FREQ:** The Display clock frequency to be used for generating the GM clock.
MMADR	020D4h	**GVD.GTHROT:** GVD Thermal Throttling Register programmed by SBIOS.
MMADR	020E0h	**GVD.FW_BLC_SELF:** Display FIFO Watermark
MMADR	020E4h	**GVD.MI_ARB:** Display FIFO Watermark
MMADR	020F4h	**GVD.G_LP_CONTROL:** GVD LP Arbitration Control Register
MMADR	020F8h	**GVD.G_HP_CONTROL:** GVD HP Arbitration Control Register
MMADR	020FCh	**GVD.G_CONTROL:** GVD Control Register
MMADR	02100 02103h	**DISPLAY_CONTROLLER.DPIO_PACKET_REGISTER:** Description Control and Address of DPIO indirect
MMADR	02100h	**GVD.SB_PCKT:** When the Sideband Packet Register is written, the “GFX/VED/Media configuration” creates a transaction towards the destination agent on the IOSF sideband channel, using the fields sent with the write operation as transaction parameters, as described below: ; - The Sideband Rid filed (bits 31:24) is used as the transaction Rid ; - The Sideband Opcode filed (bits 23:15) is used as the transaction opcode ; - The Sideband Port filed (bits 15:8) is used as the transaction destination port ; - The source port is hard-coded to 6h (“GFX/VED/Media configuration” port) ; - The Sideband Byte Enable Field (bits 7:4) is used as the transaction Byte Enable ; If the opcode results in a data write semantic transaction, the write-data will be taken from the Sideband Data Register. If the opcode results in a data read semantic transaction, the read- data will be placed in the Sideband Data Register and may later be read by software. ; When Sideband Busy is set, Sideband Packet Register, Sideband Data Register and Sideband Address Register fields cannot be written. If the opcode results in a data read semantic transaction, data will be ready at Sideband Data register only when the Sideband Busy is cleared.
MMADR	02104h	**GVD.SB_DATA:** The Sideband Data Register is used by the sideband register access mechanism (triggered by Sideband Packet Register) for holding write-data in write-transactions or read-data for read-transactions as explained below
MMADR	02104h 02107h	**DISPLAY_CONTROLLER.DPIO_DATA_REGISTER:** Description Data of DPIO indirect
MMADR	02108h	**GVD.SB_ADDR:** The Sideband Address Register is used by the sideband transaction (triggered by Sideband Packet Register) for holding the address (of the internal register, within the destination unit).
MMADR	02110h	**GVD.DPIO_CFG:** DPIO configuration register. Note: the reset signal for this register is the `CDV.pmu_xxx_powergood_zcrnfwh

Base	Offset	Description
MMADR	05010h	**DISPLAY_CONTROLLER.GPIOCTL_0:** Description GPIO I2C register gmbus_register. v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
MMADR	05014h	**DISPLAY_CONTROLLER.GPIOCTL_1:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
MMADR	05018h	**DISPLAY_CONTROLLER.GPIOCTL_2:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
MMADR	0501Ch	**DISPLAY_CONTROLLER.GPIOCTL_3:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4

Base	Offset	Description
		These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
MMADR	05020h	**DISPLAY_CONTROLLER.GPIOCTL_4:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
MMADR	05100h	**DISPLAY_CONTROLLER.GMBUS0:** Description GMBUS clock and port select gmbus_register.v reg_gmbus0 The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to. The clock rate options are 50KHz 100KHz 400KHz and 1MHz. This register should be set before the first data valid bit is set because it will be read only at the very first data valid bit and not read during the period of the transmission until stop is issued and next first data valid bit is set.
MMADR	05104h	**DISPLAY_CONTROLLER.GMBUS1:** Description GMBUS command and status gmbus_register.v reg_gmbus1 This register lets the software indicate to the GMBUS controller the slave device address register index and indicate when the data write is complete. When the SW_CLR_INT bit is asserted all writes to the GMBUS2 GMBUS3 and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.
MMADR	05108h	**DISPLAY_CONTROLLER.GMBUS2:** Description GMBUS status gmbus_register.v reg_gmbus2
MMADR	0510Ch	**DISPLAY_CONTROLLER.GMBUS3:** Description GMBUS data buffer gmbus_register.v reg_gmbus3 This is data read write register. This

Base	Offset	Description
		register is double buffered. Bit 0 is the first bit sent or read bit 7 is the 8thbit sent or read all the way through bit 31 being the 32ndbit sent or read. For GMBUS write operations with a non zero byte count this register be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.
MMADR	05110h	**DISPLAY_CONTROLLER.GMBUS4:** Description GMBUS interrupt mask gmbus_register.v reg_gmbus4
MMADR	05120h	**DISPLAY_CONTROLLER.GMBUS5:** Description GMBUS index gmbus_register.v reg_gmbus5 This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.
MMADR	05130h	**DISPLAY_CONTROLLER.GMBUS6:** Description GMBUS data buffer gmbus_register.v reg_gmbus6 This is the AKSV write register written by system BIOS on boot. Bit 0 is the first bit sent bit 7 is the 8thbit sent through bit 31 being the 32ndbit sent.
MMADR	05134h	**DISPLAY_CONTROLLER.GMBUS7:** Description GMBUS data buffer gmbus_register.v reg_gmbus7 This is the AKSV write register written by system BIOS on boot. Bit 0 is the first bit sent through bit 7 being the 8thbit sent.
MMADR	06014h	**DISPLAY_CONTROLLER.DPLLA_CTRL:** Description DPLL A Control cpdmmreg.v reg03_lt
MMADR	06018h	**DISPLAY_CONTROLLER.DPLLB_CTRL:** Description DPLL B Control cpdmmreg.v reg04_lt
MMADR	0601Ch	**DISPLAY_CONTROLLER.DPLLAMD:** Description Pipe A multiply cpdmmreg.v reg15_lt
MMADR	06020h	**DISPLAY_CONTROLLER.DPLLBMD:** Description Pipe B multiply cpdmmreg.v reg16_lt
MMADR	06104	**DISPLAY_CONTROLLER.D_STATE:** Description Power state behavior cpdmmreg.v reg11_lt
MMADR	06200h	**DISPLAY_CONTROLLER.DSPCLK_GATE_D:** Description clock gating cpdmmreg.v reg12_lt
MMADR	06210h	**DISPLAY_CONTROLLER.RAMCLK_GATE_D:** Description memory clock gating cpdmmreg.v gfxramcg2
MMADR	0A000h	**DISPLAY_CONTROLLER.DPALETTE_A:** Table 8206 1 8209 2. 8 Bit Mode
MMADR	0A800h	**DISPLAY_CONTROLLER.DPALETTE_B:** 8 Bit Mode
MMADR	30000h	**DISPLAY_CONTROLLER.OVADD:** This register provides a graphics memory address that will be used on the next Overlay register update. This graphics memory address points to an array of Overlay registers. This register cannot be used to flip the overlay if the cache has not been configured through a command pipe flip packet.
MMADR	30004h	**DISPLAY_CONTROLLER.OTEST:**

Base	Offset	Description
MMADR	30008h	**DISPLAY_CONTROLLER.DOVSTA:** This read only register indicates status for the overlay. Since the Overlay pipe can be assigned to either display pipe references to display are either the pipe A timing generator or the pipe B timing generator depending on which the Overlay logic is currently slaved to.
MMADR	3000Ch	**DISPLAY_CONTROLLER.DOVSTAEX:** This read only register provides extended status information about the overlay. The format is RESERVED.
MMADR	30010h	**DISPLAY_CONTROLLER.OGAMC5:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
MMADR	30014h	**DISPLAY_CONTROLLER.OGAMC4:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
MMADR	30018h	**DISPLAY_CONTROLLER.OGAMC3:** These registers are used to

Base	Offset	Description
		determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
MMADR	3001Ch	**DISPLAY_CONTROLLER.OGAMC2:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
MMADR	30020h	**DISPLAY_CONTROLLER.OGAMC1:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential

Base	Offset	Description
		points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
MMADR	30024h	**DISPLAY_CONTROLLER.OGAMC0:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
MMADR	30058h	**DISPLAY_CONTROLLER.OVRSYNCPH0:**
MMADR	3005Ch	**DISPLAY_CONTROLLER.OVRSYNCPH1:**
MMADR	30060h	**DISPLAY_CONTROLLER.OVRSYNCPH2:**
MMADR	30064h	**DISPLAY_CONTROLLER.OVRSYNCPH3:**
MMADR	30100h	**DISPLAY_CONTROLLER.OBUF_0Y:** This register value is mirrored from DDR in address 00h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
MMADR	30104h 30107	**DISPLAY_CONTROLLER.OBUF_1Y:** This register value is mirrored from DDR in address 04h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
MMADR	30108h	**DISPLAY_CONTROLLER.OBUF_0U:** This register value is mirrored

Base	Offset	Description
	3010B	from DDR in address 08h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
MMADR	3010Ch	**DISPLAY_CONTROLLER.OBUF_0V:** This register value is mirrored from DDR in address 0Ch R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
MMADR	30110h 30113	**DISPLAY_CONTROLLER.OBUF_1U:** This register value is mirrored from DDR in address 10h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
MMADR	30114h	**DISPLAY_CONTROLLER.OBUF_1V:** This register value is mirrored from DDR in address 14h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
MMADR	30118h 3011B	**DISPLAY_CONTROLLER.OSTRIDE:** This register value is mirrored from DDR in address 18h R W . These values represent the stride of the overlay video data buffers. A stride value determines the line to line increment of the buffer which is independent of the actual width of the overlay video data that gets displayed. . The memory Address Offset in DDR is Read Write.
MMADR	3011Ch	**DISPLAY_CONTROLLER.YRGB_VPH:** This register value is mirrored from DDR in address 1Ch R W . The memory Address Offset in DDR is Read Write.
MMADR	30120h	**DISPLAY_CONTROLLER.UV_VPH:** This register value is mirrored from DDR in address 20h R W . The memory Address Offset in DDR is Read Write.
MMADR	30124h	**DISPLAY_CONTROLLER.HORZ_PH:** This register value is mirrored from DDR in address 24h R W . The memory Address Offset in DDR is Read Write.
MMADR	30128h	**DISPLAY_CONTROLLER.INIT_PHS:** This register value is mirrored from DDR in address 28h R W . This register provides a method to create a negative initial phase or one with a positive integer offset. If the corresponding bits are set to all ones the initial phase is the fractional phase register value minus one. These bits should only be set in cases where the buffer pointer is pointing to the first pixel of the line or column because it will effectively cause the first pixel to be duplicated. The memory Address Offset in DDR is Read Write.
MMADR	3012Ch	**DISPLAY_CONTROLLER.DWINPOS:** This register value is mirrored from DDR in address 2Ch R W . The memory Address Offset in DDR is

Base	Offset	Description
		Read Write.
MMADR	30130h	**DISPLAY_CONTROLLER.DWINSZ:** This register value is mirrored from DDR in address 30h R W . The memory Address Offset in DDR is Read Write.
MMADR	30134h	**DISPLAY_CONTROLLER.SWIDTH:** This register value is mirrored from DDR in address 34h R W . The memory Address Offset in DDR is Read Write.
MMADR	30138h	**DISPLAY_CONTROLLER.SWIDTHSW:** This register value is mirrored from DDR in address 38h R W . Hardware uses values in this register to determine the number of SWORDs 32 bytes to be fetched from the memory for each overlay source scan line. The memory Address Offset in DDR is Read Write.
MMADR	3013Ch	**DISPLAY_CONTROLLER.SHEIGHT:** This register value is mirrored from DDR in address 3Ch R W . The memory Address Offset in DDR is Read Write.
MMADR	30140h	**DISPLAY_CONTROLLER.YRGBSCALE:** This register value is mirrored from DDR in address 40h R W . The memory Address Offset in DDR is Read Write.
MMADR	30144h	**DISPLAY_CONTROLLER.UVSCALE:** This register value is mirrored from DDR in address 44h R W . The memory Address Offset in DDR is Read Write.
MMADR	30148h	**DISPLAY_CONTROLLER.OCLRC0:** This register value is mirrored from DDR in address 48h R W . The memory Address Offset in DDR is Read Write.
MMADR	3014Ch	**DISPLAY_CONTROLLER.OCLRC1:** This register value is mirrored from DDR in address 4Ch R W . The sum of the absolute value of SH_SIN and SH_COS must be limited to less than 8. The memory Address Offset in DDR is Read Write.
MMADR	30150h	**DISPLAY_CONTROLLER.DCLRKV:** This register value is mirrored from DDR in address 50h R W . The memory Address Offset in DDR is Read Write.
MMADR	30154h	**DISPLAY_CONTROLLER.DCLRKM:** This register value is mirrored from DDR in address 54h R W . The memory Address Offset in DDR is Read Write.
MMADR	30158h	**DISPLAY_CONTROLLER.SCHRKVH:** This register value is mirrored from DDR in address 58h R W . The memory Address Offset in DDR is Read Write.
MMADR	3015Ch	**DISPLAY_CONTROLLER.SCHRKVL:** This register value is mirrored from DDR in address 5Ch R W . The memory Address Offset in DDR is Read Write.
MMADR	30160h	**DISPLAY_CONTROLLER.SCHRKEN:** This register value is mirrored from DDR in address 60h R W . The memory Address Offset in DDR is Read Write.
MMADR	30164h	**DISPLAY_CONTROLLER.OCONFIG:** This register value is mirrored from DDR in address 64h R W . The memory Address Offset in DDR is Read Write.

Base	Offset	Description
MMADR	30168h	**DISPLAY_CONTROLLER.OCOMD:** This register value is mirrored from DDR in address 68h R W . This register and the Overlay Configuration register provide the basic programming options that the overlay engine needs to begin its work. The memory Address Offset in DDR is Read Write.
MMADR	30170h	**DISPLAY_CONTROLLER.OSTART_0Y:** This register value is mirrored from DDR in address 70h R W . The memory Address Offset in DDR is Read Write.
MMADR	30174h	**DISPLAY_CONTROLLER.OSTART_1Y:** This register value is mirrored from DDR in address 74h R W . The memory Address Offset in DDR is Read Write.
MMADR	30178h	**DISPLAY_CONTROLLER.OSTART_0U:** This register value is mirrored from DDR in address 78h R W . The memory Address Offset in DDR is Read Write.
MMADR	3017Ch	**DISPLAY_CONTROLLER.OSTART_0V:** This register value is mirrored from DDR in address 7Ch R W . The memory Address Offset in DDR is Read Write.
MMADR	30180h	**DISPLAY_CONTROLLER.OSTART_1U:** This register value is mirrored from DDR in address 80h R W . The memory Address Offset in DDR is Read Write.
MMADR	30184h	**DISPLAY_CONTROLLER.OSTART_1V:** This register value is mirrored from DDR in address 84h R W . The memory Address Offset in DDR is Read Write.
MMADR	30188h	**DISPLAY_CONTROLLER.OTILEOFF_0Y:** This register value is mirrored from DDR in address 88h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
MMADR	3018Ch	**DISPLAY_CONTROLLER.OTILEOFF_1Y:** This register value is mirrored from DDR in address 8Ch R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
MMADR	30190h	**DISPLAY_CONTROLLER.OTILEOFF_0U:** This register value is mirrored from DDR in address 90h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
MMADR	30194h	**DISPLAY_CONTROLLER.OTILEOFF_0V:** This register value is mirrored from DDR in address 94h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in

Base	Offset	Description
		linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
MMADR	30198h	**DISPLAY_CONTROLLER.OTILEOFF_1U:** This register value is mirrored from DDR in address 98h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
MMADR	3019Ch	**DISPLAY_CONTROLLER.OTILEOFF_1V:** This register value is mirrored from DDR in address 9Ch R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
MMADR	301A0h	**DISPLAY_CONTROLLER.RESERVED:** This register value is mirrored from DDR in address 0h R W . The memory Address Offset in DDR is Read Write.
MMADR	301A4h	**DISPLAY_CONTROLLER.UVSCALEV:** This register value is mirrored from DDR in address 4h R W . The memory Address Offset in DDR is Read Write.
MMADR	30300h	**DISPLAY_CONTROLLER.Y_VCOEFS:** This register value is mirrored from DDR in address 200h R W . The memory Address Offset in DDR is Read Write. The offset is 200h 2FFh
MMADR	30400h	**DISPLAY_CONTROLLER.Y_HCOEFS:** This register value is mirrored from DDR in address 300h R W . The memory Address Offset in DDR is Read Write. The offset is 300h 4FFh
MMADR	30600h	**DISPLAY_CONTROLLER.UV_VCOEFS:** This register value is mirrored from DDR in address 500h R W . The memory Address Offset in DDR is Read Write. The offset is 500h 5FFh
MMADR	30700h	**DISPLAY_CONTROLLER.UV_HCOEFS:** This register value is mirrored from DDR in address 600h R W . The memory Address Offset in DDR is Read Write. The offset is 600h 6FFh.
MMADR	60000h	**DISPLAY_CONTROLLER.HTOTAL_A:**
MMADR	60004h	**DISPLAY_CONTROLLER.HBLANK_A:**
MMADR	60008h	**DISPLAY_CONTROLLER.HSYNC_A:**
MMADR	6000Ch	**DISPLAY_CONTROLLER.VTOTAL_A:**
MMADR	60010h	**DISPLAY_CONTROLLER.VBLANK_A:**
MMADR	60014h	**DISPLAY_CONTROLLER.VSYNC_A:**
MMADR	6001Ch	**DISPLAY_CONTROLLER.PIPESRCA:**
MMADR	60020h	**DISPLAY_CONTROLLER.BCLRPAT_A:** This register value determines what color should be sent to the display in the border region the space

Base	Offset	Description
		between the end of active and the beginning of blank and the end of blank and the beginning of active.
MMADR	60028h	**DISPLAY_CONTROLLER.VSYNCSHIFT_A:**
MMADR	60050h	**DISPLAY_CONTROLLER.CRCCTRLREDA:** The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. For any changes to the CRC controls you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. Border area is always included in the CRC calculation. There are five CRC calculators Red Green Blue Residual1 and Residual2 DevCTG DevCedarview processoreach with an 8 bit data input and 23 bit CRC result. For Display Port CRC DevCTG DevCedarview processor the 40 bit lane data is spread across the inputs of all five of the CRC calculators. For Pipe the 30 bit pixel data is spread across the inputs of four of the CRC calculators. The fifth is unused and will be ignored for expected CRC comparison and error generation. Pipe CRC should not be run when Display Port or TV is enabled on this pipe.
MMADR	60054h	**DISPLAY_CONTROLLER.CRCCTRLGREENA:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	60058h	**DISPLAY_CONTROLLER.CRCCTRLBLUEA:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	6005Ch	**DISPLAY_CONTROLLER.CRCCTRLALPHAA:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	60060h	**DISPLAY_CONTROLLER.CRCRESREDA:**
MMADR	60064h	**DISPLAY_CONTROLLER.CRCRESGREENA:**
MMADR	60068h	**DISPLAY_CONTROLLER.CRCRESBLUEA:**
MMADR	6006Ch	**DISPLAY_CONTROLLER.CRCRESALPHAA:**
MMADR	60070h	**DISPLAY_CONTROLLER.CRCCTRLRESIDUE2A:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	60080h	**DISPLAY_CONTROLLER.CRCRESRESIDUE2A:** The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	61000h	**DISPLAY_CONTROLLER.HTOTAL_BPIPE_B_HORIZONTAL_TOTAL_REGISTER:**

Base	Offset	Description
MMADR	61004h	**DISPLAY_CONTROLLER.HBLANK_BPIPE_B_HORIZONTAL_BLANK_REGISTER:**
MMADR	61008h	**DISPLAY_CONTROLLER.HSYNC_BPIPE_B_HORIZONTAL_SYNC_REGISTER:**
MMADR	6100Ch	**DISPLAY_CONTROLLER.VTOTAL_BPIPE_BVERTICAL_TOTAL_REGISTER:**
MMADR	61010h	**DISPLAY_CONTROLLER.VBLANK_BPIPE_BVERTICAL_BLANK_REGISTER:**
MMADR	61014h	**DISPLAY_CONTROLLER.VSYNC_BPIPE_B_VERTICAL_SYNC_REGISTER:**
MMADR	6101Ch	**DISPLAY_CONTROLLER.PIPEBSRC:**
MMADR	61020h	**DISPLAY_CONTROLLER.BCLRPAT_B:** This register determines the color sent during the border region the periods between the end of blank and the start of active and the end of active and the start of blank. Also same color will be sent during pseudo border period. VGA border color is determined by the VGA border overscan color register.
MMADR	61028h	**DISPLAY_CONTROLLER.VSYNCSHIFT_B:**
MMADR	61050h	**DISPLAY_CONTROLLER.CRCCTRLREDB:** The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. For any changes to the CRC controls you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. Border area is always included in the CRC calculation. See description of CRCCtrlColorA for more details.
MMADR	61054h	**DISPLAY_CONTROLLER.CRCCTRLGREENB:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.
MMADR	61058h	**DISPLAY_CONTROLLER.CRCCTRLBLUEB:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.
MMADR	6105Ch	**DISPLAY_CONTROLLER.CRCCTRLALPHAB:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.
MMADR	61060h	**DISPLAY_CONTROLLER.CRCRESREDB:**
MMADR	61064h	**DISPLAY_CONTROLLER.CRCRESGREENB:**
MMADR	61068h	**DISPLAY_CONTROLLER.CRCRESBLUEB:**
MMADR	6106Ch	**DISPLAY_CONTROLLER.CRCRESALPHAB:**
MMADR	61070h	**DISPLAY_CONTROLLER.CRCCTRLRESIDUE2B:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except

Base	Offset	Description
		when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	61080h	**DISPLAY_CONTROLLER.CRCRESRESIDUAL2B:** The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
MMADR	61100h	**DISPLAY_CONTROLLER.ADPA:** Description CRT port control dprrega.v adp_Q
MMADR	61104h	**DISPLAY_CONTROLLER.CRTIO_DFX:** Description CRT port control dprrega.v crt_dfx
MMADR	61110h	**DISPLAY_CONTROLLER.PORT_HOTPLUG_EN:** Description DPD enable control dprrega.v ql_hotplugen_Q NOTE For correct operation of display port hot plug detection the device 2 configuration register GMBUSFREQ at offset 0xCC 0xCD must be programmed correctly.
MMADR	61114h	**DISPLAY_CONTROLLER.PORT_HOTPLUG_STAT:** Description CRT port control dprrega.v porthotst_aR This register is the second level of a two level interrupt and status scheme. Status bits in this register are sticky once set they can be cleared by writing a one to that bit. A write of a zero does not affect the corresponding Interrupt status bit. The corresponding enable bits determine if the interrupt status bit should be propagated to the first line interrupt status register. When an interrupt occurs the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt. Before clearing a Port sourced interrupt e.g. CRT hotplug in the IIR the corresponding interrupt source status in the PORT_HOTPLUG_STAT must be cleared by writing a 1 to the appropriate bit. In the case where fields are larger than 1 bit wide all bits in the field must be cleared by writing a 1 to them.
MMADR	61140h	**DISPLAY_CONTROLLER.SDVO_HDMIB:** Description HDMIB port control dprrega.v sdvo_bQ Note This Digital Display Port defaults to sDVO port functionality when it is not programmed as a HDMI port. The operating mode of the port is determined by the setting of the encoding register field bits 11 10.
MMADR	61150h	**DISPLAY_CONTROLLER.SDVO_DP:** Description DFT DPIO and AUX control dprrega.v sdvo_dftQ
MMADR	61154h	**DISPLAY_CONTROLLER.SDVO_DP2:** Description DFT DPT control dprrega.v dpr_dpt_dft2_i
MMADR	61160h	**DISPLAY_CONTROLLER.SDVO_HDMIC:** Description HDMIC port control dprrega.v sdvo_cQ Note This Digital Display Port defaults to sDVO port functionality when it is not programmed as a HDMI port. The operating mode of the port is determined by the setting of the encoding register field bits 11 10.
MMADR	61170h	**DISPLAY_CONTROLLER.VIDEO_DIP_CTL:** Please note that writes to this register take effect immediately. Therefore it is critical for software to follow the write and read sequences as described in the bit 31 text.
MMADR	61178h	**DISPLAY_CONTROLLER.VIDEO_DIP_DATA:** Description Video control dprrega.v only at read if_ramcsrddata
MMADR	61180h	**DISPLAY_CONTROLLER.LVDS:** Description Video control dplreg.v lvds_port_cntl Write Protect by Panel Power Sequencer on

Base	Offset	Description
MMADR	61184h	**DISPLAY_CONTROLLER.LVDSCKT1:** Description PHY LVDSIO TX Control dplrreg.v dsp_lvd_tx_cnt This register contains the control bit to get optimal performance out of LVDS Transmitter circuit
MMADR	61188h	**DISPLAY_CONTROLLER.LVDSCKT2:** Description PHY LVDSIO Analog Control dplrreg.v dsp_lvd_ana_cnt This register contains circuit control bits to optimize analog reference circuit performance of lvdsphy
MMADR	6118ch	**DISPLAY_CONTROLLER.LVDSCKT3:** Description PHY LVDSIO LoopBack Control dplrreg.v dsp_lvd_lb_cnt This register contains circuit control bits to optimize analog reference circuit performance of lvdsphy
MMADR	61190h	**DISPLAY_CONTROLLER.LVDSCKT4:** Description PHY LVDSIO Future used dplrreg.v lvd_dsp_phy_spare
MMADR	61194h	**DISPLAY_CONTROLLER.LVDSTCR:** Description PHY LVDSIO Future used dplrreg.v lvd_dsp_phy_spare
MMADR	61200h	**DISPLAY_CONTROLLER.PP_STATUS:**
MMADR	61204h	**DISPLAY_CONTROLLER.PP_CONTROL:** Description PP Control dplrreg.v pnl_pwr_cntl
MMADR	61208h	**DISPLAY_CONTROLLER.PP_ON_DELAYS:** Description PP On Delay values dplrreg.v DPLRppon_sd Write Protect by Panel Power Sequencer on
MMADR	6120Ch	**DISPLAY_CONTROLLER.PP_OFF_DELAYS:** Description PP Delay Off values dplrreg.v DPLRppoff_sd Write Protect by Panel Power Sequencer on Mobile products
MMADR	61210h	**DISPLAY_CONTROLLER.PP_DIVISOR:** Description PP Divisor dplrreg.v DPLRrefdiv_pp_cd Write Protect by Panel Power Sequencer on Mobile Products. This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is .5 1.5 sec. But limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.
MMADR	61230h	**DISPLAY_CONTROLLER.PFIT_CONTROL:**
MMADR	61234h	**DISPLAY_CONTROLLER.PFIT_PGM_RATIOS:** When programmed scaling mode Panel Fitting Controls 28 26 001 is selected this determines the vertical and horizontal ratios used for panel fitting scaling. The values should be based on the source sizes and active sizes programmed into the pipe timing registers. The values written into the register should be rounded to the proper number of bits for the best precision. The value programmed should be source size register value 1 active size register value 1 When programmed scaling mode is not selected read back of this register gives the auto generated vertical and horizontal scaling ratios used for panel fitting scaling. Register writes will be ignored. The ratios are calculated each VBLANK. When in HiRes modes the values are based on the source sizes and active sizes programmed into the pipe timing registers. When in VGA modes it is determined by the VGA source sizes calculated by the VGA and active sizes from the pipe timing registers. VGA source sizes may have invalid values due to mode change transitions. These will eventually be correct when the mode change is complete. The value read is internally generated source size register value 1 active size register value 1 For

Base	Offset	Description
		each register field the MSB is the 1 bit integer value and the lower 12 bits are the fractional value. A value of 1.0 will indicate 1 1 scaling. A value greater than 1.0 will indicate downscaling. A value less than 1.0 will indicate up scaling. The vertical and horizontal ratios are usually identical except for when source and active aspect ratios differ.
MMADR	61238h	**DISPLAY_CONTROLLER.RESERVED_USED_TO_BE_AUTO_SCALING_RATIOS_READBACK:**
MMADR	6123Ch	**DISPLAY_CONTROLLER.RESERVED_USED_TO_BE_SCALING_INITIAL_PHASE:**
MMADR	61250h	**DISPLAY_CONTROLLER.BLC_PWM_CLT2:**
MMADR	61254h	**DISPLAY_CONTROLLER.BLC_PWM_CTL:**
MMADR	61260h	**DISPLAY_CONTROLLER.BLM_HIST_CTL:**
MMADR	61264h	**DISPLAY_CONTROLLER.IMAGE_ENHANCEMENT_BIN_DATA_REGISTER:** Writes to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index. Function 0 usage Threshold Count this Function is Read Only
MMADR	61268h	**DISPLAY_CONTROLLER.HISTOGRAM_THRESHOLD_GUARDBAND_REGISTER:**
MMADR	61400h	**DISPLAY_CONTROLLER.HDCP_CONFIG:** This register configures the HDCP mode.
MMADR	61404h	**DISPLAY_CONTROLLER.HDCP_INIT:** This register is used to inject entropy into the An calculation. Hardware holds 64 bits of initialization vector. The hardware destination for writes to this register alternates between the high 32 bits and the low 32 bits. When generating An hardware will use the two most recent values written to this register as a 64 bit source of entropy.
MMADR	61408h	**DISPLAY_CONTROLLER.HDCP_BKSV_LO:** This register holds part of the BKSV value.
MMADR	6140Ch	**DISPLAY_CONTROLLER.HDCP_BKSV_HI:** This register holds part of the BKSV value.
MMADR	61410h	**DISPLAY_CONTROLLER.HDCP_AN_LO:** This register holds part of the An value. Writeable with debug fuse enabled
MMADR	61414h	**DISPLAY_CONTROLLER.HDCP_AN_HI:** This register holds part of the An value. Writeable with debug fuse enabled
MMADR	61418h	**DISPLAY_CONTROLLER.HDCP_RI:** This register holds the receiver s RI value.
MMADR	6141Ch	**DISPLAY_CONTROLLER.HDCP_AKEY_LO:** This register holds part of the AKEY value.
MMADR	61420h	**DISPLAY_CONTROLLER.HDCP_AKEY_MED:** This register holds part of the Akey value.
MMADR	61424h	**DISPLAY_CONTROLLER.HDCP_AKEY_HI:** This register holds part of the AKEY value.
MMADR	6142Ch	**DISPLAY_CONTROLLER.HDCP_V_0:** These registers hold the V hash result from the receiver used for repeaters.
MMADR	61430h	**DISPLAY_CONTROLLER.HDCP_V_1:** These registers hold the V hash result from the receiver used for repeaters.

Base	Offset	Description
MMADR	61434h	**DISPLAY_CONTROLLER.HDCP_V_2:** These registers hold the V hash result from the receiver used for repeaters.
MMADR	61438h	**DISPLAY_CONTROLLER.HDCP_V_3:** These registers hold the V hash result from the receiver used for repeaters.
MMADR	6143Ch	**DISPLAY_CONTROLLER.HDCP_V_4:** These registers hold the V hash result from the receiver used for repeaters.
MMADR	61440h	**DISPLAY_CONTROLLER.HDCP_SHA1_IN:** This register provides the input for the SHA1 hash.
MMADR	61444h	**DISPLAY_CONTROLLER.HDCP_REP:** This register describes information needed for HDCP repeater support.
MMADR	61448h	**DISPLAY_CONTROLLER.HDCP_STATUS:** This register describes the HDCP status.
MMADR	6144Ch	**DISPLAY_CONTROLLER.HDCP_DBG_STAT:** This register reports HDCP status information for debugging. Debug fuse removes all access
MMADR	61450h	**DISPLAY_CONTROLLER.HDCP_AKSV_HI:** This is a clear on read register.
MMADR	61454h	**DISPLAY_CONTROLLER.HDCP_AKSV_LO:** This is a clear on read register
MMADR	62000h	**DISPLAY_CONTROLLER.AUD_CONFIG:** This register configures the audio output.
MMADR	62010h	**DISPLAY_CONTROLLER.AUD_DEBUG:**
MMADR	62020h	**DISPLAY_CONTROLLER.AUD_VID_DID:** These values are returned from the device as the Vendor ID Device ID response to a Get Root Node command. Previous default values 808629FBh DEVCL 80862801h DEVBLC
MMADR	62024h	**DISPLAY_CONTROLLER.AUD_RID:** These values are returned from the device as the Revision ID response to a Get Root Node command.
MMADR	62028h	**DISPLAY_CONTROLLER.AUD_ROOT_SUBN_CNT:** These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.
MMADR	62040h	**DISPLAY_CONTROLLER.AUD_FUNC_GRP:** These values are returned from the device as the Function Group Type response to a Get Audio Function Group command.
MMADR	62044h	**DISPLAY_CONTROLLER.AUD_FUNCGRP_SUBN_CNT:** These values are returned from the device as the Subordinate Node Count response to a Get Audio Function Group command.
MMADR	62048h	**DISPLAY_CONTROLLER.AUD_GRP_CAP:** These values are returned from the device as the Audio Function Group Capabilities response to a Get Audio Function Group command.
MMADR	6204Ch	**DISPLAY_CONTROLLER.AUD_PWRST:** These values are returned from the device as the Power State response to a Get Audio Function Group command.
MMADR	62050h	**DISPLAY_CONTROLLER.AUD_SUPPWR:** These values are returned from the device as the Supported Power States response to a Get Audio Function Group command.

Base	Offset	Description
MMADR	62054h	**DISPLAY_CONTROLLER.AUD_SID:** These values are returned from the device as the Subsystem ID response to a Get Audio Function Group command.
MMADR	62070h	**DISPLAY_CONTROLLER.AUD_OUT_CWCAP:** These values are returned from the device as the Audio Output Converter Widget Capabilities response to a Get Audio Output Converter Widget command. Previous default value 00000211h DevCL DevBLC
MMADR	62074h	**DISPLAY_CONTROLLER.AUD_OUT_PCMSIZE:** These values are returned from the device as the PCM Size and Rates response to a Get Audio Output Converter Widget command. Previous default value 001E0170h DevCL DevBLC
MMADR	62078h	**DISPLAY_CONTROLLER.AUD_OUT_STR:** These values are returned from the device as the Stream Formats response to a Get Audio Output Converter Widget command.
MMADR	6207Ch	**DISPLAY_CONTROLLER.AUD_OUT_DIG_CNVT:** These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.
MMADR	62080h	**DISPLAY_CONTROLLER.AUD_OUT_CH_STR:** These values are returned from the device as the Channel ID and Stream ID response to a Get Audio Output Converter Widget command.
MMADR	62084h	**DISPLAY_CONTROLLER.AUD_OUT_STR_DESC:** These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.
MMADR	620A0h	**DISPLAY_CONTROLLER.AUD_PINW_CAP:** These values are returned from the device as the Pin Complex Widget Capabilities response to a Get Pin Widget command.
MMADR	620A4h	**DISPLAY_CONTROLLER.AUD_PIN_CAP:** These values are returned from the device as the Pin Capabilities response to a Get Pin Widget command.
MMADR	620A8h	**DISPLAY_CONTROLLER.AUD_PINW_CONNLNG:** These values are returned from the device as the Connection List Length response to a Get Pin Widget command.
MMADR	620ACh	**DISPLAY_CONTROLLER.AUD_PINW_CONNLST:** These values are returned from the device as the Connection List Entry response to a Get Pin Widget command.
MMADR	620B0h	**DISPLAY_CONTROLLER.AUD_PINW_CNTR:** These values are returned from the device as the Pin Widget Control response to a Get Pin Widget command.
MMADR	620B4h	**DISPLAY_CONTROLLER.AUD_CNTL_ST:**
MMADR	620B8h	**DISPLAY_CONTROLLER.AUD_PINW_UNSOLRESP:** These values are returned from the device as the Unsolicited Response Enable response to a Get Pin Widget command.
MMADR	620BCh	**DISPLAY_CONTROLLER.AUD_PINW_CONFIG:** These values are returned from the device as the Config Default response to a Get Pin Widget command.
MMADR	620D4h	**DISPLAY_CONTROLLER.AUD_HDMIW_STATUS:**
MMADR	6210Ch	**DISPLAY_CONTROLLER.AUD_HDMIW_HDMIEDID:** These registers contain the HDMI data block from the EDID. The graphics driver reads

Base	Offset	Description
		the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA 861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command. Writing sequence Video software sets ELD invalid and sets the ELD access address to 0 or to the desired DWORD to be written. Video software writes ELD data 1 DWORD at a time. The ELD access address auto increments with each DWORD write wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time. Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. Reading sequence Video software sets the ELD access address to 0 or to the desired DWORD to be read. Video software reads ELD data 1 DWORD at a time. The ELD access address auto increments with each DWORD read wrapping around to address 0 when the max buffer address size of 0xF has been reached.
MMADR	62118h	**DISPLAY_CONTROLLER.AUD_HDMIW_INFOFR:** When the IF type or DWORD index is not valid the contents of the DIP will return all 0 s. These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index then fetch the indexed byte using the HDMI DIP get. Video driver read sequence for debug only Video software sets DIP type to the appropriate DIP and sets the DIP access address to the desired DWORD. Video software reads DIP data 1 DWORD at a time. The DIP access address auto increments with each DWORD write wrapping around to address 0 when the max buffer address size of 0xF has been reached.
MMADR	62120h	**DISPLAY_CONTROLLER.AUD_CONV_CHCNT:** HDMI converter Channel Mapping verb. Read only Reference HDMI SDVO EDS 0.79 Section 5.3.13 HDMI Channel to Converter Channel Mapping
MMADR	62128h	**DISPLAY_CONTROLLER.AUD_CTS_ENABLE:** These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.
MMADR	64100h	**DISPLAY_CONTROLLER.DP_B:** Description Display Port B control dprrega_b0.v ql_displayb1 Please note that DisplayPort B uses the same lanes as HDMIB. Therefore HDMIB and DisplayPort B cannot be enabled simultaneously. Calculation of TU is as follows For modes that divide into the link frequency evenly Active TU payload capacity. Please note that this is the same ratio as data m n Payload capacity dot CLK bytes per pixel LS_CLK of lanes
MMADR	64110h	**DISPLAY_CONTROLLER.DPB_AUX_CH_CTL:** Description AuxB control dprrega_b0.v auxb_ctl_rdback Programming note Do not change any fields while Busy bit 31 is asserted.
MMADR	64114h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA1:** Description AuxB Data1 dprrega_b0.v auxb_dpr_data1 ql_auxb_d1 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64118h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA2:** Description AuxB Data2 dprrega_b0.v auxb_dpr_data2 ql_auxb_d2 The read value will

Base	Offset	Description
		not be valid while Busy bit 31 is asserted.
MMADR	6411Ch	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA3:** Description AuxB Data3 dprrega_b0.v auxb_dpr_data3 ql_auxb_d3 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64120h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA4:** Description AuxB Data4 dprrega_b0.v auxb_dpr_data4 ql_auxb_d4 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64124h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA5:** Description AuxB Data5 dprrega_b0.v auxb_dpr_data5 ql_auxb_d5 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64130h	**DISPLAY_CONTROLLER.DP_AUX_CH_AKSV_HI:** Description AuxB AKSV High dprrega_b0.v DPR_AUX_AKSV_HI This is programmed with the lower 4 bytes of AKSV. DP_AUX_AKSV_LO should be programmed with the highest byte of AKSV. More than one AUX channel can select to use the AKSV buffer simultaneously. This will become the second DWORD of the message when AKSV buffer is selected. The first DWORD will come from the DP_AUX_CH_DATA1 register.
MMADR	64134h	**DISPLAY_CONTROLLER.DP_AUX_CH_AKSV_LO:** Description AuxB AKSV High dprrega_b0.V DPR_AUX_AKSV_LO This is programmed with the highest byte of AKSV. DP_AUX_AKSV_HI should be programmed with the lower 4 bytes of AKSV. More than one AUX channel can select to use the AKSV buffer simultaneously.
MMADR	64200h	**DISPLAY_CONTROLLER.DPC:** Description Display Port C control dprrega_b0.v ql_displayc1 Please note that DisplayPort C uses the same lanes as HDMIC. Therefore HDMIC and DisplayPort C cannot be enabled simultaneously.
MMADR	64210h	**DISPLAY_CONTROLLER.DPC_AUX_CH_CTL:** Description AuxC Data1 DPRREGA_B0.V AUXC_DPR_DATA1 QL_AUXC_D1 Programming note Do not change any fields while Busy bit 31 is asserted.
MMADR	64214h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA1:** Description AuxC Data1 dPRREGA_B0.V AUXC_DPR_DATA1 QL_AUXC_D1 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64218h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA2:** Description AuxC Data2 dprrega_b0.v auxc_dpr_data2 ql_auxc_d2 The read value will not be valid while Busy bit 31 is asserted.
MMADR	6421Ch	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA3:** Description AuxC Data3 dprrega_b0.v auxc_dpr_data3 ql_auxc_d3 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64220h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA4:** Description AuxC Data4 dprrega_b0.v auxc_dpr_data4 ql_auxc_d4 The read value will not be valid while Busy bit 31 is asserted.
MMADR	64224h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA5:** Description AuxC Data5 dprrega_b0.v auxc_dpr_data5 ql_auxc_d5 The read value will not be valid while Busy bit 31 is asserted.
MMADR	70000h	**DISPLAY_CONTROLLER.PIPEA_DSL:** This register enables the read back of the display pipe vertical line counter . The display line value is from the display pipe A timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation scan line zero is the first active line of the display. When in VGA centering mode the

Base	Offset	Description
		scan line 0 is the 1stactive scan line of the pseudo border not the centered active VGA image. In interlaced display timings the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Programming Note In order to cause the scan line logic to report the correct Line Counter value the corresponding Display Pipeline timing registers must be programmed to valid non zero e.g. 640x480 60Hz values before enabling the Pipe or programming VGA timing and enabling native VGA.
MMADR	70004h	**DISPLAY_CONTROLLER.PIPEA_SLC:** This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands or through MMIO for DevBLC and DevCTG . They can safely be accessed at any time. The Top and Bottom Line Count Compare registers are compared with the display line values from display A timing generator. The Top compare register operator is a less than or equal while the Bottom compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts status and command stream flow control wait for within range and wait for not within range . For range check the value programmed should be the desired value 1 so for line 0 the value programmed is VTOTAL and for line 1 the value programmed is 0.
MMADR	70008h	**DISPLAY_CONTROLLER.PIPEACONF:**
MMADR	70010h	**DISPLAY_CONTROLLER.PIPEAGCMAXRED:**
MMADR	70014h	**DISPLAY_CONTROLLER.PIPEAGCMAXGREEN:**
MMADR	70018h	**DISPLAY_CONTROLLER.PIPEAGCMAXBLUE:**
MMADR	70024h	**DISPLAY_CONTROLLER.PIPEASTAT:** This register is the second level of a two level interrupt and status scheme. A single bit in the first line interrupt status register represents the state of this register which is equal to the AND of a status bits with their corresponding enable bits OR ed together. First line interrupt status bits can cause interrupts or writes of the status register to cacheable memory. Bits in this register indicate the status of the display pipe A and can cause interrupt status bit changes in the first level interrupt and status register. Status bits in this register as sticky and once they are set will be cleared by writing a one to that bit. A write of a zero will not have an effect on the corresponding Interrupt status bit. The corresponding enable bits will determine if the interrupt status bit should be used in the first line interrupt status register. When an interrupt occurs the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt. Programming 1. Prior to clearing a Display Pipe sourced interrupt e.g. Display Pipe A VBLANK in the IIR the corresponding interrupt source status in the PIPEASTAT or PIPEBSTAT register e.g. Pipe A VBLANK Interrupt Status bit of PIPEASTAT must first be cleared. Note that clearing these status bits requires writing a 1 to the appropriate bit position.
MMADR	70030h	**DISPLAY_CONTROLLER.DSPARB:** Notes Each active display plane A B or C requires a FIFO to cover for memory latency. The FIFOs all come from a single RAM that is divided into areas for each display plane. The amount of the RAM used by each display plane is defined by this register. The two fields in the register split the display RAM into three portions allocated between display planes A B and C. This register is double buffered and updated on the leading edge of Vertical Blank of the pipe that the planes are assigned to. This register should only be

Base	Offset	Description
		changed when a single pipe is enabled or if all of the Display A B C planes are disabled. It takes effect on the next VBLANK for whichever pipe is currently active. Each display plane needs a minimum FIFO size that is at least MaxLatencyForPlane PixelRate PixelSize 512. All values should be rounded up to the next unit of 64B. Notes A special C3 mode can occur when a single display of Display A and Display B is active and the overlay and Display C are disabled. In that mode when C3 is entered the values in the BSTART and CSTART fields are ignored and the entire RAM is allocated to the single active display plane. Notes DevBW and DevBLC The control granularity of FIFO size is 64 bytes and the total size of the RAM is 384 16 bytes making TOTALSIZE equal to 96. The range of values for CSTART and BSTART is 0 95. Notes DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series The control granularity of FIFO size is 64 bytes and the total size of the RAM is 512 16 bytes making TOTALSIZE equal to 128. The range of values for CSTART and BSTART is 0 127. Notes DevBLC and DevCTG The entire register is reserved. Hardware controls the FIFO sizing automatically. Notes DevIntel Atom Processor D2000 series and N2000 Series FIFO Sizes A 28 B 31 C 37Notes The display dot clock frequency or pixel rate must not exceed 90 of the core display clock. When a primary plane is enabled with 64bpp format and sprite is also enabled on the same pipe the dot clock frequency or pixel rate must be less than 80 of the core display clock.
MMADR	70034h	**DISPLAY_CONTROLLER.FW1:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.
MMADR	70038h	**DISPLAY_CONTROLLER.FW2:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.
MMADR	7003Ch	**DISPLAY_CONTROLLER.FW3:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.
MMADR	70040h	**DISPLAY_CONTROLLER.PIPEAFRAMEHIGH:** Requires that this pipe s PLL is running
MMADR	70044h	**DISPLAY_CONTROLLER.PIPEAFRAMEPIXEL:** Requires that this pipe s PLL be running
MMADR	70050h	**DISPLAY_CONTROLLER.PIPEAGMCHDATAM:**
MMADR	70054h	**DISPLAY_CONTROLLER.PIPEAGMCHDATAN:**
MMADR	70060h	**DISPLAY_CONTROLLER.PIPEADPLINKM:**
MMADR	70064h	**DISPLAY_CONTROLLER.PIPEADPLINKN:**
MMADR	70070h	**DISPLAY_CONTROLLER.FW4:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level. For each FIFO there are two watermarks wmark1 and wmark. When FIFO status is above wmark1 hardware generates a status of 0. When FIFO status is between wmark1 and wmark it generates a status of 2. When FIFO status is below wmark it generates a status of 3. The FIFO status is indicated by the blue color.

Base	Offset	Description
		When the FIFO is full its FIFO status is 0. The two wmark levels are shown below
MMADR	70074h	**DISPLAY_CONTROLLER.FW5:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.
MMADR	70078h	**DISPLAY_CONTROLLER.FW6:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.
MMADR	70080h	**DISPLAY_CONTROLLER.CURACNTR:** This register and all other cursor registers will remain in their holding register readable after a write. The holding registers are transferred into the active registers on the asserting edge of Vertical Blank only after a write cycle to the base address register has completed. DevBLC and DevCTG For hires modes Cursor A is connected to pipe A only. For VGA popup it follows the VGA pipe select.
MMADR	70084h	**DISPLAY_CONTROLLER.CURABASE:** This register specifies the graphics memory address at which the cursor image data is located. Writes to this register acts like a trigger that enables atomic updates of the cursor registers. When updating the cursor registers this register should be written last in the sequence. This register should be written even if the actual contents did not change to allow the holding registers to move to the active registers on the next VBLANK. For legacy cursor modes this register is sufficient to specify the address of the entire cursor. For ARGB modes this register specifies the address of the first page of the cursor data.
MMADR	70088h	**DISPLAY_CONTROLLER.CURAPOS:** This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically requires that the base address be written and is double buffered.
MMADR	7008Ch	**DISPLAY_CONTROLLER.CURARESV:**
MMADR	70090h	**DISPLAY_CONTROLLER.CURAPALET:** These palette registers can be accessed through this MMIO interface register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. The two bit index selects one of the four colors or two of the colors when in the AND XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two bit index selects one of the four colors or two of the colors when in the AND XOR cursor mode.
MMADR	700C0h	**DISPLAY_CONTROLLER.CURBCNTR:** The hardware cursor registers are memory mapped and accessible through 32 bit 16 bit or 8 bit accesses. They are all including the palette registers double buffered. Writes to cursor registers are done to a holding register. The actual register update will occur based on the assigned pipes VBLANK. It is recommended that the base register be accessed through a 32 bit write only. To update all cursor registers atomically a sequence that ends with a base address register write should be used. DevBLC and DevCTG Cursor B is connected to pipe B only.

Base	Offset	Description
MMADR	700C4h	**DISPLAY_CONTROLLER.CURBBASE:** This register specifies the memory address at which the cursor data is located. Writes to this register should be done with 32 bit accesses and acts as a trigger to atomically update the cursor register set. For legacy cursor modes this register is sufficient to specify the address of the entire cursor. The address is the graphics address. For ARGB modes this register specifies the address of the first page of the cursor data.
MMADR	700C8h	**DISPLAY_CONTROLLER.CURBPOS:** This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically and is double buffered. The load register is transferred into the active register on the leading edge of Vertical Blank of the pipe cursor is currently assigned after the trigger has been set.
MMADR	700CCh	**DISPLAY_CONTROLLER.CURBRESV:**
MMADR	700D0h	**DISPLAY_CONTROLLER.CURB_PALET:** These palette registers can be accessed through this MMIO interface or through a legacy mode using the VGA palette register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. In the two bit AND XOR cursor modes the two bit index selects one of the four colors or two of the colors when in the mode. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
MMADR	7017Ch	**DISPLAY_CONTROLLER.DSPAADDR:**
MMADR	70180h	**DISPLAY_CONTROLLER.DSPACNTR:** Notes The active set of registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls. If the currently selected pipe is disabled the update is immediate.
MMADR	70184h	**DISPLAY_CONTROLLER.DSPALINOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
MMADR	70188h	**DISPLAY_CONTROLLER.DSPASTRIDE:**
MMADR	70194h	**DISPLAY_CONTROLLER.DSPAKEYVAL:** This register specifies the key color to be used with the mask bits to determine if the display source data matches the key. This register will only have an effect when the display color key is enabled. The overlay destination key value is used for overlay keying when Display A is being used as a primary display with overlay destination keying enabled. This key can be used as a Display C destination key onto Display A.
MMADR	70198h	**DISPLAY_CONTROLLER.DSPAKEYMSK:** This register specifies the

Base	Offset	Description
		key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.
MMADR	7019Ch	**DISPLAY_CONTROLLER.DSPASURF:**
MMADR	701A4h	**DISPLAY_CONTROLLER.DSPATILEOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPALINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VBLANK only. A change to this register will take effect on the next vblank following the write.
MMADR	701ACh	**DISPLAY_CONTROLLER.DSPASURFLIVE:**
MMADR	70400h	**DISPLAY_CONTROLLER.CBR1:**
MMADR	70404h	**DISPLAY_CONTROLLER.CBR2:**
MMADR	70408h	**DISPLAY_CONTROLLER.CCBR:**
MMADR	7040Ch	**DISPLAY_CONTROLLER.CBR3:**
MMADR	71000h	**DISPLAY_CONTROLLER.PIPEB_DSLDISPLAY_SCAN_LINE:** This register enables the read back of the display pipe vertical line counter . The display line value is from the display pipe B timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation scan line zero is the first active line of the display. When in VGA centering mode the scan line 0 is the 1stactive scan line of the pseudo border not the centered active VGA image display area. In interlaced display timings the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Programming Note In order to cause the scan line logic to report the correct Line Counter value the corresponding Display Pipeline timing registers must be programmed to valid non zero e.g. 640x480 60Hz values before enabling the Pipe or programming VGA timing and enabling native VGA.
MMADR	71004h	**DISPLAY_CONTROLLER.PIPEB_SLC:** The Start and End Line Count Compare registers are compared with the display line values from the timing generator. They change at the leading edge of HSYNC. They can safely be accessed at any time. The End compare register operator is a less than or equal while the Start compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts status and command stream flow control wait for within range and wait for not within range . For range check the value programmed should be the desired value 1. So for line 0 the value programmed is VTOTAL and for line 1 the value programmed is 0. This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands or through MMIO for DevBLC and DevCTG.

Base	Offset	Description
MMADR	71008h	**DISPLAY_CONTROLLER.PIPEBCONF:**
MMADR	71010h	**DISPLAY_CONTROLLER.PIPEBGCMAXRED:**
MMADR	71014h	**DISPLAY_CONTROLLER.PIPEBGCMAXGREEN:**
MMADR	71018h	**DISPLAY_CONTROLLER.PIPEBGCMAXBLUE:**
MMADR	71024h	**DISPLAY_CONTROLLER.PIPEBSTAT:** Programming Prior to clearing a Display Pipe sourced interrupt e.g. Display Pipe A VBLANK in the IIR the corresponding interrupt source status in the PIPEASTAT or PIPEBSTAT register e.g. Pipe A VBLANK Interrupt Status bit of PIPEASTAT must first be cleared. Note that clearing these status bits requires writing a 1 to the appropriate bit position.
MMADR	71040h	**DISPLAY_CONTROLLER.PIPEBFRAMEHIGH:**
MMADR	71044h	**DISPLAY_CONTROLLER.PIPEBFRAMEPIXEL:**
MMADR	71050h	**DISPLAY_CONTROLLER.PIPEBGMCHDATAM:**
MMADR	71054h	**DISPLAY_CONTROLLER.PIPEBGMCHDATAN:**
MMADR	71060h	**DISPLAY_CONTROLLER.PIPEBDPLINKM:**
MMADR	71064h	**DISPLAY_CONTROLLER.PIPEBDPLINKN:**
MMADR	7117Ch	**DISPLAY_CONTROLLER.DSPBADDR:**
MMADR	71180h	**DISPLAY_CONTROLLER.DSPBCNTR:** The active set of registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls. If the currently selected pipe is disabled the update is immediate.
MMADR	71184h	**DISPLAY_CONTROLLER.DSPBLINOFFSET:** This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
MMADR	71188h	**DISPLAY_CONTROLLER.DSPBSTRIDE:**
MMADR	71194h	**DISPLAY_CONTROLLER.DSPBKEYVAL:** This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The overlay destination key value is used for overlay keying when Display B is being used as a secondary display with overlay destination keying enabled.
MMADR	71198h	**DISPLAY_CONTROLLER.DSPBKEYMSK:** This register specifies the key mask to be used with the color value bits to determine if the sprite source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.
MMADR	7119Ch	**DISPLAY_CONTROLLER.DSPBSURF:** Writing to this register triggers

Base	Offset	Description
		the display plane flip. When it is desired to change multiple display B registers this register should be written last as a write to this register will cause all new register values to take effect.
MMADR	711A4h	**DISPLAY_CONTROLLER.DSPBTILEOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VBLANK only. A change to this register will take effect on the next vblank following the write.
MMADR	711ACh	**DISPLAY_CONTROLLER.DSPBSURFLIVE:**
MMADR	71200h	**DISPLAY_CONTROLLER.DSPBFLPQSTAT:**
MMADR	71400h	**DISPLAY_CONTROLLER.VGACNTRL:** This register provides support for VGA compatibility modes. This register is used by video BIOS only.
MMADR	72180h	**DISPLAY_CONTROLLER.DSPCCNTR:** The active set of basic control registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls with the exception of the Display C color control registers. If the currently selected pipe is disabled the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.
MMADR	72184h	**DISPLAY_CONTROLLER.DSPCLINOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
MMADR	72188h	**DISPLAY_CONTROLLER.DSPCSTRIDE:**
MMADR	7218Ch	**DISPLAY_CONTROLLER.DSPCPOS:** These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display this should be set to the entire display rectangle.
MMADR	72190h	**DISPLAY_CONTROLLER.DSPCSIZE:** This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display

Base	Offset	Description
		rectangle that the sprite is assigned to.
MMADR	72194h	**DISPLAY_CONTROLLER.DSPCKEYMINVAL:** This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5 5 5 or 5 6 5 formats must be filled with duplicates of the three or two MSBs of the pixel value.
MMADR	72198h	**DISPLAY_CONTROLLER.DSPCKEYMSK:**
MMADR	7219Ch	**DISPLAY_CONTROLLER.DSPCSURF:** Writing to this register triggers the display plane flip. When it is desired to change multiple display C registers this register should be written last as a write to this register will cause all new register values to take effect.
MMADR	721A0h	**DISPLAY_CONTROLLER.DSPCKEYMAXVAL:** This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.
MMADR	721A4h	**DISPLAY_CONTROLLER.DSPCTILEOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
MMADR	721A8h	**DISPLAY_CONTROLLER.DSPCCONTALPHA:**
MMADR	721D0h	**DISPLAY_CONTROLLER.DCLRC0:**
MMADR	721D4h	**DISPLAY_CONTROLLER.DCLRC1:** The sum of the absolute value of SH_SIN and SH_COS must be limited to less than 8. ABS SH_SIN ABS SH_COS LT 8
MMADR	721E0h	**DISPLAY_CONTROLLER.GAMC5:** Same as previous register.
MMADR	721E4h	**DISPLAY_CONTROLLER.GAMC4:** Same as previous register.
MMADR	721E8h	**DISPLAY_CONTROLLER.GAMC3:** Same as previous register.
MMADR	721ECh	**DISPLAY_CONTROLLER.GAMC2:** Same as previous register.
MMADR	721F0h	**DISPLAY_CONTROLLER.GAMC1:** Same as previous register.
MMADR	721F4h	**DISPLAY_CONTROLLER.GAMC0:** These registers are used to determine the characteristics of the gamma correction for the display C pixel data pre blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color

Base	Offset	Description
		intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points 0 and 1023 have fixed values 0 and 1023 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise screen artifacts may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U

1.10 IOSF-SB (Msg Bus) Space

1.10.1 Intel Atom Processor D2000 series and N2000 Series IOSF-SB Bus Access

Intel Atom Processor D2000 series and N2000 Series GMCH contains a Message Network called IOSF Sideband (IOSF-SB, SB, or sideband) as an internal communication medium for simple, low bandwidth, sideband communication. Host software (BIOS) can access the message network via configuration registers in device 0 to access private (i.e. non host-mapped) registers and to initiate messages (for example, interrupts, or power management events).

Access to this network by the CPU is needed for only a handful of GMCH operations including:

- Configuring system DRAM and DMI
- Setting CPU POC and causing a CPU-Only reset
- GMCH Performance Monitoring (PMON).
- Thermal management setup.
- Display IO and PLL configuration.

Note: Some GMCH registers are ONLY accessible to software via this method.

1.10.2 Intel Atom Processor D2000 series and N2000 Series IOSF-SB Access mechanisms

Due to operating system security requirements, IA software drivers for GFX/Video/Display need to only address PCI device 2 configuration space (0/2/0) while “host” related software should only address PCI device 0 configuration space (0/0/0). For prior parts (LNC/PNW), all media related registers were visible through device 2 MMIO or directly in the PCI header. With CDV, the display IOs and PLLs are only accessible through IOSF-SB and not exposed in MMIO.

CDV’s generic mechanism for accessing IOSF-SB without exploding it into an ever changing MMIO mapping is to use a data/index register indirection similar to CONFIG_ADDRESS CONFIG_DATA used by IA code to access PCI config space. Within the host bridge configuration space, two registers provide a mailbox capability into the Message Network:

- **MCR (Message Control Register):** provides the message bus command fields. A write to this register issues a message on the Message Network with the fields specified by that write data. All byte enables must be enabled when writing this register.
- **MCRX (Message Control Register Extension:** Provides bits 31:8 of the address/offset for transactions that require it. Must be written before MCR. Returns to ‘0 after MCR is written.
- **MDR (Message Data Register):** provides the means to specify data to be written or retrieving data that was read during a message operation. For messages with a data payload, MDR must be written with the data to be sent prior to a write to MCR. For messages that return data, MDR contains the data read after the write to MCR completes.

These Registers are described in the table below:

<table>
<tr><th>Register Name</th><th>Description</th></tr>
<tr><td>MCR</td><td>Message Control Register. A write to this register issues a message on the GMCH internal message network with the fields specified by that write data. All byte enables must be enabled when writing this register. When the sideband packet register is written, the “Configuration Helper Unit” creates a transaction on the IOSF sideband channel, using the fields sent with the 0xD0 write operation, as described in the register below. Note that this register is a virtual configuration register that triggers an IOSF sideband command and cannot be counted on retain the values written to it. If the opcode for the transaction results in a data write semantic transaction, then the data for the transaction will be taken from the Sideband Data Register at offset D4h. If the opcode results in a data read semantic transaction, then the resulting data will be placed in the Sideband Data Register and may later be read by software.
<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:24</td><td>WO</td><td>xxh</td><td>Message Opcode: The sideband opcode to be used by the triggered transaction.</td></tr>
<tr><td>23:16</td><td>WO</td><td>xxh</td><td>Message Port: The sideband port to be targeted by the triggered transaction.</td></tr>
<tr><td>15:08</td><td>WO</td><td>xxh</td><td>Message Offset low: The sideband register offset to be targeted by the triggered transaction. Note that this field applies only to register read and write operations.</td></tr>
<tr><td>07:04</td><td>WO</td><td>xh</td><td>Message Byte Enables: The sideband byte enables to be used by the triggered transaction. Note that this field applies only to register read and write operations. Active high byte enables which enable each of the corresponding bytes in the MDR when high.</td></tr>
<tr><td>03:00</td><td>WO</td><td>0h</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>MDR</td><td>Message Data Register. Provides the means to specify data to be written or retrieving data that was read due to a message operation. For messages with a data payload, MDR must be written with the data to be sent prior to a write to MCR. For messages that return data, MDR contains the data read after the write to MCR completes.
<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:00</td><td>RW</td><td>00000000h</td><td>Message Data : Sideband data register, used as the place to store the data, when the operation triggered by an MCR write is a “read” semantic, or the place to get the data if the MCR-triggered operation is a “write” semantic.</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Register Name</th><th>Description</th></tr>
<tr><td>MCRX</td><td>
Message Control Register Extension. The MCR lacks the upper address or offset bits necessary to create some necessary transactions over IOSF sideband (units that needs more than 8bits of offset). This register is the home for those extensions. Its contents are used to fill in the upper address or offset bits of an IOSF sideband request and are cleared upon a write to the MCR.
<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:08</td><td>RW</td><td>000000h</td><td>Message Offset High: Bits 31:8 of the address/offset for a transaction to be created when a write to configuration register 0xD0 is executed. Bits 7:0 still come from the MCR register. The contents of this register field are cleared at the conclusion of a configuration write to MCR (which means this register must be written first for transactions with more than 8 bits of offset)..</td></tr>
<tr><td>07:00</td><td>RW</td><td>00h</td><td>Reserved</td></tr>
</table>
</td></tr>
</table>

NOTE: There is no guarantee of atomicity (locking of the message bus) or latency.

There are two sets of these registers. One for PCI 0/0/0 and one for PCI 0/2/0. Both behave the same, but the 0/2/0 is reserved for use by the GFX/media driver.

- PCI 0/0/0

PCI B0:D0:F0 Header Start	PCI B0:D0:F0 Header End	Register Name
D0h	D3h	MCR
D4h	D7h	MDR
D8h	DBh	MCRX

- PCI 0/2/0

PCI B0:D2:F0 Header Start	PCI B0:D2:F0 Header End	Register Name
A0h	A3h	MCR
A4h	A7h	MDR
A8h	ABh	MCRX

1.10.3 Intel Atom Processor D2000 series and N2000 Series IOSF-SB Port Assignments

Interface	Routing Number	Register Read/Write Opcodes	Description
AM/MA	00h	10h/11h	IOSF primary channel router.
BM/MB	03h	10h/11h	DRAM buffering and arbitration unit.
CM/MC	08h	10h/11h	Configuration helper unit.
HM/MH	02h	10h/11h	Processor interface.
DM/MD	01h	10h/11h	DRAM controller.
GM/MG	06h, 07h	10h/11h	GFX/VED/Media configuration.
PM/MP	04h	10h/11h	Power Management Controller (PMU)
ZM/MZ	05h	10h/11h	Debug controller.
FM/MF	81h	10h/11h	Fuse unit.
YM/MY	10-80h	10h/11h	DMI Controller.
IM/MI	88h	00h/01h	Display IO and PLLs
WM/MW	09h	00h/01h	DMI IO
RM/MR	87h	06h/07h	DDR IO
EM/ME	8Ah	10h/11h	DDR Training Unit (REUT)
JM/MJ	89h	10h/11h	GPIO
VM/MV	8Bh	10h/11h	PMU Controller (VDMs to/from “IOSF Primary Channel Router” for ICH)

1.10.4 Msg Bus Register Space

Port	Reg/Mem	Description
00h	0h/	**AEC:** AEC Enhanced Configuration Space ; The Lincroft SCH supports PCI Express enhanced configuration space, which is mapped into PCI memory space at a 256 Mbyte offset given by the upper four bits of the AEC register
00h	10h/	**AMIRRORCTL:** AH Mirroring Control ; The “IOSF primary channel router” is able to mirror operations that it sends towards the “Processor interface” into concurrent operations sent towards the “DRAM buffering and arbitration unit” in order to facilitate CPU only PSMI. These mirrored packets, when enabled, are sent to a rotating 1MB region in DRAM space that is configured by this register. This register is used only for PSMI mode, so in typical operation it would be set to 0000_0000h.
00h	1h/	**ACF8DATA:** CF8 Data Register. This can be written due to CF8 transaction or msg bus.

Port	Reg / Mem	Description
00h	20h/	**ASTATUS:** “IOSF primary channel router” Status Control ;The “IOSF primary channel router” may indicate the urgency of the transactions that it has offered or will offer to the “DRAM buffering and arbitration unit” through two-wire status ports that are associated with the RequestABx ports. During normal operation, requests on the RequestAB1 port are treated as ?very low-priority?, since they will simply be buffered in the Intel HD Audio unit. However, if the transactions are not serviced within a reasonable period of time, the Intel HD Audio unit will experience errors. As a result, the “IOSF primary channel router” has the ability to raise the priority of these transactions to ?urgent? after a specified amount of time has elapsed. A similar mechanism exists for non-Intel HD Audio SCL transactions, except that the priorities fluctuate between ?fairly low-priority? and ?normal priority?. The time constants used to control the modulation are given in this register, along with a mechanism to hardwire the priorities, in case of error.
00h	30h/	**APEERBASE:** specifies the base of the memory region inside of which the “IOSF primary channel router” routes upstream peer-to-peer writes back downstream. When the “IOSF primary channel router” detects an upstream posted write operation that is not targeted towards the iFSB MSI region, it checks whether the access lies between this base register and the value contained in the Peer Limit Register. If the address lies between (inclusive), then the write operation is directed back downstream and enters a normal target decode process. If the address lies outside the region specified by the registers, then the access is routed towards DRAM.
00h	31h/	**APEERLIMIT:** specifies the top of the memory region inside of which the “IOSF primary channel router” routes upstream peer-to-peer writes back downstream. When the “IOSF primary channel router” detects an upstream posted write operation that is not targeted towards the iFSB MSI region, it checks whether the access lies between the base register and the value contained in this register. If the address lies between (inclusive), then the write operation is directed back downstream and enters a normal target decode process. If the address lies outside the region specified by the registers, then the access is routed towards DRAM
00h	32h/	**AVIB:** VDM Balloon Blocking Control
00h	33h/	**AVQR:** VDM Balloon Tag Status
00h	40h/	**AHBALON:** VDM Balloon Tag Status
00h	f0h/	**MISR_A0:** Muxed B to Ax PRI control and address 128
00h	f1h/	**MISR_A1:** Muxed B to Ax PRI data 256
01h	00h/	**DRP:** DRAM Rank Population Register; This register identifies the type of memory populated on each of the two memory DIMMs and the enabling and disabling of certain Ranks in them. It should not be changed after the Initialization Complete bit is set in the DCO register.
01h	01h/	**DTR0:** DRAM Timing Register 0; This identifies the timing to be used to interface to the DRAM devices. This information is based on the specifications for the memory devices populated

Port	Reg/Mem	Description
		as well as the specifications driven by the system requirements. It should not be changed after the Initialization Complete bit is set in the DCO register.
01h	02h/	**DTR1:** DRAM Timing Register 1;This identifies the timing to be used to interface to the DRAM devices. This information is based on the specifications for the memory devices populated as well as the specifications driven by the system requirements. It should not be changed after the Initialization Complete bit is set in the DCO register.
01h	03h/	**DTR2:** DRAM Timing Register 2;This identifies the timing to be used to interface to the DRAM devices. This information is based on the specifications for the memory devices populated as well as the specifications driven by the system requirements. It should not be changed after the Initialization Complete bit is set in the DCO register.
01h	04h/	**DTR3:** DRAM Timing Register 3; This identifies the ODT related timing.
01h	06h/	**DPMC0:** DRAM Power Management Control Register 0
01h	07h/	**DPMC1:** DRAM Power Management Register 1
01h	08h/	**DRFC:** DRAM Refresh Control Register
01h	09h/	**DSCH:** DRAM Scheduler control Register
01h	0Ah/	**DCAL:** DRAM Calibration Control
01h	0Bh/	**DRMC:** DRAM Scheduler control Register
01h	0Ch/	**PMSTS:** Power Management Status
01h	0Fh/	**DCO:** DRAM Controller Operation Register
01h	10h/	**DTRC:** DRAM Training Control
01h	12h/	**DCBR:** DRAM engineering bits
01h	20h/	**DSTAT:** “DRAM controller” Status register
01h	21h/	**PGTBL:** DRAM Page Table
01h	31h/	**MISRCCCLR:** MISR clear CMD/CTRL Register
01h	32h/	**MISRDDCLR:** MISR clear DM/DQ Register
01h	34h/	**MISRCCSIG:** MISR Signature CMD/CTRL Register
01h	35h/	**MISRDDSIG:** MISR Signature DM/DQ Register 0
01h	4Ah/	**SSKPD0:** BIOS/GFX Scratchpad
01h	4Bh/	**SSKPD1:** BIOS/GFX Scratchpad
01h	50h/	**BONUS0:**
01h	51h/	**BONUS1:**
01h	80h/	**SCR00:** Scrambler Pattern
01h	81h/	**SCR01:** Scrambler Pattern
01h	82h/	**SCR02:** Scrambler Pattern

Port	Reg / Mem	Description
01h	83h/	**SCR03:** Scrambler Pattern
01h	84h/	**SCR04:** Scrambler Pattern
01h	85h/	**SCR05:** Scrambler Pattern
01h	86h/	**SCR06:** Scrambler Pattern
01h	87h/	**SCR07:** Scrambler Pattern
01h	88h/	**SCR08:** Scrambler Pattern
01h	89h/	**SCR09:** Scrambler Pattern
01h	8Ah/	**SCR10:** Scrambler Pattern
01h	8Bh/	**SCR11:** Scrambler Pattern
01h	8Ch/	**SCR12:** Scrambler Pattern
01h	8Dh/	**SCR13:** Scrambler Pattern
01h	8Eh/	**SCR14:** Scrambler Pattern
01h	8Fh/	**SCR15:** Scrambler Pattern
01h	E0h/	**PMSEL0:** Performance Monitor Event Select Register 0
01h	E1h/	**PMSEL1:** Performance Monitor Event Select Register 1
01h	E2h/	**PMSEL2:** Performance Monitor Event Select Register 2
01h	E3h/	**PMSEL3:** Performance Monitor Event Select Register 3
01h	E8h/	**PMAUXMAX:** Performance Monitor AUX Max Register
01h	E9h/	**PMAUXMIN:** Performance Monitor AUX Min Register
01h	EAh/	**PMAUXSEL:** Performance Monitor AUX Select Register
02h	0h/	**HMISC1:** Host Power-On Configuration Miscellaneous Settings Controls : cfgreg32_00
02h	1h/	**HPOC:** Host Power-On Configuration Settings : cfgreg32_01
02h	20h/	**HSNPCNTR:** Host Snoop Counter : cfgreg32_20
02h	30h/	**HCLKOVERRIDECNTR:** Host CLOCK override Counter : cfgreg32_30
02h	3h/	**HMISC2:** Host Miscellaneous Controls : cfgreg32_03
02h	4h/	**HSMMCTL:** Host System Management Mode Controls : cfgreg32_04
02h	5h/	**HMASTERCNTR0:** Host Master Threshold Limit 0 : cfgreg32_05
02h	6h/	**HMASTERCNTR1:** Host Master Threshold Limit 1 : cfgreg32_06
02h	7h/	**HSCYC_:** Host Special Cycle Filter : cfgreg32_07
02h	8h/	**HMBOUND:** Host Memory/IO Boundary Register : cfgreg32_08
02h	9h/	**HECREG:** HECREG - Extended Configuration Space Config : cfgreg32_09

Port	Reg/Mem	Description
02h	Ah/	**HPINCR:** Host Special Cycle FilterPin Control Register : cfgreg32_0A
02h	Bh/	**HRSTR_CLKOVR:** Host Snoop CounterOverride VBCLK : cfgreg32_0B
02h	Eh/	**HRSTR_BRPIFAIRNESS:** BPRI fairness counter configuration : cfgreg32_0C
02h	Fh/	**HMBOUNDHI:** Host Memory/IO High Boundary : cfgreg32_0F
02h	f0h/	**MISR_H0:** FSB upstream data 245
02h	f1h/	**MISR_H1:** FSB upstream address 32
02h	f2h/	**MISR_H2:** FSB upstream ctrl 64
03h	01h/	**BCTRL:** “DRAM buffering and arbitration unit” basic Control information used by the “DRAM buffering and arbitration unit”. Note that the “DRAM buffering and arbitration unit” is by default not configured for power management.
03h	02h/	**BWFLUSH:** “DRAM buffering and arbitration unit” Write Flush Policy ;The BWFLUSH register controls the policy used to determine when dirty entries must be flushed to DRAM. When the number of dirty entries retained by the “DRAM buffering and arbitration unit” is lower than the low water mark, no flushes will be performed. When the number of dirty entries is between the two values, the “DRAM controller” will opportunistically flush data to DRAM. When the number of dirty entries exceeds the high water mark, the “DRAM buffering and arbitration unit” will initiate a high-priority flush and push dirty data to DRAM until the count is once again below the low water mark.
03h	03h/	**BBANKMASK:** “DRAM buffering and arbitration unit” Write Flush Bank Mask; The BBANKMASK register is used by the address-aware flushing mechanism to determine the bit location of the bank bits within a 36 bit addresses. Bits 23:0 of this register are mapped to bits 35:12 of the addresses in the “DRAM buffering and arbitration unit” tag store. ; The operating value for this register is heavily dependent upon the DDR configuration.
03h	04h/	**BBROWMASK:** “DRAM buffering and arbitration unit” Write Flush Bank Mask; The BBANKMASK register is used by the address-aware flushing mechanism to determine the bit location of the bank bits within a 36 bit addresses. Bits 23:0 of this register are mapped to bits 35:12 of the addresses in the “DRAM buffering and arbitration unit” tag store. ; The operating value for this register is heavily dependent upon the DDR configuration.
03h	05h/	**BRANKMASK:** “DRAM buffering and arbitration unit” Write Flush Bank Mask; The BBANKMASK register is used by the address-aware flushing mechanism to determine the bit location of the bank bits within a 36 bit addresses. Bits 23:0 of this register are mapped to bits 35:12 of the addresses in the “DRAM buffering and arbitration unit” tag store. ; The operating value for this register is heavily dependent upon the DDR configuration.

Port	Reg / Mem	Description
03h	18h/	**BIMRDATA:** “DRAM buffering and arbitration unit” Isolated Memory Region Data Value. controls the data returned to agents that violate the IMR rules
03h	19h/	**BIMRVCTL:** “DRAM buffering and arbitration unit” Write Flush Bank Mask; The BBANKMASK register is used by the address-aware flushing mechanism to determine the bit location of the bank bits within a 36 bit addresses. Bits 23:0 of this register are mapped to bits 35:12 of the addresses in the “DRAM buffering and arbitration unit” tag store. ; The operating value for this register is heavily dependent upon the DDR configuration. This register will is ANDED with an internal constant
03h	1Eh/	**BNOCACHEL:** “DRAM buffering and arbitration unit” Non-Cached Region ;This register defines a region of memory that, when DMA devices behind the A-unit or G-unit perform an access (whether snooped or not), will not cause a FSB snoop.
03h	1Fh/	**BNOCACHEH:** “DRAM buffering and arbitration unit” Non-Cached Region ;This register defines a region of memory that, when DMA devices behind the A-unit or G-unit perform an access (whether snooped or not), will not cause a FSB snoop.
03h	20h/	**BTHCTRL:** “DRAM buffering and arbitration unit” Throttling Control ;This register defines the range of addresses that will eventually be serviced by the DRAM controllers first rank (Rank0) and therefore subtractively which addresses will be serviced by the DRAM controllers second rank (Rank1).
03h	21h/	**BTHMASK:** “DRAM buffering and arbitration unit” Throttling Masks ;The BTHMASK register contains the fields that control “DRAM buffering and arbitration unit” throttling of transactions to DRAM.
03h	30h/	**DEBUG0:** “DRAM buffering and arbitration unit” This register contains an assortment of bits that enable debug features Chicken Bits and other misc control bits.
03h	31h/	**LNC_BCHICKENBITSDEBUG1:** “DRAM buffering and arbitration unit” This register contains more bits that enable debug Chicken Bits and other misc control bits. Added in LNC only
03h	38h/	**VC3LOCK:** This register enables VC3 traffic to access the IMR region it describes. Once this register is programmed, VC3 traffic is the only agent that can access the IMR region and all VC3 traffic that falls outside the region is automatically discarded.
03h	40h/	**IMR0L:** This register, along with IMR0H, IMR0RM, and IMR0WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR0W and IMR0R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR0L, IMR0H, IMR0R, and IMR0W is located in this register.

Port	Reg/Mem	Description
03h	41h/	**IMR0H:** This register, along with IMR0L, IMR0R, and IMR0W, defines an isolated region of memory that can be masked to prohibit certain "DRAM buffering and arbitration unit" agents from accessing memory
03h	42h/	**IMR0RM:** This register, along with IMR0L, IMR0R, and IMR0W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	43h/	**IMR0WM:** This register, along with IMR0L, IMR0R, and IMR0W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	44h/	**IMR1L:** This register, along with IMR1H, IMR1RM, and IMR1WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR1W and IMR1R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR1L, IMR1H, IMR1R, and IMR1W is located in this register.
03h	45h/	**IMR1H:** This register, along with IMR1L, IMR1R, and IMR1W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	46h/	**IMR1RM:** This register, along with IMR1L, IMR1R, and IMR1W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	47h/	**IMR1WM:** This register, along with IMR1L, IMR1R, and IMR1W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	48h/	**IMR2L:** This register, along with IMR2H, IMR2RM, and IMR2WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR2W and IMR2R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR2L, IMR2H, IMR2R, and IMR2W is located in this register.
03h	49h/	**IMR2H:** This register, along with IMR2L, IMR2R, and IMR2W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	4ah/	**IMR2RM:** This register, along with IMR2L, IMR2R, and IMR2W, defines an isolated region of memory that can be masked to

Port	Reg / Mem	Description
		prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	4bh/	**IMR2WM:** This register, along with IMR2L, IMR2R, and IMR2W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	4ch/	**IMR3L:** This register, along with IMR3H, IMR3RM, and IMR3WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR3W and IMR3R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR3L, IMR3H, IMR3R, and IMR3W is located in this register.
03h	4dh/	**IMR3H:** This register, along with IMR3L, IMR3R, and IMR3W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	4eh/	**IMR3RM:** This register, along with IMR3L, IMR3R, and IMR3W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	4fh/	**IMR3WM:** This register, along with IMR3L, IMR3R, and IMR3W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	50h/	**IMR4L:** This register, along with IMR4H, IMR4RM, and IMR4WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR4W and IMR4R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR4L, IMR4H, IMR4R, and IMR4W is located in this register.
03h	51h/	**IMR4H:** This register, along with IMR4L, IMR4R, and IMR4W, defines an isolated region of memory that can be masked to prohibit certain "DRAM buffering and arbitration unit" agents from accessing memory
03h	52h/	**IMR4RM:** This register, along with IMR4L, IMR4R, and IMR4W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	53h/	**IMR4WM:** This register, along with IMR4L, IMR4R, and IMR4W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory

Port	Reg/Mem	Description
03h	54h/	**IMR5L:** This register, along with IMR5H, IMR5RM, and IMR5WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR5W and IMR5R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR5L, IMR5H, IMR5R, and IMR5W is located in this register.
03h	55h/	**IMR5H:** This register, along with IMR5L, IMR5R, and IMR5W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	56h/	**IMR5RM:** This register, along with IMR5L, IMR5R, and IMR5W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	57h/	**IMR5WM:** This register, along with IMR5L, IMR5R, and IMR5W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	58h/	**IMR6L:** This register, along with IMR6H, IMR6RM, and IMR6WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as configured by the IMR6W and IMR6R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR6L, IMR6H, IMR6R, and IMR6W is located in this register.
03h	59h/	**IMR6H:** This register, along with IMR6L, IMR6R, and IMR6W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	5ah/	**IMR6RM:** This register, along with IMR6L, IMR6R, and IMR6W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	5bh/	**IMR6WM:** This register, along with IMR6L, IMR6R, and IMR6W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	5ch/	**IMR7L:** This register, along with IMR7H, IMR7RM, and IMR7WM, defines an isolated region of memory that can be masked to prohibit certain system agents from accessing memory. When a device behind a masked port performs an access (whether snooped or not), an IMR may optionally prevent that transaction from changing the state of memory or from getting correct data in response to the operation, as

Port	Reg / Mem	Description
		configured by the IMR7W and IMR7R registers, respectively. Write data will be dropped, and reads will return data from the IMRData register. Note that the bit that locks IMR7L, IMR7H, IMR7R, and IMR7W is located in this register.
03h	5dh/	**IMR7H:** This register, along with IMR7L, IMR7R, and IMR7W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	5eh/	**IMR7RM:** This register, along with IMR7L, IMR7R, and IMR7W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	5fh/	**IMR7WM:** This register, along with IMR7L, IMR7R, and IMR7W, defines an isolated region of memory that can be masked to prohibit certain “DRAM buffering and arbitration unit” agents from accessing memory
03h	60h/	**BARBCTRL0:** “DRAM buffering and arbitration unit” Incoming Arbiter Control0 ;BarbCtrl 0 and 1 regulate the admission of requests into the “DRAM buffering and arbitration unit” from the nine client streams. Its policy is expressed as a collection of timeslices, one per incoming request stream.
03h	61h/	**BARBCTRL1:** “DRAM buffering and arbitration unit” Incoming Arbiter Control1 ;BarbCtrl 1 is a continuation of the functionality of BarbCtrl0.
03h	E0h/	**BEMON0:** EMON Control register for counter 0
03h	E1h/	**BEMON1:** EMON Control register for counter 1
03h	E2h/	**BEMON2:** EMON Control register for counter 2
03h	E3h/	**BEMON3:** EMON Control register for counter 3
03h	f0h/	**MISR_B0:** B to GFx PRI data 256
03h	f1h/	**MISR_B1:** Gfx to B - PRI control and address 128
03h	f2h/	**MISR_B2:** B to Ved PRI DATA 256
03h	f3h/	**MISR_B3:** Ved to B - PRI control and address 128
04h	50h/	**SVID_CONFIG:** This register contains the SVID controller configuration
04h	51h/	**SVID_PP_CONFIG:** This register have the VR address and enable for VCC VNN and AUX
04h	52h/	**SVID_COMMAND:** This register is used for the PCODE/SVID interface. an SVID transaction frame is build out of it
04h	53h/	**SVID_STATUS:** This register contains the 3x8-bit Status of supported VRs (VR0, VR1 and VR_Aux) + Error indication.
04h	54h/	**SVID_DATA_IN:** This register contains the data read from VR by GetReg command
04h	55h/	**SVID_VCC_RAIL_CONFIG:** This register controls VCC rail VID commands
04h	56h/	**VID_FUSES:** This register contains VID VNN fuses and process

Port	Reg/Mem	Description
		fuse
04h	58h/	**GV_CTRL:** This register contains SOC Enhanced Intel SpeedStep® Technology setting for DSP/VED/GFX
04h	59h/	**GV_STATUS:** This register contains SOC Enhanced Intel SpeedStep Technology status for DSP/VED/GFX
04h	5Ah/	**CLOCKS_SKU_OVERRIDE:** This register controls CCK clocks SKU override
04h	5Eh/	**RFU0:** This register is Reserved for future use
04h	5Fh/	**RFU1:** This register is Reserved for future use
04h	60h/	**PWRGT_CNT:** Active Power Gate Control Register; This register indicates the configuration of the voltage islands for the various blocks that the “Power Management Controller (PMU)” controls. This register is updated by the software driver to request power up/power down of the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island. Each island is controlled by a 2-bit field. The upper bit (bit 1) is used by software to request power up, and the lower bit (bit 0) is used by software to request power down. At reset/power up, all the Islands comes up enabled (00) indicating that software is not requesting power up/down.. The register fields are set by software via the Message Bus interface. Hardware clears the bits when the request is serviced.
04h	61h/	**PWRGT_STS:** Power Gate Status; This register indicates the status of the voltage islands for the various blocks that the “Power Management Controller (PMU)” controls. This register is updated by hardware. 2 bits are used to indicate power up/power down status of each the islands: viz. the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island as shown in the table below. At reset/power up, all the Islands comes up enabled (D0).
04h	62h/	**PWRGT_IE:** Power Gate Interrupt Enable; This register indicates the interrupt enables for the power islands for the various blocks that the “Power Management Controller (PMU)” controls. The software driver sets this bit to trigger an interrupt when the particular island is brought back to D0. There is one bit for each of the islands: viz. the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island as shown in the table below. . At reset/power up, all IE comes up as 0, indicating interrupts are not enabled
04h	63h/	**TAP_PGON_OVR:** TAP power gate ON overrides: Info file testing should exclude this register
04h	64h/	**TAP_PGOFF_OVR:** TAP power gate OFF overrides : Info file testing should exclude this register
04h	65h/	**TAP_CLKEN_ON_OVR:** TAP clken ON overrides: Info file testing should exclude this register
04h	66h/	**TAP_CLKEN_OFF_OVR:** TAP clken OFF overrides
04h	67h/	**TAP_FWON_OVR:** TAP firewall ON overrides

Port	Reg / Mem	Description
04h	68h/	**TAP_FWOFF_OVR:** TAP firewall OFF overrides
04h	69h/	**TAP_RST_ON_OVR:** TAP reset ON overrides
04h	6Ah/	**TAP_RST_OFF_OVR:** TAP reset OFF overrides
04h	6Bh/	**PWRGT_EN_OUT:** power gate enables outputs from all VNN switched units
04h	6Ch/	**PWRGT_RF_EN_OUT:** power gate enables outputs from all RF VNN switched units, these are connected up only in netlist and the read value in RTL will be X
04h	6Dh/	**STDBY_PWROFF:** Power Management I/O Base Address
04h	6Eh/	**STRAPS_REG:** Power Management I/O Base Address, reset values are not applicable
04h	6Fh/	**SC_BASEADDR_REG:** register for BIOS to write south complex address
04h	70h/	**PMBA:** Power Management I/O Base Address
04h	71h/	**PCR:** “Power Management Controller (PMU)” Control Register
04h	72h/	**OR1:** Option Register 1
04h	73h/	**OR2:** Option Register 2
04h	74h/	**WDTC:** 8051 Watchdog Timer Control Register; The watchdog timer is a 16-bit countdown timer that must internally be “pinged” by the 8051 to indicate it is still functional. It counts in 1µs granularity.
04h	75h/	**WDTV:** 8051 Watchdog Timer Value Register
04h	76h/	**OR3:** Option Register 3
04h	77h/	**OR4:** Option Register 4
04h	78h/	**OSPMBA:** OS Power Management I/O Base Address
04h	79h/	**PSMIBA:** PSMI I/O Base Address
04h	7Ah/	**APMBA:** Active Power Management (APM) I/O Base Address
04h	7Bh/	**CPU_RST:** Register for CPU only reset
04h	7Ch/	**OR5:** Options Register 5
04h	80h/	**TMC:** Thermal Management Control
04h	81h/	**TTR0:** Rank 0 Bandwidth Trip Thresholds; This holds the value to compare against the active event counts when bandwidth evaluation is enabled. It is programmed as a limit for traffic by BIOS to stay within thermal limits. It is recommended only using these in absence of thermal sensors.
04h	82h/	**TTR1:** Rank 1 Bandwidth Trip Thresholds
04h	83h/	**TTS:** SCH Bandwidth Trip Thresholds; Note that this register uses the sum of both ranks (if populated) to compare against this threshold, and shares the enforcement across the masks for both ranks

Port	Reg/Mem	Description
04h	84h/	**DTELB:** Default Thermal Enforcement Limits for Bandwidth Trips; This contains default enforcement limits for the power management controller to load when Bandwidth Evaluation is enabled, and the threshold has been exceeded. It is a starting point each time entering throttling. The power management controller may adjust the strength dynamically.
04h	85h/	**DTELT:** Default Thermal Enforcement Limits for Thermal Trips; Same as DTELB, but for Thermal based trips
04h	86h/	**LTEL:** Lowest Thermal Enforcement Limits; Same fields as defined in DTELB and DTELT, but this register defines the LOWEST limit the power management controller will enforce for both bandwidth-based or thermal-based enforcement.; If DTSC is disabled, this register is ignored.
04h	87h/	**GTEL:** Graphics Thermal Enforcement Limits; This contains default enforcement limits for the power management controller to load when a threshold has been exceeded
04h	B0h/	**TSC:** Thermal Sensor Control; All bits in this register are lockable via PCR.TSLC
04h	B1h/	**TRR:** Thermometer Read Register; This register generally provides the calibrated current temperature(s) from the thermometer circuit when the Thermometer mode is enabled.
04h	B2h/	**TPSTC:** All bits in this register are lockable via PCR.TSLC.
04h	B3h/	**TPSA:** Trip Point Settings Auxiliary
04h	B4h/	**CPSA:** Clear Point Settings Auxiliary
04h	B5h/	**TSIS:** Thermal Sensor and Interrupt Status; This contains status events for interrupts and which trip mechanisms are actively engaged. It does not distinguish which sensor was the source of the trip. TRR can be read to determine which zone each sensor is in, if necessary.
04h	B6h/	**TTB:** Thermal Trip Behavior
04h	C0h/	**TSIU0:** Thermal Sensor In-Use Bits
04h	C1h/	**TSIU1:** Thermal Sensor In-Use Bits
04h	C2h/	**TSIU2:** Thermal Sensor In-Use Bits
04h	C3h/	**TSIU3:** Thermal Sensor In-Use Bits
04h	C4h/	**TSIU4:** Thermal Sensor In-Use Bits
04h	C5h/	**TMA:** Address register for thermal MSI
04h	C6h/	**TMD:** Data register for thermal MSI
04h	C7h/	**DSP_POWERON_ADDR:** Address register for Display power-on MSI
04h	C8h/	**DSP_POWERON_DATA:** Data register for Display power-on MSI
04h	C9h/	**IMR_VIOLATION_ADDR:** Address register for IMR Violation MSI
04h	CAh/	**IMR_VIOLATION_DATA:** Data register for IMR Violation MSI

Port	Reg / Mem	Description
04h	CBh/	**8051_FW_DEBUG0:**
04h	CCh/	**8051_FW_DEBUG1:**
04h	E0h/	**GMCH_PERF_EVTSEL0:** GMCH_PERF_EVTSEL0
04h	E1h/	**GMCH_PERF_EVTSEL1:** GMCH_PERF_EVTSEL1
04h	E2h/	**GMCH_PERF_EVTSEL2:** GMCH_PERF_EVTSEL2
04h	E3h/	**GMCH_PERF_EVTSEL3:** GMCH_PERF_EVTSEL3
04h	E8h/	**PASR_DW0:** DDR PASR DW0
04h	E9h/	**PASR_DW1:** DDR PASR DW1
05h	00h/	**DFX.ZCONFIG_CFGREG0:**
05h	01h/	**DFX.ZCONFIG_CFGREG1:**
05h	02h/	**DFX.ZCONFIG_VISA_REG:** visa debug
05h	03h/	**DFX.ZCONFIG_CFGREG3:**
05h	08h/	**DFX.PMU_JTAG_STRAPPING:** PMU_JTAG_STRAPPING
05h	18h/	**DFX.GLB_JTAG_STRAPPING:** GLB_JTAG_STRAPPING
05h	20h/	**DFX.SPARE_MSGBUS_TAP:** unused
05h	30h/	**DFX.VIZA_REG0:** visa reg0
05h	34h/	**DFX.VIZA_REG1:** visa reg1
05h	38h/	**DFX.VIZA_REG2:** visa reg2
05h	3ch/	**DFX.VIZA_REG3:** visa reg3
05h	40h/	**DFX.VIZA_REG4:** visa reg4
05h	44h/	**DFX.VIZA_REG5:** visa reg5
05h	48h/	**DFX.VIZA_REG6:** visa reg6
05h	4ch/	**DFX.VIZA_REG7:** visa reg7
05h	50h/	**DFX.VIZA_REG8:** visa reg8
05h	54h/	**DFX.VIZA_REG9:** visa reg9
05h	58h/	**DFX.VIZA_REG10:** visa reg10
05h	5ch/	**DFX.VIZA_REG11:** visa reg11
05h	60h/	**DFX.VIZA_REG12:** visa reg12
05h	64h/	**DFX.VIZA_REG13:** visa reg13
05h	68h/	**DFX.VIZA_REG14:** visa reg14
05h	6ch/	**DFX.VIZA_REG15:** visa reg15
05h	70h/	**DFX.VIZA_REG16:** visa reg16
05h	74h/	**DFX.VIZA_REG17:** visa reg17
05h	78h/	**DFX.VIZA_REG18:** visa reg18
05h	84h/	**DFX.IOMAP_GPIO_CFG:** IO mapper GPIO0 config register

Port	Reg/Mem	Description
05h	88h/	**DFX.IOMAP_GPIO_DPIO_CFG:** IO mapper GPIO, dpio0 config register
05h	8ch/	**DFX.IOMAP_DPIO_LVDS_CFG:** IO mapper GPIO, dpio0 config register
05h	90h/	**DFX.RSVD_CFG:** RSVD register
05h	C0h/	**DFX.BIST_ARRAY_VED_SCTINIT:** sctinit bit to SRAM mem of ved
05h	C4h/	**DFX.BIST_ARRAY_MS00H:**
05h	C8h/	**DFX.MBIST_MODE_EN:**
05h	E0h/	**DFX.GMCH_PERF_EVTSEL0:** GMCH_PERF_EVTSEL0
05h	E1h/	**DFX.GMCH_PERF_EVTSEL1:** GMCH_PERF_EVTSEL1
05h	E2h/	**DFX.GMCH_PERF_EVTSEL2:** GMCH_PERF_EVTSEL2
05h	E3h/	**DFX.GMCH_PERF_EVTSEL3:** GMCH_PERF_EVTSEL2
05h	E8h/	**DFX.GMCH_PERF_FIXED_CTR0:** Fixed Counter 0 -- counts coreclk cycles when enabled
05h	F0h/	**DFX.GMCH_PERF_CAPABILITIES:** Perfmon Capabilities Register and Clock gating override
05h	F1h/	**DFX.GMCH_PERF_GLOBAL_CTRL:** Perfmon fixed and General Counter Control
05h	F2h/	**DFX.GMCH_PERF_GLOBAL_STATUS:** Perfmon fixed and General Counter Status
05h	F3h/	**DFX.GMCH_PERF_GLOBAL_OVF_CTRL:** Perfmon fixed and General Counter Overflow Clear
05h	F4h/	**DFX.GMCH_PERF_FIXED_CTR_CTRL:** Fixed Counter Control
05h	F8h/	**DFX.GMCH_PERF_GP_CTR0_L:** General Purpose Counter 0 Lower Half
05h	F9h/	**DFX.GMCH_PERF_GP_CTR1_L:** General Purpose Counter 1 Lower Half
05h	FAh/	**DFX.GMCH_PERF_GP_CTR2_L:** General Purpose Counter 2
05h	FBh/	**DFX.GMCH_PERF_GP_CTR3_L:** General Purpose Counter 3
05h	FCh/	**DFX.GMCH_PERF_GP_CTR0_H:** General Purpose Counter 0 Upper Half
05h	FDh/	**DFX.GMCH_PERF_GP_CTR1_H:** General Purpose Counter 1 Upper Half
05h	FEh/	**DFX.GMCH_PERF_GP_CTR2_H:** General Purpose Counter 2 Upper Half
05h	FFh/	**DFX.GMCH_PERF_GP_CTR3_H:** General Purpose Counter 3 Upper Half
06h	/00 70410h	**DISPLAY_CONTROLLER.SWFXX:** These 32 bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is

Port	Reg / Mem	Description
		defined by the software architecture.
06h	/02020h	**GVD.PGTBL_CTL:** Page Table Control. The PGTBL_CTL register is provides the starting physical memory address of the Graphics Translation Table (GTT). ; Once a GTT is established, software must use the GTTADR space to update entries in the GTT. GTTADR is a 256KB space claimed by graphics device during PCI enumeration. This allows the device to ; The GTT must be 4KByte aligned. The GTT must reside in unsnooped Main Memory and must be contiguous 256KBs.
06h	/02024h	**GVD.PGTBL_ER:** Page Table Error. The PGTBL_ER Debug register stores information indicating the source of an error associated with GM mapping via GTT. XX_INVALID_GTE_PTE: Translated Page Table Entry (PTE) is marked as not valid. Implemented by all streams. Detected at translation time.
06h	/02028h	**GVD.CLAIM_ER:** Claim Error Counter - counts the RM claim error (no RM claim) reported at CLAIM_ERROR field of EIR.
06h	/02050h	**GVD.MISR4:** MISR4
06h	/02060h	**GVD.GFX_GVD_CG_DIS:** GFX/GVD Clock Gating Disable
06h	/02064h	**GVD.VED_CG_DIS:** VED Clock Gating Disable
06h	/02084h	**GVD.IIR_RW:** Alternate means to access the IIR register. This address provides software RW access to the IIR register. Write/Restore to the IIR register using this address will not trigger an interrupt to the CPU.
06h	/02098h	**GVD.GVD_ECO:** Spare Register for HW ECOs
06h	/0209Ch	**GVD.SCPD0:** Scratch Pad 0 Register
06h	/020A0h	**GVD.IER:** IER: Interrupt Enable Register. The IER register contains an interrupt enable bit for each interrupt bit in the Interrupt Identity Register (IIR) register. A disabled interrupt will still appear in the Interrupt Identity Register to allow polling of interrupt sources. The bits in this register enable a CPU interrupt to be generated whenever the corresponding bit in the Interrupt Identity Register becomes set.
06h	/020A4h	**GVD.IIR:** IIR: Interrupt Identity Register. The IIR register contains the persistent values of the interrupt bits that are unmasked by the IMR and thus can generate a CPU interrupt (if enabled via the IER). When a CPU interrupt is generated, this should be the first register to be interrogated to determine the source of the interrupt. Bits set in this register will remain set until the interrupt condition is cleared by software. Writing a 1 into the appropriate bit position within this register clears interrupts. ; Programming Note: Prior to clearing a Display Pipe-sourced interrupt (e.g., Display Pipe A VBLANK) in the IIR, the corresponding interrupt (source) status in the PIPEASTAT register (e.g., Pipe A VBLANK Interrupt Status bit of PIPEASTAT) must first be cleared.
06h	/020A8h	**GVD.IMR:** IMR: Interrupt Mask. The IMR register is used by software to control which ISR bits are masked or unmasked. Unmasked bits will be reported in the IIR, possibly triggering a CPU interrupt, and will persist in the IIR until cleared by software. Masked bits will not be reported in the IIR and

Port	Reg/Mem	Description
		therefore cannot generate CPU interrupts.
06h	/020ACh	**GVD.ISR:** Interrupt Status The ISR register contains the non-persistent value of all interrupt status bits. The IMR register selects which of these interrupt conditions are reported in the persistent IIR (i.e., set bits must be cleared by software). Bits in the IER are used to selectively enable IIR bits to cause CPU interrupts. The User Interrupt bit in this register is a short pulse therefore software should not expect to use this register to sample these conditions.
06h	/020B0h	**GVD.EIR:** Error Identity. This register contains the persistent values of ESR error status bits that are unmasked via the EMR register. The logical OR of all (defined) bits in this register is reported in the Master Error bit of the Interrupt Status Register (ISR). In order to clear an error condition, software must first clear the error by writing a 1 to the appropriate bit(s) in this field. If required, software should then proceed to clear the Master Error bit of the IIR.
06h	/020B4h	**GVD.EMR:** Error Mask. This register contains a bit mask that selects which error condition bits (from the ESR) are reported in the EIR.
06h	/020B8h	**GVD.ESR:** Error Status. This register contains the non-persistent values of all hardware-detected error condition bits.
06h	/020C8h	**GVD.DISP_CLK_FREQ:** Encoding of Display clock and Core clock frequency as determined by CCK unit.
06h	/020CCh	**GVD.GM_FREQ:** The Display clock frequency to be used for generating the GM clock.
06h	/020D4h	**GVD.GTHROT:** GVD Thermal Throttling Register programmed by SBIOS.
06h	/020E0h	**GVD.FW_BLC_SELF:** Display FIFO Watermark
06h	/020E4h	**GVD.MI_ARB:** Display FIFO Watermark
06h	/020F8h	**GVD.G_HP_CONTROL:** GVD HP Arbitration Control Register
06h	/020FCh	**GVD.G_CONTROL:** GVD Control Register
06h	/02100 02103h	**DISPLAY_CONTROLLER.DPIO_PACKET_REGISTER:** Description Control and Address of DPIO indirect
06h	/02100h	**GVD.SB_PCKT:** When the Sideband Packet Register is written, the “GFX/VED/Media configuration” creates a transaction towards the destination agent on the IOSF sideband channel, using the fields sent with the write operation as transaction parameters, as described below: ; - The Sideband Rid filed (bits 31:24) is used as the transaction Rid ; - The Sideband Opcode filed (bits 23:15) is used as the transaction opcode ; - The Sideband Port filed (bits 15:8) is used as the transaction destination port ; - The source port is hard-coded to 6h (“GFX/VED/Media configuration” port) ; - The Sideband Byte Enable Field (bits 7:4) is used as the transaction Byte Enable ; If the opcode results in a data write semantic transaction, the write-data will be taken from the Sideband Data Register. If the opcode results in a data read semantic transaction, the read-data will be placed in the Sideband Data Register and may later be read by software. ; When Sideband Busy is set, Sideband

Port	Reg / Mem	Description
		Packet Register, Sideband Data Register and Sideband Address Register fields cannot be written. If the opcode results in a data read semantic transaction, data will be ready at Sideband Data register only when the Sideband Busy is cleared.
06h	/02104h	**GVD.SB_DATA:** The Sideband Data Register is used by the sideband register access mechanism (triggered by Sideband Packet Register) for holding write-data in write-transactions or read-data for read-transactions as explained below
06h	/02104h 02107h	**DISPLAY_CONTROLLER.DPIO_DATA_REGISTER:** Description Data of DPIO indirect
06h	/02108h	**GVD.SB_ADDR:** The Sideband Address Register is used by the sideband transaction (triggered by Sideband Packet Register) for holding the address (of the internal register, within the destination unit).
06h	/02110h	**GVD.DPIO_CFG:** DPIO configuration register. Note: the reset signal for this register is the `CDV.pmu_xxx_powergood_zcrnfwh
06h	/05010h	**DISPLAY_CONTROLLER.GPIOCTL_0:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
06h	/05014h	**DISPLAY_CONTROLLER.GPIOCTL_1:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are

Port	Reg / Mem	Description
		multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
06h	/05018h	**DISPLAY_CONTROLLER.GPIOCTL_2:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
06h	/0501Ch	**DISPLAY_CONTROLLER.GPIOCTL_3:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
06h	/05020h	**DISPLAY_CONTROLLER.GPIOCTL_4:** Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual

Port	Reg / Mem	Description
		status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.
06h	/05100h	**DISPLAY_CONTROLLER.GMBUS0:** Description GMBUS clock and port select gmbus_register.v reg_gmbus0 The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to. The clock rate options are 50KHz 100KHz 400KHz and 1MHz. This register should be set before the first data valid bit is set because it will be read only at the very first data valid bit and not read during the period of the transmission until stop is issued and next first data valid bit is set.
06h	/05104h	**DISPLAY_CONTROLLER.GMBUS1:** Description GMBUS command and status gmbus_register.v reg_gmbus1 This register lets the software indicate to the GMBUS controller the slave device address register index and indicate when the data write is complete. When the SW_CLR_INT bit is asserted all writes to the GMBUS2 GMBUS3 and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.
06h	/05108h	**DISPLAY_CONTROLLER.GMBUS2:** Description GMBUS status gmbus_register.v reg_gmbus2
06h	/0510Ch	**DISPLAY_CONTROLLER.GMBUS3:** Description GMBUS data buffer gmbus_register.v reg_gmbus3 This is data read write register. This register is double buffered. Bit 0 is the first bit sent or read bit 7 is the 8thbit sent or read all the way through bit 31 being the 32ndbit sent or read. For GMBUS write operations with a non zero byte count this register be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.
06h	/05110h	**DISPLAY_CONTROLLER.GMBUS4:** Description GMBUS interrupt mask gmbus_register.v reg_gmbus4
06h	/05120h	**DISPLAY_CONTROLLER.GMBUS5:** Description GMBUS index gmbus_register.v reg_gmbus5 This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.
06h	/05130h	**DISPLAY_CONTROLLER.GMBUS6:** Description GMBUS data buffer gmbus_register.v reg_gmbus6 This is the AKSV write register written by system BIOS on boot. Bit 0 is the first bit sent bit 7 is the 8thbit sent through bit 31 being the 32ndbit sent.
06h	/05134h	**DISPLAY_CONTROLLER.GMBUS7:** Description GMBUS data buffer gmbus_register.v reg_gmbus7 This is the AKSV write

Port	Reg / Mem	Description
		register written by system BIOS on boot. Bit 0 is the first bit sent through bit 7 being the 8thbit sent.
06h	/06014h	**DISPLAY_CONTROLLER.DPLLA_CTRL:** Description DPLL A Control cpdmmreg.v reg03_lt
06h	/06018h	**DISPLAY_CONTROLLER.DPLLB_CTRL:** Description DPLL B Control cpdmmreg.v reg04_lt
06h	/0601Ch	**DISPLAY_CONTROLLER.DPLLAMD:** Description Pipe A multiply cpdmmreg.v reg15_lt
06h	/06020h	**DISPLAY_CONTROLLER.DPLLBMD:** Description Pipe B multiplier cpdmmreg.v reg16_lt
06h	/06104	**DISPLAY_CONTROLLER.D_STATE:** Description Power state behavior cpdmmreg.v reg11_lt
06h	/06200h	**DISPLAY_CONTROLLER.DSPCLK_GATE_D:** Description clock gating cpdmmreg.v reg12_lt
06h	/06210h	**DISPLAY_CONTROLLER.RAMCLK_GATE_D:** Description memory clock gating cpdmmreg.v gfxramcg2
06h	/0A000h	**DISPLAY_CONTROLLER.DPALETTE_A:** Table 8206 1 8209 2. 8 Bit Mode
06h	/0A800h	**DISPLAY_CONTROLLER.DPALETTE_B:** 8 Bit Mode
06h	/30000h	**DISPLAY_CONTROLLER.OVADD:** This register provides a graphics memory address that will be used on the next Overlay register update. This graphics memory address points to an array of Overlay registers. This register cannot be used to flip the overlay if the cache has not been configured through a command pipe flip packet.
06h	/30004h	**DISPLAY_CONTROLLER.OTEST:**
06h	/30008h	**DISPLAY_CONTROLLER.DOVSTA:** This read only register indicates status for the overlay. Since the Overlay pipe can be assigned to either display pipe references to display are either the pipe A timing generator or the pipe B timing generator depending on which the Overlay logic is currently slaved to.
06h	/3000Ch	**DISPLAY_CONTROLLER.DOVSTAEX:** This read only register provides extended status information about the overlay. The format is RESERVED.
06h	/30010h	**DISPLAY_CONTROLLER.OGAMC5:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to

Port	Reg / Mem	Description
		GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
06h	/30014h	**DISPLAY_CONTROLLER.OGAMC4:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
06h	/30018h	**DISPLAY_CONTROLLER.OGAMC3:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in

Port	Reg/Mem	Description
		YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
06h	/3001Ch	**DISPLAY_CONTROLLER.OGAMC2:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
06h	/30020h	**DISPLAY_CONTROLLER.OGAMC1:** These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
06h	/30024h	**DISPLAY_CONTROLLER.OGAMC0:** These registers are used to determine the characteristics of the gamma correction for

Port	Reg / Mem	Description
		the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.
06h	/30058h	**DISPLAY_CONTROLLER.OVRSYNCPH0:**
06h	/3005Ch	**DISPLAY_CONTROLLER.OVRSYNCPH1:**
06h	/30060h	**DISPLAY_CONTROLLER.OVRSYNCPH2:**
06h	/30064h	**DISPLAY_CONTROLLER.OVRSYNCPH3:**
06h	/30100h	**DISPLAY_CONTROLLER.OBUF_0Y:** This register value is mirrored from DDR in address 00h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
06h	/30104h 30107	**DISPLAY_CONTROLLER.OBUF_1Y:** This register value is mirrored from DDR in address 04h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
06h	/30108h 3010B	**DISPLAY_CONTROLLER.OBUF_0U:** This register value is mirrored from DDR in address 08h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
06h	/3010Ch	**DISPLAY_CONTROLLER.OBUF_0V:** This register value is mirrored from DDR in address 0Ch R W . This value specifies

Port	Reg / Mem	Description
		the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
06h	/30110h 30113	**DISPLAY_CONTROLLER.OBUF_1U:** This register value is mirrored from DDR in address 10h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
06h	/30114h	**DISPLAY_CONTROLLER.OBUF_1V:** This register value is mirrored from DDR in address 14h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.
06h	/30118h 3011B	**DISPLAY_CONTROLLER.OSTRIDE:** This register value is mirrored from DDR in address 18h R W . These values represent the stride of the overlay video data buffers. A stride value determines the line to line increment of the buffer which is independent of the actual width of the overlay video data that gets displayed. . The memory Address Offset in DDR is Read Write.
06h	/3011Ch	**DISPLAY_CONTROLLER.YRGB_VPH:** This register value is mirrored from DDR in address 1Ch R W . The memory Address Offset in DDR is Read Write.
06h	/30120h	**DISPLAY_CONTROLLER.UV_VPH:** This register value is mirrored from DDR in address 20h R W . The memory Address Offset in DDR is Read Write.
06h	/30124h	**DISPLAY_CONTROLLER.HORZ_PH:** This register value is mirrored from DDR in address 24h R W . The memory Address Offset in DDR is Read Write.
06h	/30128h	**DISPLAY_CONTROLLER.INIT_PHS:** This register value is mirrored from DDR in address 28h R W . This register provides a method to create a negative initial phase or one with a positive integer offset. If the corresponding bits are set to all ones the initial phase is the fractional phase register value minus one. These bits should only be set in cases where the buffer pointer is pointing to the first pixel of the line or column because it will effectively cause the first pixel to be duplicated. The memory Address Offset in DDR is Read Write.
06h	/3012Ch	**DISPLAY_CONTROLLER.DWINPOS:** This register value is mirrored from DDR in address 2Ch R W . The memory Address Offset in DDR is Read Write.
06h	/30130h	**DISPLAY_CONTROLLER.DWINSZ:** This register value is mirrored from DDR in address 30h R W . The memory Address

Port	Reg / Mem	Description
		Offset in DDR is Read Write.
06h	/30134h	**DISPLAY_CONTROLLER.SWIDTH:** This register value is mirrored from DDR in address 34h R W . The memory Address Offset in DDR is Read Write.
06h	/30138h	**DISPLAY_CONTROLLER.SWIDTHSW:** This register value is mirrored from DDR in address 38h R W . Hardware uses values in this register to determine the number of SWORDs 32 bytes to be fetched from the memory for each overlay source scan line. The memory Address Offset in DDR is Read Write.
06h	/3013Ch	**DISPLAY_CONTROLLER.SHEIGHT:** This register value is mirrored from DDR in address 3Ch R W . The memory Address Offset in DDR is Read Write.
06h	/30140h	**DISPLAY_CONTROLLER.YRGBSCALE:** This register value is mirrored from DDR in address 40h R W . The memory Address Offset in DDR is Read Write.
06h	/30144h	**DISPLAY_CONTROLLER.UVSCALE:** This register value is mirrored from DDR in address 44h R W . The memory Address Offset in DDR is Read Write.
06h	/30148h	**DISPLAY_CONTROLLER.OCLRC0:** This register value is mirrored from DDR in address 48h R W . The memory Address Offset in DDR is Read Write.
06h	/3014Ch	**DISPLAY_CONTROLLER.OCLRC1:** This register value is mirrored from DDR in address 4Ch R W . The sum of the absolute value of SH_SIN and SH_COS must be limited to less than 8. ABS SH_SIN ABS SH_COS. The memory Address Offset in DDR is Read Write.
06h	/30150h	**DISPLAY_CONTROLLER.DCLRKV:** This register value is mirrored from DDR in address 50h R W . The memory Address Offset in DDR is Read Write.
06h	/30154h	**DISPLAY_CONTROLLER.DCLRKM:** This register value is mirrored from DDR in address 54h R W . The memory Address Offset in DDR is Read Write.
06h	/30158h	**DISPLAY_CONTROLLER.SCHRKVH:** This register value is mirrored from DDR in address 58h R W . The memory Address Offset in DDR is Read Write.
06h	/3015Ch	**DISPLAY_CONTROLLER.SCHRKVL:** This register value is mirrored from DDR in address 5Ch R W . The memory Address Offset in DDR is Read Write.
06h	/30160h	**DISPLAY_CONTROLLER.SCHRKEN:** This register value is mirrored from DDR in address 60h R W . The memory Address Offset in DDR is Read Write.
06h	/30164h	**DISPLAY_CONTROLLER.OCONFIG:** This register value is mirrored from DDR in address 64h R W . The memory Address Offset in DDR is Read Write.
06h	/30168h	**DISPLAY_CONTROLLER.OCOMD:** This register value is mirrored from DDR in address 68h R W . This register and the Overlay Configuration register provide the basic programming

Port	Reg / Mem	Description
		options that the overlay engine needs to begin its work. The memory Address Offset in DDR is Read Write.
06h	/30170h	**DISPLAY_CONTROLLER.OSTART_0Y:** This register value is mirrored from DDR in address 70h R W . The memory Address Offset in DDR is Read Write.
06h	/30174h	**DISPLAY_CONTROLLER.OSTART_1Y:** This register value is mirrored from DDR in address 74h R W . The memory Address Offset in DDR is Read Write.
06h	/30178h	**DISPLAY_CONTROLLER.OSTART_0U:** This register value is mirrored from DDR in address 78h R W . The memory Address Offset in DDR is Read Write.
06h	/3017Ch	**DISPLAY_CONTROLLER.OSTART_0V:** This register value is mirrored from DDR in address 7Ch R W . The memory Address Offset in DDR is Read Write.
06h	/30180h	**DISPLAY_CONTROLLER.OSTART_1U:** This register value is mirrored from DDR in address 80h R W . The memory Address Offset in DDR is Read Write.
06h	/30184h	**DISPLAY_CONTROLLER.OSTART_1V:** This register value is mirrored from DDR in address 84h R W . The memory Address Offset in DDR is Read Write.
06h	/30188h	**DISPLAY_CONTROLLER.OTILEOFF_0Y:** This register value is mirrored from DDR in address 88h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
06h	/3018Ch	**DISPLAY_CONTROLLER.OTILEOFF_1Y:** This register value is mirrored from DDR in address 8Ch R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
06h	/30190h	**DISPLAY_CONTROLLER.OTILEOFF_0U:** This register value is mirrored from DDR in address 90h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
06h	/30194h	**DISPLAY_CONTROLLER.OTILEOFF_0V:** This register value is mirrored from DDR in address 94h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of

Port	Reg / Mem	Description
		this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
06h	/30198h	**DISPLAY_CONTROLLER.OTILEOFF_1U:** This register value is mirrored from DDR in address 98h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
06h	/3019Ch	**DISPLAY_CONTROLLER.OTILEOFF_1V:** This register value is mirrored from DDR in address 9Ch R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.
06h	/301A0h	**DISPLAY_CONTROLLER.RESERVED:** This register value is mirrored from DDR in address 0h R W . The memory Address Offset in DDR is Read Write.
06h	/301A4h	**DISPLAY_CONTROLLER.UVSCALEV:** This register value is mirrored from DDR in address 4h R W . The memory Address Offset in DDR is Read Write.
06h	/30300h	**DISPLAY_CONTROLLER.Y_VCOEFS:** This register value is mirrored from DDR in address 200h R W . The memory Address Offset in DDR is Read Write. The offset is 200h 2FFh
06h	/30400h	**DISPLAY_CONTROLLER.Y_HCOEFS:** This register value is mirrored from DDR in address 300h R W . The memory Address Offset in DDR is Read Write. The offset is 300h 4FFh
06h	/30600h	**DISPLAY_CONTROLLER.UV_VCOEFS:** This register value is mirrored from DDR in address 500h R W . The memory Address Offset in DDR is Read Write. The offset is 500h 5FFh
06h	/30700h	**DISPLAY_CONTROLLER.UV_HCOEFS:** This register value is mirrored from DDR in address 600h R W . The memory Address Offset in DDR is Read Write. The offset is 600h 6FFh.
06h	/60000h	**DISPLAY_CONTROLLER.HTOTAL_A:**
06h	/60004h	**DISPLAY_CONTROLLER.HBLANK_A:**
06h	/60008h	**DISPLAY_CONTROLLER.HSYNC_A:**
06h	/6000Ch	**DISPLAY_CONTROLLER.VTOTAL_A:**
06h	/60010h	**DISPLAY_CONTROLLER.VBLANK_A:**
06h	/60014h	**DISPLAY_CONTROLLER.VSYNC_A:**
06h	/6001Ch	**DISPLAY_CONTROLLER.PIPESRCA:**
06h	/60020h	**DISPLAY_CONTROLLER.BCLRPAT_A:** This register value

Port	Reg/Mem	Description
		determines what color should be sent to the display in the border region the space between the end of active and the beginning of blank and the end of blank and the beginning of active.
06h	/60028h	**DISPLAY_CONTROLLER.VSYNCSHIFT_A:**
06h	/60050h	**DISPLAY_CONTROLLER.CRCCTRLREDA:** The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. For any changes to the CRC controls you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. Border area is always included in the CRC calculation. There are five CRC calculators Red Green Blue Residual1 and Residual2 DevCTG DevIntel Atom Processor D2000 series and N2000 Series each with an 8 bit data input and 23 bit CRC result. For Display Port CRC DevCTG Dev Intel Atom Processor D2000 series and N2000 Series the 40 bit lane data is spread across the inputs of all five of the CRC calculators. For Pipe the 30 bit pixel data is spread across the inputs of four of the CRC calculators. The fifth is unused and will be ignored for expected CRC comparison and error generation. Pipe CRC should not be run when Display Port or TV is enabled on this pipe.
06h	/60054h	**DISPLAY_CONTROLLER.CRCCTRLGREENA:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
06h	/60058h	**DISPLAY_CONTROLLER.CRCCTRLBLUEA:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
06h	/6005Ch	**DISPLAY_CONTROLLER.CRCCTRLALPHAA:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
06h	/60060h	**DISPLAY_CONTROLLER.CRCRESREDA:**
06h	/60064h	**DISPLAY_CONTROLLER.CRCRESGREENA:**
06h	/60068h	**DISPLAY_CONTROLLER.CRCRESBLUEA:**
06h	/6006Ch	**DISPLAY_CONTROLLER.CRCRESALPHAA:**
06h	/60070h	**DISPLAY_CONTROLLER.CRCCTRLRESIDUE2A:** Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC

Port	Reg / Mem	Description
		calculations.
06h	/60080h	**DISPLAY_CONTROLLER.CRCRESRESIDUE2A:** The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
06h	/61000h	**DISPLAY_CONTROLLER.HTOTAL_BPIPE_B_HORIZONTAL_TOTAL_REGISTER:**
06h	/61004h	**DISPLAY_CONTROLLER.HBLANK_BPIPE_B_HORIZONTAL_BLANK_REGISTER:**
06h	/61008h	**DISPLAY_CONTROLLER.HSYNC_BPIPE_B_HORIZONTAL_SYNC_REGISTER:**
06h	/6100Ch	**DISPLAY_CONTROLLER.VTOTAL_BPIPE_BVERTICAL_TOTAL_REGISTER:**
06h	/61010h	**DISPLAY_CONTROLLER.VBLANK_BPIPE_BVERTICAL_BLANK_REGISTER:**
06h	/61014h	**DISPLAY_CONTROLLER.VSYNC_BPIPE_B_VERTICAL_SYNC_REGISTER:**
06h	/6101Ch	**DISPLAY_CONTROLLER.PIPEBSRC:**
06h	/61020h	**DISPLAY_CONTROLLER.BCLRPAT_B:** This register determines the color sent during the border region the periods between the end of blank and the start of active and the end of active and the start of blank. Also same color will be sent during pseudo border period. VGA border color is determined by the VGA border overscan color register.
06h	/61028h	**DISPLAY_CONTROLLER.VSYNCSHIFT_B:**
06h	/61050h	**DISPLAY_CONTROLLER.CRCCTRLREDB:** The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. For any changes to the CRC controls you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. Border area is always included in the CRC calculation. See description of CRCCtrlColorA for more details
06h	/61054h	**DISPLAY_CONTROLLER.CRCCTRLGREENB:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.
06h	/61058h	**DISPLAY_CONTROLLER.CRCCTRLBLUEB:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.
06h	/6105Ch	**DISPLAY_CONTROLLER.CRCCTRLALPHAB:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.
06h	/61060h	**DISPLAY_CONTROLLER.CRCRESREDB:**
06h	/61064h	**DISPLAY_CONTROLLER.CRCRESGREENB:**

Port	Reg/Mem	Description
06h	/61068h	**DISPLAY_CONTROLLER.CRCRESBLUEB:**
06h	/6106Ch	**DISPLAY_CONTROLLER.CRCRESALPHAB:**
06h	/61070h	**DISPLAY_CONTROLLER.CRCCTRLRESIDUE2B:** Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
06h	/61080h	**DISPLAY_CONTROLLER.CRCRESRESIDUAL2B:** The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.
06h	/61100h	**DISPLAY_CONTROLLER.ADPA:** Description CRT port control dprrega.v adp_Q
06h	/61104h	**DISPLAY_CONTROLLER.CRTIO_DFX:** Description CRT port control dprrega.v crt_dfx
06h	/61110h	**DISPLAY_CONTROLLER.PORT_HOTPLUG_EN:** Description DPD enable control dprrega.v ql_hotplugen_Q NOTE For correct operation of display port hot plug detection the device 2 configuration register GMBUSFREQ at offset 0xCC 0xCD must be programmed correctly.
06h	/61114h	**DISPLAY_CONTROLLER.PORT_HOTPLUG_STAT:** Description CRT port control dprrega.v porthotst_aR This register is the second level of a two level interrupt and status scheme. Status bits in this register are sticky once set they can be cleared by writing a one to that bit. A write of a zero does not affect the corresponding Interrupt status bit. The corresponding enable bits determine if the interrupt status bit should be propagated to the first line interrupt status register. When an interrupt occurs the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt. Before clearing a Port sourced interrupt e.g. CRT hotplug in the IIR the corresponding interrupt source status in the PORT_HOTPLUG_STAT must be cleared by writing a 1 to the appropriate bit. In the case where fields are larger than 1 bit wide all bits in the field must be cleared by writing a 1 to them.
06h	/61140h	**DISPLAY_CONTROLLER.SDVO_HDMIB:** Description HDMIB port control dprrega.v sdvo_bQ Note This Digital Display Port defaults to sDVO port functionality when it is not programmed as a HDMI port. The operating mode of the port is determined by the setting of the encoding register field bits 11 10.
06h	/61150h	**DISPLAY_CONTROLLER.SDVO_DP:** Description DFT DPIO and AUX control dprrega.v sdvo_dftQ
06h	/61154h	**DISPLAY_CONTROLLER.SDVO_DP2:** Description DFT DPT control dprrega.v dpr_dpt_dft2_i
06h	/61160h	**DISPLAY_CONTROLLER.SDVO_HDMIC:** Description HDMIC port control dprrega.v sdvo_cQ Note This Digital Display Port defaults to sDVO port functionality when it is not programmed as a HDMI port. The operating mode of the port is determined

Port	Reg / Mem	Description
		by the setting of the encoding register field bits 11 10.
06h	/61170h	**DISPLAY_CONTROLLER.VIDEO_DIP_CTL:** Please note that writes to this register take effect immediately. Therefore it is critical for software to follow the write and read sequences as described in the bit 31 text.
06h	/61178h	**DISPLAY_CONTROLLER.VIDEO_DIP_DATA:** Description Video control dprrega.v only at read if_ramcsrddata
06h	/61180h	**DISPLAY_CONTROLLER.LVDS:** Description Video control dplreg.v lvds_port_cntl Write Protect by Panel Power Sequencer on
06h	/61184h	**DISPLAY_CONTROLLER.LVDSCKT1:** Description PHY LVDSIO TX Control dplrreg.v dsp_lvd_tx_cnt This register contains the control bit to get optimal performance out of LVDS Transmitter circuit
06h	/61188h	**DISPLAY_CONTROLLER.LVDSCKT2:** Description PHY LVDSIO Analog Control dplrreg.v dsp_lvd_ana_cnt This register contains circuit control bits to optimize analog reference circuit performance of lvdsphy
06h	/6118ch	**DISPLAY_CONTROLLER.LVDSCKT3:** Description PHY LVDSIO LoopBack Control dplrreg.v dsp_lvd_lb_cnt This register contains circuit control bits to optimize analog reference circuit performance of lvdsphy
06h	/61190h	**DISPLAY_CONTROLLER.LVDSCKT4:** Description PHY LVDSIO Future used dplrreg.v lvd_dsp_phy_spare
06h	/61194h	**DISPLAY_CONTROLLER.LVDSTCR:** Description PHY LVDSIO Future used dplrreg.v lvd_dsp_phy_spare
06h	/61200h	**DISPLAY_CONTROLLER.PP_STATUS:**
06h	/61204h	**DISPLAY_CONTROLLER.PP_CONTROL:** Description PP Control dplrreg.v pnl_pwr_cntl
06h	/61208h	**DISPLAY_CONTROLLER.PP_ON_DELAYS:** Description PP On Delay values dplrreg.v DPLRppon_sd Write Protect by Panel Power Sequencer on
06h	/6120Ch	**DISPLAY_CONTROLLER.PP_OFF_DELAYS:** Description PP Delay Off values dplrreg.v DPLRppoff_sd Write Protect by Panel Power Sequencer on Mobile products
06h	/61210h	**DISPLAY_CONTROLLER.PP_DIVISOR:** Description PP Divisor dplrreg.v DPLRrefdiv_pp_cd Write Protect by Panel Power Sequencer on Mobile Products. This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is .5 1.5 sec. But limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.
06h	/61230h	**DISPLAY_CONTROLLER.PFIT_CONTROL:**

Port	Reg / Mem	Description
06h	/61234h	**DISPLAY_CONTROLLER.PFIT_PGM_RATIOS:** When programmed scaling mode Panel Fitting Controls 28 26 001 is selected this determines the vertical and horizontal ratios used for panel fitting scaling. The values should be based on the source sizes and active sizes programmed into the pipe timing registers. The values written into the register should be rounded to the proper number of bits for the best precision. The value programmed should be source size register value 1 active size register value 1 When programmed scaling mode is not selected read back of this register gives the auto generated vertical and horizontal scaling ratios used for panel fitting scaling. Register writes will be ignored. The ratios are calculated each VBLANK. When in HiRes modes the values are based on the source sizes and active sizes programmed into the pipe timing registers. When in VGA modes it is determined by the VGA source sizes calculated by the VGA and active sizes from the pipe timing registers. VGA source sizes may have invalid values due to mode change transitions. These will eventually be correct when the mode change is complete. The value read is internally generated source size register value 1 active size register value 1 For each register field the MSB is the 1 bit integer value and the lower 12 bits are the fractional value. A value of 1.0 will indicate 1-to-1 scaling. A value greater than 1.0 will indicate downscaling. A value less than 1.0 will indicate up scaling. The vertical and horizontal ratios are usually identical except for when source and active aspect ratios differ.
06h	/61238h	**DISPLAY_CONTROLLER.RESERVED_USED_TO_BE_AUTO_SCALING_RATIOS_READBACK:**
06h	/6123Ch	**DISPLAY_CONTROLLER.RESERVED_USED_TO_BE_SCALING_INITIAL_PHASE:**
06h	/61250h	**DISPLAY_CONTROLLER.BLC_PWM_CLT2:**
06h	/61254h	**DISPLAY_CONTROLLER.BLC_PWM_CTL:**
06h	/61260h	**DISPLAY_CONTROLLER.BLM_HIST_CTL:**
06h	/61264h	**DISPLAY_CONTROLLER.IMAGE_ENHANCEMENT_BIN_DATA_REGISTER:** Writes to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index. Function 0 usage Threshold Count this Function is Read Only
06h	/61268h	**DISPLAY_CONTROLLER.HISTOGRAM_THRESHOLD_GUARDBAND_REGISTER:**
06h	/61400h	**DISPLAY_CONTROLLER.HDCP_CONFIG:** This register configures the HDCP mode.
06h	/61404h	**DISPLAY_CONTROLLER.HDCP_INIT:** This register is used to inject entropy into the An calculation. Hardware holds 64 bits of initialization vector. The hardware destination for writes to this register alternates between the high 32 bits and the low 32 bits. When generating An hardware will use the two most recent values written to this register as a 64 bit source of entropy.
06h	/61408h	**DISPLAY_CONTROLLER.HDCP_BKSV_LO:** This register

Port	Reg / Mem	Description
		holds part of the Bksv value.
06h	/6140Ch	**DISPLAY_CONTROLLER.HDCP_BKSV_HI:** This register holds part of the Bksv value.
06h	/61410h	**DISPLAY_CONTROLLER.HDCP_AN_LO:** This register holds part of the An value. Writeable with debug fuse enabled
06h	/61414h	**DISPLAY_CONTROLLER.HDCP_AN_HI:** This register holds part of the An value. Writeable with debug fuse enabled
06h	/61418h	**DISPLAY_CONTROLLER.HDCP_RI:** This register holds the receiver s Ri value.
06h	/6141Ch	**DISPLAY_CONTROLLER.HDCP_AKEY_LO:** This register holds part of the Akey value.
06h	/61420h	**DISPLAY_CONTROLLER.HDCP_AKEY_MED:** This register holds part of the Akey value.
06h	/61424h	**DISPLAY_CONTROLLER.HDCP_AKEY_HI:** This register holds part of the Akey value.
06h	/6142Ch	**DISPLAY_CONTROLLER.HDCP_V_0:** These registers hold the V hash result from the receiver used for repeaters.
06h	/61430h	**DISPLAY_CONTROLLER.HDCP_V_1:** These registers hold the V hash result from the receiver used for repeaters.
06h	/61434h	**DISPLAY_CONTROLLER.HDCP_V_2:** These registers hold the V hash result from the receiver used for repeaters.
06h	/61438h	**DISPLAY_CONTROLLER.HDCP_V_3:** These registers hold the V hash result from the receiver used for repeaters.
06h	/6143Ch	**DISPLAY_CONTROLLER.HDCP_V_4:** These registers hold the V hash result from the receiver used for repeaters.
06h	/61440h	**DISPLAY_CONTROLLER.HDCP_SHA1_IN:** This register provides the input for the SHA1 hash.
06h	/61444h	**DISPLAY_CONTROLLER.HDCP_REP:** This register describes information needed for HDCP repeater support.
06h	/61448h	**DISPLAY_CONTROLLER.HDCP_STATUS:** This register describes the HDCP status.
06h	/6144Ch	**DISPLAY_CONTROLLER.HDCP_DBG_STAT:** This register reports HDCP status information for debugging. Debug fuse removes all access
06h	/61450h	**DISPLAY_CONTROLLER.HDCP_AKSV_HI:** This is a clear on read register.
06h	/61454h	**DISPLAY_CONTROLLER.HDCP_AKSV_LO:** This is a clear on read register
06h	/62000h	**DISPLAY_CONTROLLER.AUD_CONFIG:** This register configures the audio output.
06h	/62010h	**DISPLAY_CONTROLLER.AUD_DEBUG:**
06h	/62020h	**DISPLAY_CONTROLLER.AUD_VID_DID:** These values are returned from the device as the Vendor ID Device ID response to a Get Root Node command. Previous default values

Port	Reg / Mem	Description
		808629FBh DEVCL 80862801h DEVBLC
06h	/62024h	**DISPLAY_CONTROLLER.AUD_RID:** These values are returned from the device as the Revision ID response to a Get Root Node command.
06h	/62028h	**DISPLAY_CONTROLLER.AUD_ROOT_SUBN_CNT:** These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.
06h	/62040h	**DISPLAY_CONTROLLER.AUD_FUNC_GRP:** These values are returned from the device as the Function Group Type response to a Get Audio Function Group command.
06h	/62044h	**DISPLAY_CONTROLLER.AUD_FUNCGRP_SUBN_CNT:** These values are returned from the device as the Subordinate Node Count response to a Get Audio Function Group command.
06h	/62048h	**DISPLAY_CONTROLLER.AUD_GRP_CAP:** These values are returned from the device as the Audio Function Group Capabilities response to a Get Audio Function Group command.
06h	/6204Ch	**DISPLAY_CONTROLLER.AUD_PWRST:** These values are returned from the device as the Power State response to a Get Audio Function Group command.
06h	/62050h	**DISPLAY_CONTROLLER.AUD_SUPPWR:** These values are returned from the device as the Supported Power States response to a Get Audio Function Group command.
06h	/62054h	**DISPLAY_CONTROLLER.AUD_SID:** These values are returned from the device as the Subsystem ID response to a Get Audio Function Group command.
06h	/62070h	**DISPLAY_CONTROLLER.AUD_OUT_CWCAP:** These values are returned from the device as the Audio Output Converter Widget Capabilities response to a Get Audio Output Converter Widget command. Previous default value 00000211h DevCL DevBLC
06h	/62074h	**DISPLAY_CONTROLLER.AUD_OUT_PCMSIZE:** These values are returned from the device as the PCM Size and Rates response to a Get Audio Output Converter Widget command. Previous default value 001E0170h DevCL DevBLC
06h	/62078h	**DISPLAY_CONTROLLER.AUD_OUT_STR:** These values are returned from the device as the Stream Formats response to a Get Audio Output Converter Widget command.
06h	/6207Ch	**DISPLAY_CONTROLLER.AUD_OUT_DIG_CNVT:** These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.
06h	/62080h	**DISPLAY_CONTROLLER.AUD_OUT_CH_STR:** These values are returned from the device as the Channel ID and Stream ID response to a Get Audio Output Converter Widget command.
06h	/62084h	**DISPLAY_CONTROLLER.AUD_OUT_STR_DESC:** These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.
06h	/620A0h	**DISPLAY_CONTROLLER.AUD_PINW_CAP:** These values are

Port	Reg / Mem	Description
		returned from the device as the Pin Complex Widget Capabilities response to a Get Pin Widget command.
06h	/620A4h	**DISPLAY_CONTROLLER.AUD_PIN_CAP:** These values are returned from the device as the Pin Capabilities response to a Get Pin Widget command.
06h	/620A8h	**DISPLAY_CONTROLLER.AUD_PINW_CONNLNG:** These values are returned from the device as the Connection List Length response to a Get Pin Widget command.
06h	/620ACh	**DISPLAY_CONTROLLER.AUD_PINW_CONNLST:** These values are returned from the device as the Connection List Entry response to a Get Pin Widget command.
06h	/620B0h	**DISPLAY_CONTROLLER.AUD_PINW_CNTR:** These values are returned from the device as the Pin Widget Control response to a Get Pin Widget command.
06h	/620B4h	**DISPLAY_CONTROLLER.AUD_CNTL_ST:**
06h	/620B8h	**DISPLAY_CONTROLLER.AUD_PINW_UNSOLRESP:** These values are returned from the device as the Unsolicited Response Enable response to a Get Pin Widget command.
06h	/620BCh	**DISPLAY_CONTROLLER.AUD_PINW_CONFIG:** These values are returned from the device as the Config Default response to a Get Pin Widget command.
06h	/620D4h	**DISPLAY_CONTROLLER.AUD_HDMIW_STATUS:**
06h	/6210Ch	**DISPLAY_CONTROLLER.AUD_HDMIW_HDMIEDID:** These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA 861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command. Writing sequence Video software sets ELD invalid and sets the ELD access address to 0 or to the desired DWORD to be written. Video software writes ELD data 1 DWORD at a time. The ELD access address auto increments with each DWORD write wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time. Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. Reading sequence Video software sets the ELD access address to 0 or to the desired DWORD to be read. Video software reads ELD data 1 DWORD at a time. The ELD access address auto increments with each DWORD read wrapping around to address 0 when the max buffer address size of 0xF has been reached.
06h	/62118h	**DISPLAY_CONTROLLER.AUD_HDMIW_INFOFR:** When the IF type or DWORD index is not valid the contents of the DIP will return all 0 s. These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the

Port	Reg/Mem	Description
		HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index then fetch the indexed byte using the HDMI DIP get. Video driver read sequence for debug only Video software sets DIP type to the appropriate DIP and sets the DIP access address to the desired DWORD. Video software reads DIP data 1 DWORD at a time. The DIP access address auto increments with each DWORD write wrapping around to address 0 when the max buffer address size of 0xF has been reached.
06h	/62120h	**DISPLAY_CONTROLLER.AUD_CONV_CHCNT:** HDMI converter Channel Mapping verb. Read only Reference HDMI SDVO EDS 0.79 Section 5.3.13 HDMI Channel to Converter Channel Mapping
06h	/62128h	**DISPLAY_CONTROLLER.AUD_CTS_ENABLE:** These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.
06h	/64100h	**DISPLAY_CONTROLLER.DP_B:** Description Display Port B control dprrega_b0.v ql_displayb1 Please note that DisplayPort B uses the same lanes as HDMIB. Therefore HDMIB and DisplayPort B cannot be enabled simultaneously. Calculation of TU is as follows For modes that divide into the link frequency evenly Active TU payload capacity. Please note that this is the same ratio as data m n Payload capacity dot clk bytes per pixel ls_clk of lanes
06h	/64110h	**DISPLAY_CONTROLLER.DPB_AUX_CH_CTL:** Description AuxB control dprrega_b0.v auxb_ctl_rdback Programming note Do not change any fields while Busy bit 31 is asserted.
06h	/64114h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA1:** Description AuxB Data1 dprrega_b0.v auxb_dpr_data1 ql_auxb_d1 The read value will not be valid while Busy bit 31 is asserted.
06h	/64118h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA2:** Description AuxB Data2 dprrega_b0.v auxb_dpr_data2 ql_auxb_d2 The read value will not be valid while Busy bit 31 is asserted.
06h	/6411Ch	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA3:** Description AuxB Data3 dprrega_b0.v auxb_dpr_data3 ql_auxb_d3 The read value will not be valid while Busy bit 31 is asserted.
06h	/64120h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA4:** Description AuxB Data4 dprrega_b0.v auxb_dpr_data4 ql_auxb_d4 The read value will not be valid while Busy bit 31 is asserted.
06h	/64124h	**DISPLAY_CONTROLLER.DPB_AUX_CH_DATA5:** Description AuxB Data5 dprrega_b0.v auxb_dpr_data5 ql_auxb_d5 The read value will not be valid while Busy bit 31 is asserted.
06h	/64130h	**DISPLAY_CONTROLLER.DP_AUX_CH_AKSV_HI:** Description AuxB AKSV High dprrega_b0.v dpr_aux_AKSV_hi This is programmed with the lower 4 bytes of AKSV. DP_AUX_AKSV_LO should be programmed with the highest byte of AKSV. More than one AUX channel can select to use the AKSV buffer simultaneously. This will become the second DWORD of the message when AKSV buffer is selected. The first DWORD will come from the DP_AUX_CH_DATA1 register.

Port	Reg / Mem	Description
06h	/64134h	**DISPLAY_CONTROLLER.DP_AUX_CH_AKSV_LO:** Description AuxB AKSV High dprrega_b0.v dpr_aux_AKSV_lo This is programmed with the highest byte of AKSV. DP_AUX_AKSV_HI should be programmed with the lower 4 bytes of AKSV. More than one AUX channel can select to use the AKSV buffer simultaneously.
06h	/64200h	**DISPLAY_CONTROLLER.DPC:** Description Display Port C control dprrega_b0.v ql_displayc1 Please note that DisplayPort C uses the same lanes as HDMIC. Therefore HDMIC and DisplayPort C cannot be enabled simultaneously.
06h	/64210h	**DISPLAY_CONTROLLER.DPC_AUX_CH_CTL:** Description AuxC Data1 dprrega_b0.v auxc_dpr_data1 ql_auxc_d1 Programming note Do not change any fields while Busy bit 31 is asserted.
06h	/64214h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA1:** Description AuxC Data1 dprrega_b0.v auxc_dpr_data1 ql_auxc_d1 The read value will not be valid while Busy bit 31 is asserted.
06h	/64218h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA2:** Description AuxC Data2 dprrega_b0.v auxc_dpr_data2 ql_auxc_d2 The read value will not be valid while Busy bit 31 is asserted.
06h	/6421Ch	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA3:** Description AuxC Data3 dprrega_b0.v auxc_dpr_data3 ql_auxc_d3 The read value will not be valid while Busy bit 31 is asserted.
06h	/64220h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA4:** Description AuxC Data4 dprrega_b0.v auxc_dpr_data4 ql_auxc_d4 The read value will not be valid while Busy bit 31 is asserted.
06h	/64224h	**DISPLAY_CONTROLLER.DPC_AUX_CH_DATA5:** Description AuxC Data5 dprrega_b0.v auxc_dpr_data5 ql_auxc_d5 The read value will not be valid while Busy bit 31 is asserted.
06h	/70000h	**DISPLAY_CONTROLLER.PIPEA_DSL:** This register enables the read back of the display pipe vertical line counter . The display line value is from the display pipe A timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation scan line zero is the first active line of the display. When in VGA centering mode the scan line 0 is the 1stactive scan line of the pseudo border not the centered active VGA image. In interlaced display timings the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Programming Note In order to cause the scan line logic to report the correct Line Counter value the corresponding Display Pipeline timing registers must be programmed to valid non zero e.g. 640x480 60Hz values before enabling the Pipe or programming VGA timing and enabling native VGA.
06h	/70004h	**DISPLAY_CONTROLLER.PIPEA_SLC:** This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands or through MMIO for DevBLC and DevCTG . They can safely be accessed at any time. The Top and Bottom Line Count Compare registers are compared with the display line values from display A timing generator. The Top compare

Port	Reg / Mem	Description
		register operator is a less than or equal while the Bottom compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts status and command stream flow control wait for within range and wait for not within range . For range check the value programmed should be the desired value 1 so for line 0 the value programmed is VTOTAL and for line 1 the value programmed is 0.
06h	/70008h	**DISPLAY_CONTROLLER.PIPEACONF:**
06h	/70010h	**DISPLAY_CONTROLLER.PIPEAGCMAXRED:**
06h	/70014h	**DISPLAY_CONTROLLER.PIPEAGCMAXGREEN:**
06h	/70018h	**DISPLAY_CONTROLLER.PIPEAGCMAXBLUE:**
06h	/70024h	**DISPLAY_CONTROLLER.PIPEASTAT:** This register is the second level of a two level interrupt and status scheme. A single bit in the first line interrupt status register represents the state of this register which is equal to the AND of a status bits with their corresponding enable bits OR ed together. First line interrupt status bits can cause interrupts or writes of the status register to cacheable memory. Bits in this register indicate the status of the display pipe A and can cause interrupt status bit changes in the first level interrupt and status register. Status bits in this register as sticky and once they are set will be cleared by writing a one to that bit. A write of a zero will not have an effect on the corresponding Interrupt status bit. The corresponding enable bits will determine if the interrupt status bit should be used in the first line interrupt status register. When an interrupt occurs the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt. Programming 1. Prior to clearing a Display Pipe sourced interrupt e.g. Display Pipe A VBLANK in the IIR the corresponding interrupt source status in the PIPEASTAT or PIPEBSTAT register e.g. Pipe A VBLANK Interrupt Status bit of PIPEASTAT must first be cleared. Note that clearing these status bits requires writing a 1 to the appropriate bit position.
06h	/70030h	**DISPLAY_CONTROLLER.DSPARB:** Notes Each active display plane A B or C requires a FIFO to cover for memory latency. The FIFOs all come from a single RAM that is divided into areas for each display plane. The amount of the RAM used by each display plane is defined by this register. The two fields in the register split the display RAM into three portions allocated between display planes A B and C. This register is double buffered and updated on the leading edge of Vertical Blank of the pipe that the planes are assigned to. This register should only be changed when a single pipe is enabled or if all of the Display A B C planes are disabled. It takes effect on the next VBLANK for whichever pipe is currently active. Each display plane needs a minimum FIFO size that is at least MaxLatencyForPlane PixelRate PixelSize 512. All values should be rounded up to the next unit of 64B. Notes A special C3 mode can occur when a single display of Display A and Display B is active and the overlay and Display C are disabled. In that mode when C3 is entered the values in the BSTART and CSTART

Port	Reg / Mem	Description
		fields are ignored and the entire RAM is allocated to the single active display plane. Notes DevBW and DevBLC The control granularity of FIFO size is 64 bytes and the total size of the RAM is 384 16 bytes making TOTALSIZE equal to 96. The range of values for CSTART and BSTART is 0 95. Notes DevCL DevCTG Dev Intel Atom Processor D2000 and N2000 Series The control granularity of FIFO size is 64 bytes and the total size of the RAM is 512 16 bytes making TOTALSIZE equal to 128. The range of values for CSTART and BSTART is 0 127. Notes DevBLC and DevCTG The entire register is reserved. Hardware controls the FIFO sizing automatically. Notes Dev D2000 series and N2000 Series FIFO Sizes A 28 B 31 C 37Notes The display dot clock frequency or pixel rate must not exceed 90 of the core display clock. When a primary plane is enabled with 64bpp format and sprite is also enabled on the same pipe the dot clock frequency or pixel rate must be less than 80 of the core display clock.
06h	/70034h	**DISPLAY_CONTROLLER.FW1:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.
06h	/70038h	**DISPLAY_CONTROLLER.FW2:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.
06h	/7003Ch	**DISPLAY_CONTROLLER.FW3:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.
06h	/70040h	**DISPLAY_CONTROLLER.PIPEAFRAMEHIGH:** Requires that this pipe s PLL is running
06h	/70044h	**DISPLAY_CONTROLLER.PIPEAFRAMEPIXEL:** Requires that this pipe s PLL be running
06h	/70050h	**DISPLAY_CONTROLLER.PIPEAGMCHDATAM:**
06h	/70054h	**DISPLAY_CONTROLLER.PIPEAGMCHDATAN:**
06h	/70060h	**DISPLAY_CONTROLLER.PIPEADPLINKM:**
06h	/70064h	**DISPLAY_CONTROLLER.PIPEADPLINKN:**
06h	/70070h	**DISPLAY_CONTROLLER.FW4:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level. For each FIFO there are two watermarks wmark1 and wmark. When FIFO status is above wmark1 hardware generates a status of 0. When FIFO status is between wmark1 and wmark it generates a status of 2. When FIFO status is below wmark it generates a status of 3. The FIFO status is indicated by the blue color. When the FIFO is full its FIFO status

Port	Reg/Mem	Description
		is 0. The two wmark levels are shown below
06h	/70074h	**DISPLAY_CONTROLLER.FW5:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.
06h	/70078h	**DISPLAY_CONTROLLER.FW6:** These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.
06h	/70080h	**DISPLAY_CONTROLLER.CURACNTR:** This register and all other cursor registers will remain in their holding register readable after a write. The holding registers are transferred into the active registers on the asserting edge of Vertical Blank only after a write cycle to the base address register has completed. DevBLC and DevCTG For hires modes Cursor A is connected to pipe A only. For VGA popup it follows the VGA pipe select.
06h	/70084h	**DISPLAY_CONTROLLER.CURABASE:** This register specifies the graphics memory address at which the cursor image data is located. Writes to this register acts like a trigger that enables atomic updates of the cursor registers. When updating the cursor registers this register should be written last in the sequence. This register should be written even if the actual contents did not change to allow the holding registers to move to the active registers on the next VBLANK. For legacy cursor modes this register is sufficient to specify the address of the entire cursor. For ARGB modes this register specifies the address of the first page of the cursor data.
06h	/70088h	**DISPLAY_CONTROLLER.CURAPOS:** This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically requires that the base address be written and is double buffered.
06h	/7008Ch	**DISPLAY_CONTROLLER.CURARESV:**
06h	/70090h	**DISPLAY_CONTROLLER.CURAPALET:** These palette registers can be accessed through this MMIO interface register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. The two bit index selects one of the four colors or two of the colors when in the AND XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two bit index selects one of the four colors or two of the colors when in the AND XOR cursor mode.
06h	/700C0h	**DISPLAY_CONTROLLER.CURBCNTR:** The hardware cursor registers are memory mapped and accessible through 32 bit 16 bit or 8 bit accesses. They are all including the palette registers double buffered. Writes to cursor registers are done to a holding register. The actual register update will occur based on

Port	Reg/Mem	Description
		the assigned pipes VBLANK. It is recommended that the base register be accessed through a 32 bit write only. To update all cursor registers atomically a sequence that ends with a base address register write should be used. DevBLC and DevCTG Cursor B is connected to pipe B only.
06h	/700C4h	**DISPLAY_CONTROLLER.CURBBASE:** This register specifies the memory address at which the cursor data is located. Writes to this register should be done with 32 bit accesses and acts as a trigger to atomically update the cursor register set. For legacy cursor modes this register is sufficient to specify the address of the entire cursor. The address is the graphics address. For ARGB modes this register specifies the address of the first page of the cursor data.
06h	/700C8h	**DISPLAY_CONTROLLER.CURBPOS:** This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically and is double buffered. The load register is transferred into the active register on the leading edge of Vertical Blank of the pipe cursor is currently assigned after the trigger has been set.
06h	/700CCh	**DISPLAY_CONTROLLER.CURBRESV:**
06h	/700D0h	**DISPLAY_CONTROLLER.CURB_PALET:** These palette registers can be accessed through this MMIO interface or through a legacy mode using the VGA palette register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. In the two bit AND XOR cursor modes the two bit index selects one of the four colors or two of the colors when in the mode. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
06h	/7017Ch	**DISPLAY_CONTROLLER.DSPAADDR:**
06h	/70180h	**DISPLAY_CONTROLLER.DSPACNTR:** Notes The active set of registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls. If the currently selected pipe is disabled the update is immediate.
06h	/70184h	**DISPLAY_CONTROLLER.DSPALINOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync

Port	Reg/Mem	Description
		following the write.
06h	/70188h	**DISPLAY_CONTROLLER.DSPASTRIDE:**
06h	/70194h	**DISPLAY_CONTROLLER.DSPAKEYVAL:** This register specifies the key color to be used with the mask bits to determine if the display source data matches the key. This register will only have an effect when the display color key is enabled. The overlay destination key value is used for overlay keying when Display A is being used as a primary display with overlay destination keying enabled. This key can be used as a Display C destination key onto Display A.
06h	/70198h	**DISPLAY_CONTROLLER.DSPAKEYMSK:** This register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.
06h	/7019Ch	**DISPLAY_CONTROLLER.DSPASURF:**
06h	/701A4h	**DISPLAY_CONTROLLER.DSPATILEOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPALINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VBLANK only. A change to this register will take effect on the next vblank following the write.
06h	/701ACh	**DISPLAY_CONTROLLER.DSPASURFLIVE:**
06h	/70400h	**DISPLAY_CONTROLLER.CBR1:**
06h	/70404h	**DISPLAY_CONTROLLER.CBR2:**
06h	/70408h	**DISPLAY_CONTROLLER.CCBR:**
06h	/7040Ch	**DISPLAY_CONTROLLER.CBR3:**
06h	/71000h	**DISPLAY_CONTROLLER.PIPEB_DSLDISPLAY_SCAN_LINE :** This register enables the read back of the display pipe vertical line counter . The display line value is from the display pipe B timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation scan line zero is the first active line of the display. When in VGA centering mode the scan line 0 is the 1stactive scan line of the pseudo border not the centered active VGA image display area. In interlaced display timings the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Programming Note In order to cause the scan line logic to report the correct Line Counter value the corresponding Display Pipeline timing registers must be programmed to valid non zero e.g. 640x480 60Hz values

Port	Reg / Mem	Description
		before enabling the Pipe or programming VGA timing and enabling native VGA.
06h	/71004h	**DISPLAY_CONTROLLER.PIPEB_SLC:** The Start and End Line Count Compare registers are compared with the display line values from the timing generator. They change at the leading edge of HSYNC. They can safely be accessed at any time. The End compare register operator is a less than or equal while the Start compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts status and command stream flow control wait for within range and wait for not within range . For range check the value programmed should be the desired value 1. So for line 0 the value programmed is VTOTAL and for line 1 the value programmed is 0. This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands or through MMIO for DevBLC and DevCTG.
06h	/71008h	**DISPLAY_CONTROLLER.PIPEBCONF:**
06h	/71010h	**DISPLAY_CONTROLLER.PIPEBGCMAXRED:**
06h	/71014h	**DISPLAY_CONTROLLER.PIPEBGCMAXGREEN:**
06h	/71018h	**DISPLAY_CONTROLLER.PIPEBGCMAXBLUE:**
06h	/71024h	**DISPLAY_CONTROLLER.PIPEBSTAT:** Programming Prior to clearing a Display Pipe sourced interrupt e.g. Display Pipe A VBLANK in the IIR the corresponding interrupt source status in the PIPEASTAT or PIPEBSTAT register e.g. Pipe A VBLANK Interrupt Status bit of PIPEASTAT must first be cleared. Note that clearing these status bits requires writing a 1 to the appropriate bit position.
06h	/71040h	**DISPLAY_CONTROLLER.PIPEBFRAMEHIGH:**
06h	/71044h	**DISPLAY_CONTROLLER.PIPEBFRAMEPIXEL:**
06h	/71050h	**DISPLAY_CONTROLLER.PIPEBGMCHDATAM:**
06h	/71054h	**DISPLAY_CONTROLLER.PIPEBGMCHDATAN:**
06h	/71060h	**DISPLAY_CONTROLLER.PIPEBDPLINKM:**
06h	/71064h	**DISPLAY_CONTROLLER.PIPEBDPLINKN:**
06h	/7117Ch	**DISPLAY_CONTROLLER.DSPBADDR:**
06h	/71180h	**DISPLAY_CONTROLLER.DSPBCNTR:** The active set of registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls. If the currently selected pipe is disabled the update is immediate.
06h	/71184h	**DISPLAY_CONTROLLER.DSPBLINOFFSET:** This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear

Port	Reg/Mem	Description
		or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
06h	/71188h	**DISPLAY_CONTROLLER.DSPBSTRIDE:**
06h	/71194h	**DISPLAY_CONTROLLER.DSPBKEYVAL:** This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The overlay destination key value is used for overlay keying when Display B is being used as a secondary display with overlay destination keying enabled.
06h	/71198h	**DISPLAY_CONTROLLER.DSPBKEYMSK:** This register specifies the key mask to be used with the color value bits to determine if the sprite source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.
06h	/7119Ch	**DISPLAY_CONTROLLER.DSPBSURF:** Writing to this register triggers the display plane flip. When it is desired to change multiple display B registers this register should be written last as a write to this register will cause all new register values to take effect.
06h	/711A4h	**DISPLAY_CONTROLLER.DSPBTILEOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VBLANK only. A change to this register will take effect on the next vblank following the write.
06h	/711ACh	**DISPLAY_CONTROLLER.DSPBSURFLIVE:**
06h	/71200h	**DISPLAY_CONTROLLER.DSPBFLPQSTAT:**
06h	/71400h	**DISPLAY_CONTROLLER.VGACNTRL:** This register provides support for VGA compatibility modes. This register is used by video BIOS only.
06h	/72180h	**DISPLAY_CONTROLLER.DSPCCNTR:** The active set of basic control registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls with the exception of the

Port	Reg/Mem	Description
		Display C color control registers. If the currently selected pipe is disabled the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.
06h	/72184h	**DISPLAY_CONTROLLER.DSPCLINOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
06h	/72188h	**DISPLAY_CONTROLLER.DSPCSTRIDE:**
06h	/7218Ch	**DISPLAY_CONTROLLER.DSPCPOS:** These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display this should be set to the entire display rectangle.
06h	/72190h	**DISPLAY_CONTROLLER.DSPCSIZE:** This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the sprite is assigned to.
06h	/72194h	**DISPLAY_CONTROLLER.DSPCKEYMINVAL:** This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5 5 5 or 5 6 5 formats must be filled with duplicates of the three or two MSBs of the pixel value.
06h	/72198h	**DISPLAY_CONTROLLER.DSPCKEYMSK:**
06h	/7219Ch	**DISPLAY_CONTROLLER.DSPCSURF:** Writing to this register triggers the display plane flip. When it is desired to change multiple display C registers this register should be written last as a write to this register will cause all new register values to take effect.
06h	/721A0h	**DISPLAY_CONTROLLER.DSPCKEYMAXVAL:** This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.
06h	/721A4h	**DISPLAY_CONTROLLER.DSPCTILEOFF:** This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register and this

Port	Reg/Mem	Description
		register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.
06h	/721A8h	**DISPLAY_CONTROLLER.DSPCCONTALPHA:**
06h	/721D0h	**DISPLAY_CONTROLLER.DCLRC0:**
06h	/721D4h	**DISPLAY_CONTROLLER.DCLRC1:** The sum of the absolute value of SH_SIN and SH_COS must be limited to less than 8. ABS SH_SIN ABS SH_COS lt 8
06h	/721E0h	**DISPLAY_CONTROLLER.GAMC5:** Same as previous register.
06h	/721E4h	**DISPLAY_CONTROLLER.GAMC4:** Same as previous register.
06h	/721E8h	**DISPLAY_CONTROLLER.GAMC3:** Same as previous register.
06h	/721ECh	**DISPLAY_CONTROLLER.GAMC2:** Same as previous register.
06h	/721F0h	**DISPLAY_CONTROLLER.GAMC1:** Same as previous register.
06h	/721F4h	**DISPLAY_CONTROLLER.GAMC0:** These registers are used to determine the characteristics of the gamma correction for the display C pixel data pre blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points 0 and 1023 have fixed values 0 and 1023 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise screen artifacts may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U
06h	00h/	**GVD.ID:** D2: PCI Device and Vendor ID Register

Port	Reg/Mem	Description
06h	01h/	**GVD.PCICMDSTS:** PCI Command and Status Register
06h	020F4h/020F4h	**GVD.G_LP_CONTROL:** GVD LP Arbitration Control Register
06h	02h/	**GVD.RIDCC:** Revision Identification and Class Codes
06h	03h/	**GVD.HDR:** Header Type
06h	04h/	**GVD.MMADR:** Memory Mapped Address Range. This is the base address for all memory mapped registers.
06h	05h/	**GVD.GFX_IOBAR:** I/O Base Address. This is used only by SBIOS and is the base address for the MMIO_INDEX and MMIO_DATA registers.
06h	0Bh/	**GVD.SSID:** Subsystem Identifiers
06h	0Dh/	**GVD.CAPPOINT:** Capabilities Pointer
06h	0Fh/	**GVD.INTR:** Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver.
06h	14h/	**GVD.MGGC:** Graphics Control
06h	17h/	**GVD.BSM:** Base of Stolen Memory
06h	24h/	**GVD.MSI_CAPID:** Message Signaled Interrupts Capability ID and Control Register
06h	25h/	**GVD.MA:** Message Address
06h	26h/	**GVD.MD:** Message Data
06h	2Ch/	**GVD.VCID:** Vendor Capability ID
06h	2Dh/	**GVD.VC:** Vendor Capabilities
06h	31h/	**GVD.FD:** Functional Disable. This register is used by SBIOS, not by driver.
06h	34h/	**GVD.PMCAP:** Power Management Capabilities
06h	35h/	**GVD.PMCS:** Power Management Control/Status. Driver doesn't use this register. SBIOS doesn't use this register.
06h	38h/	**GVD.SWSMISCI:** Software SMI or SCI
06h	39h/	**GVD.ASLE:** System Display Event Register. SBIOS writes this register to generate an interrupt to the graphics/display driver.
06h	3Dh/	**GVD.LBB:** Legacy Backlight Brightness. The display driver in Lincroft does not use this register since ASLE is available.
06h	3Eh/	**GVD.MANUFACTURING_ID:** Manufacturing ID
06h	3Fh/	**GVD.ASLS:** ASL Storage. The Lincroft display driver does not need this register since memory Operational Region (OpRegion) is available. This register is kept for use as scratch space.
07h	00h/	**GVD.MMIO_INDEX:** GVD MMIO Index Register: A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed by the GMCH but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which

Port	Reg/Mem	Description
		are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver. This register must not be accessed via the IOSF bus and the message bus at the same time as the results will be unpredictable. Access through the message bus is only for save/restore and debug purposes.
07h	E0h/	**GVD.GMCH_PERF_EVTSEL0:** GMCH_PERF_EVTSEL0
07h	E1h/	**GVD.GMCH_PERF_EVTSEL1:** GMCH_PERF_EVTSEL1
07h	E2h/	**GVD.GMCH_PERF_EVTSEL2:** GMCH_PERF_EVTSEL2
07h	E3h/	**GVD.GMCH_PERF_EVTSEL3:** GMCH_PERF_EVTSEL3
08h	00h/	**ID:** D0: PCI Device ID and Vendor ID
08h	01h/	**PCI_STATUS_AND_PCI_COMMAND:**
08h	02h/	**CLASS_CODE_AND_REVISION_ID:** Class Code and Revision ID
08h	03h/	**BIST_HEADER_TYPE_AND_MASTER_LATENCY_TIMER_CACHELINE:** Header Type. Latency timer functionality
08h	0Bh/	**SSID:** SubsystemID
08h	35h/	**MESSAGESIDEBAND_DATA_REGISTER:** Message Data Register
08h	36h/	**SIDEBAND_PACKET_REGISTER_EXTENSION:** The Sideband Packet Register lacks the upper address or offset bits necessary to create some necessary transactions over IOSF sideband. This register is the home for those extensions. Its contents are used to fill in the upper address or offset bits of an IOSF sideband request and are cleared upon a write to the Sideband Packet Register.
08h	3Ch/	**SCRATCHPAD_REGISTER:** Scratchpad Register
08h	3Eh/	**MANUFACTURING_ID:** Manufacturing ID
08h	40h/	**C_LOCAL_CONTROL:** Local Control Mode
80h	0h/	**DMI.DMIVCECH_0_0_0_DMIBAR:** HASH(0x6afa30)Indicates DMI Virtual Channel capabilities.
80h	10h/	**DMI.DMIVC0RCAP_0_0_0_DMIBAR:** HASH(0x6afba0)DMI VC0 Resource Capability
80h	14h/	**DMI.DMIVC0RCTL_0_0_0_DMIBAR:** DOC .
80h	1ah/	**DMI.DMIVC0RSTS_0_0_0_DMIBAR:** HASH(0x6afcc0)DMI VC0 Resource Status
80h	1b0h/	**DMI.DMIETVM_0_0_0_DMIBAR:** DOC .
80h	1c0h/	**DMI.AERECH_0_0_0_DMIBAR:** HASH(0x6f6a90)The PCI Express Advanced Error Reporting (AER) capability is an optional extended capability. It has been implemented in this MCH, but may not be publicly exposed. If it is exposed, as controlled by the Capabilities List Control registers, the INTEL RESERVED note can be removed from all AER registers.

Port	Reg / Mem	Description
80h	1c4h/	**DMI.DMIUESTS_0_0_0_DMIBAR:** HASH(0x6f6af0)This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.
80h	1c8h/	**DMI.DMIUEMSK_0_0_0_DMIBAR:** HASH(0x6f6b90)
80h	1cch/	**DMI.DMIUESEV_0_0_0_DMIBAR:** HASH(0x6f6c30)Controls whether an individual error is reported as a non-fatal or fatal error. An error is reported as fatal when the corresponding error bit in the severity register is set. If the bit is cleared, the corresponding error is considered nonfatal.
80h	1ch/	**DMI.DMIVC1RCAP_0_0_0_DMIBAR:** HASH(0x6afd20)DMI VC1 Resource Capability
80h	1d0h/	**DMI.DMICESTS_0_0_0_DMIBAR:** HASH(0x6f8d40)This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation
80h	1d4h/	**DMI.DMICEMSK_0_0_0_DMIBAR:** HASH(0x6f8dd0)This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.
80h	1f8h/	**DMI.ECOBNSTLLL_0_0_0_DMIBAR:** DOC .
80h	1fch/	**DMI.ECOBNS_0_1_0_MMR:**
80h	200h/	**DMI.CFG_0_1_0_MMR:**
80h	204h/	**DMI.DMITC_0_0_0_DMIBAR:** DOC .
80h	208h/	**DMI.DMICC_0_0_0_DMIBAR:** HASH(0x6f8f80)
80h	20ch/	**DMI.DMIATM_0_0_0_DMIBAR:** HASH(0x6f8fe0)Address translation config
80h	20h/	**DMI.DMIVC1RCTL_0_0_0_DMIBAR:** DOC .
80h	210h/	**DMI.PSPC_0_1_0_MMR:**
80h	214h/	**DMI.DMISTS_0_0_0_DMIBAR:** HASH(0x6fae00)retry counters & link and lane status
80h	218h/	**DMI.DMISSTS_0_0_0_DMIBAR:** DOC .
80h	21ch/	**DMI.DMISSTSU_0_0_0_DMIBAR:** DOC .
80h	224h/	**DMI.LTSSMC_0_0_0_DMIBAR:**
80h	22ch/	**DMI.L0SLAT_0_0_0_DMIBAR:** HASH(0x6fb030)This register controls L0s Exit Latency for both Common and Non-Common clock configurations.
80h	230h/	**DMI.CMMPC_0_1_0_MMR:** control lane reversal , This register contains the control bits and status information for the CMM. Programming of this register must take place prior to Starting CMM (setting 230h[0]=1). ; ;
80h	234h/	**DMI.CMMSB_0_1_0_MMR:** This register contains the symbols that are transmitted on the link. Programming of this register must take place prior to Starting CMM (setting 230h[0]=1). This is an INTEL RESERVED register and should

Port	Reg / Mem	Description
		NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.
80h	238h/	**DMI.LLTC_0_0_0_DMIBAR:** DOC .
80h	250h/	**DMI.CFG2_0_1_0_MMR:**
80h	254h/	**DMI.CFG3_0_0_0_DMIBAR:** DOC .
80h	258h/	**DMI.CFG4_0_0_0_DMIBAR:** HASH(0x6d4d00)general CFG (interrupt A/b/c/d , enable debug alignment VDM ,clear Error poison downstream , downstream chain disable, vc1 Q size, L1 completion time out)
80h	26h/	**DMI.DMIVC1RSTS_0_0_0_DMIBAR:** HASH(0x6b1a70)DMI VC1 Resource Status
80h	28h/	**DMI.DMIVCPRCAP_0_0_0_DMIBAR:** HASH(0x6b1ac0)DMI VCp Resource Capability
80h	2ch/	**DMI.DMIVCPRCTL_0_0_0_DMIBAR:** DOC .
80h	300h/	**DMI.DMIVC0PRCC_0_0_0_DMIBAR:** HASH(0x6d4dd0)Total number of flow control units consumed by the local agent since initialization. These values are incremented when the Transaction Layer commits to sending information on the Link Layer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express
80h	304h/	**DMI.DMIVC0PRCL_0_0_0_DMIBAR:** HASH(0x6d4e20)Contains the limit for maximum number of flow control units which may be consumed by the local agent. Set to the value indicated in the Flow Control Packet upon receipt, which reflects the available space in the remote receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express
80h	308h/	**DMI.DMIVC0PRCA_0_0_0_DMIBAR:** HASH(0x6d4e90) Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification
80h	30ch/	**DMI.DMIVC0NPRCC_0_0_0_DMIBAR:** HASH(0x6d4f00)
80h	310h/	**DMI.DMIVC0NPRCL_0_0_0_DMIBAR:** Contains the limit for maximum number of flow control units which may be consumed by the local agent. Set to the value indicated in the Flow Control Packet upon receipt, which reflects the available space in the remote receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express
80h	314h/	**DMI.DMIVC0NPRCA_0_0_0_DMIBAR:** HASH(0x6d4fc0) Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are

Port	Reg / Mem	Description
		incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. For testing purposes a value can be written into this register that will be read only one time, when the PCI Express functionality is initialize
80h	318h/	**DMI.DMIVC0CCC_0_0_0_DMIBAR:** HASH(0x6d5010) Total number of flow control units consumed by the local agent since initialization. These values are incremented when the Transaction Layer commits to sending information on the Link Layer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express
80h	31ch/	**DMI.DMIVC0CCL_0_0_0_DMIBAR:** HASH(0x6d5060)
80h	320h/	**DMI.VC01CL_0_0_0_DMIBAR:** HASH(0x6d50d0) Contains the limit for maximum number of request transactions` fragments which may be chained for vc0 & vc1
80h	324h/	**DMI.VCPMCL_0_0_0_DMIBAR:** HASH(0x6d5140) Contains the limit for maximum number of request transactions` fragments which may be chained for vcp & vcm
80h	32ch/	**DMI.DMIVC1PRCA_0_0_0_DMIBAR:** HASH(0x6d51b0)DMI VC1 Posted Request Credits Allocated
80h	32h/	**DMI.DMIVCPRSTS_0_0_0_DMIBAR:** HASH(0x6b1bd0)DMI VCP Resource Status
80h	330h/	**DMI.DMIVC1NPRCA_0_0_0_DMIBAR:** HASH(0x6d5220)DMI VCm Non-Posted Request Credits Allocated
80h	334h/	**DMI.DMIVCPPRCA_0_0_0_DMIBAR:** HASH(0x6d5270)DMI VCp Posted Request Credits Allocated . Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. For testing purposes a value can be written into this register that will be read only one time, when the PCI Express functionality is initialized
80h	338h/	**DMI.DMIVCPNPRCA_0_0_0_DMIBAR:** HASH(0x6d52e0)Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. For testing purposes a value can be written into this register that will be read only one time, when the PCI Express functionality is initialized. After that this register can only be used for reading the current value. When reading the PCI Express
80h	344h/	**DMI.DMIVCMPRCA_0_0_0_DMIBAR:** HASH(0x6d5330)DMI VCm Posted Request Credits Allocated

Port	Reg / Mem	Description
80h	348h/	**DMI.DMIVCMNPRCA_0_0_0_DMIBAR:** HASH(0x6d53a0)DMI VCm Non-Posted Request Credits Allocated
80h	34h/	**DMI.DMIVCMRCAP_0_0_0_DMIBAR:** HASH(0x6b1c20)DMI VCm Resource Capability
80h	350h/	**DMI.VC01TP_0_0_0_DMIBAR:** HASH(0x6d53f0)VC0 and Vc1 transactions pending in TL queue
80h	354h/	**DMI.VCPMTP_0_0_0_DMIBAR:** HASH(0x6d5470)VCp and Vcm transactions pending in TL queue
80h	38h/	**DMI.DMIVCMRCTL_0_0_0_DMIBAR:** DOC .
80h	3eh/	**DMI.DMIVCMRSTS_0_0_0_DMIBAR:** HASH(0x6b1cf0)DMI VCM Resource Status
80h	40h/	**DMI.DMIRCLDECH_0_0_0_DMIBAR:** HASH(0x6b1d40)This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component. See PCI Express specification for link/topology declaration requirements.
80h	44h/	**DMI.DMIESD_0_0_0_DMIBAR:** HASH(0x6b1db0)Provides information about the root complex element containing this Link Declaration Capability.
80h	48h/	**DMI.VC01DATABUF_0_0_0_DMIBAR:** this CR controls the separation of the data memory allocated at the downstream of scl block
80h	4b8h/	**DMI.THERMALCTRL_0_1_0_MMR:** Thermal Throttling Controls , This register holds the counters values that force Tx entry to LOs
80h	4bch/	**DMI.PEGBDWTHCHGTO_0_1_0_MMR:** PEG should be removed
80h	4ch/	**DMI.VCPMDATABUF_0_0_0_DMIBAR:** this CR control the separation of the data memory allocated at the downstream to scl block
80h	4h/	**DMI.DMIPVCCAP1_0_0_0_DMIBAR:** HASH(0x6afa90)DMI Port VC Capability Register 1. Describes the configuration of PCI Express Virtual Channels associated with this port
80h	504h/	**DMI.FUSESCMN_0_1_0_MMR:**
80h	508h/	**DMI.TRNEN_0_1_0_MMR:**
80h	530h/	**DMI.PMTRL0_0_1_0_MMR:**
80h	534h/	**DMI.PMTRL0S_0_1_0_MMR:**
80h	538h/	**DMI.PTHERMCTL_0_1_0_MMR:**
80h	564h/	**DMI.CAPID0_B_0_1_0_MMR:**
80h	568h/	**DMI.CAPID0_ACMN_0_1_0_MMR:** Control of bits in this register are only required for customer visible SKU differentiation
80h	610h/	**RSVD**

Port	Reg / Mem	Description
80h	614h/	**RSVD**
80h	618h/	**RSVD**
80h	61ch/	**RSVD**
80h	620h/	**RSVD**
80h	624h/	**RSVD**
80h	68h/	**DMI.PMONDLMASK_0_0_0_DMIBAR:** this CR control the mask for the PMON - each field control separated counter
80h	70h/	**DMI.PMONTLMASK_0_0_0_DMIBAR:** this CR control the mask for the PMON - each field control separated counter
80h	80h/	**DMI.DMIRCILCECH_0_0_0_DMIBAR:** HASH(0x6c2630)This capability contains controls for the Root Complex Internal Link known as DMI
80h	814h/	**DMI.PSMICMS_0_1_0_MMR:**
80h	84h/	**DMI.LCAP_0_0_0_DMIBAR:**
80h	88h/	**DMI.LCTL_0_0_0_DMIBAR:** HASH(0x6de4f0)Allows control of PCI Express link.
80h	8h/	**DMI.DMIPVCCAP2_0_0_0_DMIBAR:** HASH(0x6afae0)DMI Port VC Capability Register 2. Describes the configuration of PCI Express Virtual Channels associated with this port.
80h	98h/	**DMI.LCTL2_0_0_0_DMIBAR:**
80h	bah/	**DMI.SLOTSTS_0_1_0_PCI:**
80h	ch/	**DMI.DMIPVCCTL_0_0_0_DMIBAR:** HASH(0x6afb40)DMI Port VC Control
80h	d04h/	**DMI.AFERTMG_0_1_0_MMR:**
80h	d08h/	**DMI.PEGSQSTAT_0_1_0_MMR:**
80h	d0ch/	**DMI.PEGTST_0_1_0_MMR:**
80h	d14h/	**DMI.DEBUP3_0_0_0_DMIBAR:**
80h	d18h/	**DMI.PEGTRANSLCGCTRL_0_1_0_MMR:**
80h	d1ch/	**DMI.PEGINITLCGCTR_0_1_0_MMR:** PEG should be removed
80h	d20h/	**DMI.PEGCOMLCGCTRL_0_1_0_MMR:**
80h	d24h/	**DMI.FCLKGTTLLL_0_0_0_DMIBAR:** does not effect rtl
80h	d28h/	**DMI.PCLKGTTLLL_0_0_0_DMIBAR:**
80h	d2ch/	**DMI.PEGCLKGTCMN_0_1_0_MMR:** PEG relate should be removed
80h	d2h/	**DMI.LSTS2_0_1_0_PCI:**
80h	d34h/	**DMI.PEGUPDNCFG_0_1_0_MMR:** PEG relate . should be removed
80h	d38h/	**DMI.PEGLATFIXCTL_0_1_0_MMR:**
80h	d68h/	**DMI.BGFCTL4_0_0_0_DMIBAR:**

Port	Reg/Mem	Description
80h	d6ch/	**DMI.BGFCTL1_0_0_0_DMIBAR:**
80h	d70h/	**DMI.BGFCTL2_0_0_0_DMIBAR:**
80h	d74h/	**DMI.BGFCTL3_0_0_0_DMIBAR:**
80h	d78h/	**DMI.NEGSTS_0_1_0_MMR:** Negotiation Status - expose the value of the partner speed/scramble/emphasis/N_FTS request
80h	d7ch/	**DMI.UPCFGSTS_0_1_0_MMR:** current width reached after up/down config & This field exposes the initial configuration width. ;
80h	d80h/	**DMI.LFSRSTS_0_1_0_MMR:**
80h	d84h/	**DMI.CCRPR_0_0_0_DMIBAR:**
80h	d88h/	**DMI.CCWPR_0_0_0_DMIBAR:**
80h	d8ch/	**DMI.CCCR_0_0_0_DMIBAR:**
80h	e04h/	**DMI.TOE0_0_1_0_MMR:**
80h	e08h/	**DMI.ROE0_0_1_0_MMR:**
80h	e4h/	**DMI.DEBUGPLU_0_1_0_PCI:**
80h	e8h/	**DMI.DEBUGTLLL1_0_0_0_DMIBAR:** DOC .
80h	f0h/	**DMI.DEBUGPL_0_0_0_DMIBAR:**
80h	f4h/	**DMI.DEBUGTLLL_0_0_0_DMIBAR:** HASH(0x6f4b80)PCI Express debug control that is not required by the PCI Express spec. Place debug control that is not defined until after VHDL freeze in the DEBUP1 register. This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.
80h	fch/	**DMI.DEBUGPL1_0_1_0_PCI:** This is an Intel Reserved register to be used for debug purposes
81h	00h/	**FUS.FUS_MSG_OVERRIDE_REG0:** Fuse override register0
81h	01h/	**FUS.FUS_MSG_OVERRIDE_REG1:** Fuse override register1
81h	02h/	**FUS.FUS_MSG_OVERRIDE_REG2:** Fuse override register2
81h	03h/	**FUS.FUS_MSG_OVERRIDE_REG3:** Fuse override register3
81h	04h/	**FUS.FUS_MSG_OVERRIDE_REG4:** Fuse override register4
81h	05h/	**FUS.FUS_MSG_OVERRIDE_REG5:** Fuse override register5
81h	06h/	**FUS.FUS_MSG_OVERRIDE_REG6:** Fuse override register6
81h	07h/	**FUS.FUS_MSG_OVERRIDE_REG7:** Fuse override register7
81h	08h/	**FUS.FUS_MSG_OVERRIDE_REG8:** Fuse override register8
81h	09h/	**FUS.FUS_MSG_OVERRIDE_REG9:** Fuse override register9
81h	0ah/	**FUS.FUS_MSG_OVERRIDE_REGA:** Fuse override registerA
81h	0bh/	**FUS.FUS_MSG_OVERRIDE_REGB:** Fuse override registerB
81h	0ch/	**FUS.FUS_MSG_OVERRIDE_REGC:** Fuse override registerC

Port	Reg/Mem	Description
81h	0dh/	**FUS.FUS_MSG_OVERRIDE_REGD:** Fuse override registerD
81h	0eh/	**FUS.FUS_MSG_OVERRIDE_REGE:** Fuse override registerE
81h	0fh/	**FUS.FUS_MSG_OVERRIDE_REGF:** Fuse override registerF
81h	10h/	**FUS.FUS_MSG_OVERRIDE_REG10:** Fuse override register 0x10
81h	11h/	**FUS.FUS_MSG_OVERRIDE_REG11:** Fuse override register 0x11
81h	12h/	**FUS.FUS_MSG_OVERRIDE_REG12:** Fuse override register 0x12
81h	13h/	**FUS.FUS_MSG_OVERRIDE_REG13:** Fuse override register 0x13
81h	14h/	**FUS.FUS_MSG_OVERRIDE_REG14:** Fuse override register 0x14
81h	15h/	**FUS.FUS_MSG_OVERRIDE_REG15:** Fuse override register 0x15
81h	16h/	**FUS.FUS_MSG_OVERRIDE_REG16:** Fuse override register 0x16
81h	17h/	**FUS.FUS_MSG_OVERRIDE_REG17:** Fuse override register 0x17
81h	18h/	**FUS.FUS_MSG_OVERRIDE_REG18:** Fuse override register 0x18
81h	20h/	**FUS.FUS_MSG_RD_REG0:** Fuse to unit read register 0
81h	21h/	**FUS.FUS_MSG_RD_REG1:** Fuse to unit read register 1
81h	22h/	**FUS.FUS_MSG_RD_REG2:** Fuse to unit read register 2
81h	23h/	**FUS.FUS_MSG_RD_REG3:** Fuse to unit read register 3
81h	24h/	**FUS.FUS_MSG_RD_REG4:** Fuse to unit read register 4
81h	25h/	**FUS.FUS_MSG_RD_REG5:** Fuse to unit read register 5
81h	26h/	**FUS.FUS_MSG_RD_REG6:** Fuse to unit read register 6
81h	27h/	**FUS.FUS_MSG_RD_REG7:** Fuse to unit read register 7
81h	28h/	**FUS.FUS_MSG_RD_REG8:** Fuse to unit read register 8
81h	29h/	**FUS.FUS_MSG_RD_REG9:** Fuse to unit read register 9
81h	2ah/	**FUS.FUS_MSG_RD_REG10:** Fuse to unit read register 10
81h	2bh/	**FUS.FUS_MSG_RD_REG11:** Fuse to unit read register 11
81h	2ch/	**FUS.FUS_MSG_RD_REG12:** Fuse to unit read register 12
81h	2dh/	**FUS.FUS_MSG_RD_REG13:** Fuse to unit read register 13
81h	2eh/	**FUS.FUS_MSG_RD_REG14:** Fuse to unit read register 14
81h	2fh/	**FUS.FUS_MSG_RD_REG15:** Fuse to unit read register 15
81h	30h/	**FUS.FUS_MSG_RD_REG16:** Fuse to unit read register 16
81h	31h/	**FUS.FUS_MSG_RD_REG17:** Fuse to unit read register 17

Port	Reg / Mem	Description
81h	32h/	**FUS.FUS_MSG_RD_REG18:** Fuse to unit read register 18
81h	33h/	**FUS.FUS_MSG_RD_REG19:** Fuse to unit read register 19
81h	34h/	**FUS.FUS_MSG_RD_REG20:** Fuse to unit read register 20
81h	35h/	**FUS.FUS_MSG_RD_REG21:** Fuse to unit read register 21
81h	36h/	**FUS.FUS_MSG_RD_REG22:** Fuse to unit read register 22
81h	37h/	**FUS.FUS_MSG_RD_REG23:** Fuse to unit read register 23
81h	38h/	**FUS.FUS_MSG_RD_REG24:** Fuse to unit read register 24
87h	0000h/	**DDRIO.DQ0_OBSCKEBBCTL:**
87h	0004h/	**DDRIO.DQ0_DLLTXCTL:**
87h	0008h/	**DDRIO.DQ0_DLLRXCTL:**
87h	000ch/	**DDRIO.DQ0_MDLLCTL:**
87h	0010h/	**DDRIO.DQ0_B0RXIOBUFCTL:**
87h	0014h/	**DDRIO.DQ0_B0VREFCTL:**
87h	0018h/	**DDRIO.DQ0_B0RXOFFSET0:**
87h	001ch/	**DDRIO.DQ0_B0RXOFFSET1:**
87h	0020h/	**DDRIO.DQ0_B1RXIOBUFCTL:**
87h	0024h/	**DDRIO.DQ0_B1VREFCTL:**
87h	0028h/	**DDRIO.DQ0_B1RXOFFSET1:**
87h	002ch/	**DDRIO.DQ0_B1RXOFFSET0:**
87h	0030h/	**DDRIO.DQ0_DFTCTL:**
87h	0034h/	**DDRIO.DQ0_DQTRAINSTS:**
87h	0038h/	**DDRIO.DQ0_DLLPICODER0B1:**
87h	003ch/	**DDRIO.DQ0_DLLPICODER0B0:**
87h	0040h/	**DDRIO.DQ0_DLLPICODER1B1:**
87h	0044h/	**DDRIO.DQ0_DLLPICODER1B0:**
87h	0048h/	**DDRIO.DQ0_DLLPICODER2B1:**
87h	004ch/	**DDRIO.DQ0_DLLPICODER2B0:**
87h	0050h/	**DDRIO.DQ0_DLLPICODER3B1:**
87h	0054h/	**DDRIO.DQ0_DLLPICODER3B0:**
87h	0058h/	**DDRIO.DQ0_RXDQSPICODEB1:**
87h	005ch/	**DDRIO.DQ0_RXDQSPICODEB0:**
87h	0060h/	**DDRIO.DQ0_RXDQPICODEB1R32:**
87h	0064h/	**DDRIO.DQ0_RXDQPICODEB1R10:**
87h	0068h/	**DDRIO.DQ0_RXDQPICODEB0R32:**
87h	006ch/	**DDRIO.DQ0_RXDQPICODEB0R10:**

Port	Reg / Mem	Description
87h	0070h/	**DDRIO.DQ0_PTRCTL0:**
87h	0074h/	**DDRIO.DQ0_PTRCTL1:**
87h	0078h/	**DDRIO.DQ0_DBCTL0:**
87h	007ch/	**DDRIO.DQ0_DBCTL1:**
87h	0080h/	**DDRIO.DQ0_LATCTL0_B0:**
87h	0084h/	**DDRIO.DQ0_LATCTL0_B1:**
87h	0088h/	**DDRIO.DQ0_LATCTL1:**
87h	008ch/	**DDRIO.DQ0_ONDURCTL_B0:**
87h	0090h/	**DDRIO.DQ0_ONDURCTL_B1:**
87h	0094h/	**DDRIO.DQ0_OVRCTL_B0:**
87h	0098h/	**DDRIO.DQ0_OVRCTL_B1:**
87h	009ch/	**DDRIO.DQ0_DQCTL:**
87h	00a0h/	**DDRIO.DQ0_RK2RKCHG_PTRCTRL_B0:**
87h	00a4h/	**DDRIO.DQ0_RK2RKCHG_PTRCTRL_B1:**
87h	00a8h/	**DDRIO.DQ0_RK2RKCTL:**
87h	00ach/	**DDRIO.DQ0_RK2RK_PTRCTL:**
87h	00b0h/	**DDRIO.DQ0_RK2RKLAT_B0:**
87h	00b4h/	**DDRIO.DQ0_RK2RKLAT_B1:**
87h	00b8h/	**DDRIO.DQ0_CLKALIGN_REG0:**
87h	00bch/	**DDRIO.DQ0_CLKALIGN_REG1:**
87h	00c0h/	**DDRIO.DQ0_CLKALIGN_REG2:**
87h	00c4h/	**DDRIO.DQ0_CLKALIGN_STS0:**
87h	00c8h/	**DDRIO.DQ0_CLKALIGN_STS1:**
87h	00cch/	**DDRIO.DQ0_COMPSLV_1_B0:**
87h	00d0h/	**DDRIO.DQ0_COMPSLV_1_B1:**
87h	00d4h/	**DDRIO.DQ0_COMPSLV_2_B0:**
87h	00d8h/	**DDRIO.DQ0_COMPSLV_2_B1:**
87h	00dch/	**DDRIO.DQ0_COMPSLV_3_B0:**
87h	00e0h/	**DDRIO.DQ0_COMPSLV_3_B1:**
87h	0800h/	**DDRIO.DQ1_OBSCKEBBCTL:**
87h	0804h/	**DDRIO.DQ1_DLLTXCTL:**
87h	0808h/	**DDRIO.DQ1_DLLRXCTL:**
87h	080ch/	**DDRIO.DQ1_MDLLCTL:**
87h	0810h/	**DDRIO.DQ1_B0RXIOBUFCTL:**
87h	0814h/	**DDRIO.DQ1_B0VREFCTL:**

Port	Reg / Mem	Description
87h	0818h/	**DDRIO.DQ1_B0RXOFFSET0:**
87h	081ch/	**DDRIO.DQ1_B0RXOFFSET1:**
87h	0820h/	**DDRIO.DQ1_B1RXIOBUFCTL:**
87h	0824h/	**DDRIO.DQ1_B1VREFCTL:**
87h	0828h/	**DDRIO.DQ1_B1RXOFFSET1:**
87h	082ch/	**DDRIO.DQ1_B1RXOFFSET0:**
87h	0830h/	**DDRIO.DQ1_DFTCTL:**
87h	0834h/	**DDRIO.DQ1_DQTRAINSTS:**
87h	0838h/	**DDRIO.DQ1_DLLPICODER0B1:**
87h	083ch/	**DDRIO.DQ1_DLLPICODER0B0:**
87h	0840h/	**DDRIO.DQ1_DLLPICODER1B1:**
87h	0844h/	**DDRIO.DQ1_DLLPICODER1B0:**
87h	0848h/	**DDRIO.DQ1_DLLPICODER2B1:**
87h	084ch/	**DDRIO.DQ1_DLLPICODER2B0:**
87h	0850h/	**DDRIO.DQ1_DLLPICODER3B1:**
87h	0854h/	**DDRIO.DQ1_DLLPICODER3B0:**
87h	0858h/	**DDRIO.DQ1_RXDQSPICODEB1:**
87h	085ch/	**DDRIO.DQ1_RXDQSPICODEB0:**
87h	0860h/	**DDRIO.DQ1_RXDQPICODEB1R32:**
87h	0864h/	**DDRIO.DQ1_RXDQPICODEB1R10:**
87h	0868h/	**DDRIO.DQ1_RXDQPICODEB0R32:**
87h	086ch/	**DDRIO.DQ1_RXDQPICODEB0R10:**
87h	0870h/	**DDRIO.DQ1_PTRCTL0:**
87h	0874h/	**DDRIO.DQ1_PTRCTL1:**
87h	0878h/	**DDRIO.DQ1_DBCTL0:**
87h	087ch/	**DDRIO.DQ1_DBCTL1:**
87h	0880h/	**DDRIO.DQ1_LATCTL0_B0:**
87h	0884h/	**DDRIO.DQ1_LATCTL0_B1:**
87h	0888h/	**DDRIO.DQ1_LATCTL1:**
87h	088ch/	**DDRIO.DQ1_ONDURCTL_B0:**
87h	0890h/	**DDRIO.DQ1_ONDURCTL_B1:**
87h	0894h/	**DDRIO.DQ1_OVRCTL_B0:**
87h	0898h/	**DDRIO.DQ1_OVRCTL_B1:**
87h	089ch/	**DDRIO.DQ1_DQCTL:**
87h	08a0h/	**DDRIO.DQ1_RK2RKCHG_PTRCTRL_B0:**

Port	Reg / Mem	Description
87h	08a4h/	**DDRIO.DQ1_RK2RKCHG_PTRCTRL_B1:**
87h	08a8h/	**DDRIO.DQ1_RK2RKCTL:**
87h	08ach/	**DDRIO.DQ1_RK2RK_PTRCTL:**
87h	08b0h/	**DDRIO.DQ1_RK2RKLAT_B0:**
87h	08b4h/	**DDRIO.DQ1_RK2RKLAT_B1:**
87h	08b8h/	**DDRIO.DQ1_CLKALIGN_REG0:**
87h	08bch/	**DDRIO.DQ1_CLKALIGN_REG1:**
87h	08c0h/	**DDRIO.DQ1_CLKALIGN_REG2:**
87h	08c4h/	**DDRIO.DQ1_CLKALIGN_STS0:**
87h	08c8h/	**DDRIO.DQ1_CLKALIGN_STS1:**
87h	08cch/	**DDRIO.DQ1_COMPSLV_1_B0:**
87h	08d0h/	**DDRIO.DQ1_COMPSLV_1_B1:**
87h	08d4h/	**DDRIO.DQ1_COMPSLV_2_B0:**
87h	08d8h/	**DDRIO.DQ1_COMPSLV_2_B1:**
87h	08dch/	**DDRIO.DQ1_COMPSLV_3_B0:**
87h	08e0h/	**DDRIO.DQ1_COMPSLV_3_B1:**
87h	1000h/	**DDRIO.DQ2_OBSCKEBBCTL:**
87h	1004h/	**DDRIO.DQ2_DLLTXCTL:**
87h	1008h/	**DDRIO.DQ2_DLLRXCTL:**
87h	100ch/	**DDRIO.DQ2_MDLLCTL:**
87h	1010h/	**DDRIO.DQ2_B0RXIOBUFCTL:**
87h	1014h/	**DDRIO.DQ2_B0VREFCTL:**
87h	1018h/	**DDRIO.DQ2_B0RXOFFSET0:**
87h	101ch/	**DDRIO.DQ2_B0RXOFFSET1:**
87h	1020h/	**DDRIO.DQ2_B1RXIOBUFCTL:**
87h	1024h/	**DDRIO.DQ2_B1VREFCTL:**
87h	1028h/	**DDRIO.DQ2_B1RXOFFSET1:**
87h	102ch/	**DDRIO.DQ2_B1RXOFFSET0:**
87h	1030h/	**DDRIO.DQ2_DFTCTL:**
87h	1034h/	**DDRIO.DQ2_DQTRAINSTS:**
87h	1038h/	**DDRIO.DQ2_DLLPICODER0B1:**
87h	103ch/	**DDRIO.DQ2_DLLPICODER0B0:**
87h	1040h/	**DDRIO.DQ2_DLLPICODER1B1:**
87h	1044h/	**DDRIO.DQ2_DLLPICODER1B0:**
87h	1048h/	**DDRIO.DQ2_DLLPICODER2B1:**

Port	Reg / Mem	Description
87h	104ch/	**DDRIO.DQ2_DLLPICODER2B0:**
87h	1050h/	**DDRIO.DQ2_DLLPICODER3B1:**
87h	1054h/	**DDRIO.DQ2_DLLPICODER3B0:**
87h	1058h/	**DDRIO.DQ2_RXDQSPICODEB1:**
87h	105ch/	**DDRIO.DQ2_RXDQSPICODEB0:**
87h	1060h/	**DDRIO.DQ2_RXDQPICODEB1R32:**
87h	1064h/	**DDRIO.DQ2_RXDQPICODEB1R10:**
87h	1068h/	**DDRIO.DQ2_RXDQPICODEB0R32:**
87h	106ch/	**DDRIO.DQ2_RXDQPICODEB0R10:**
87h	1070h/	**DDRIO.DQ2_PTRCTL0:**
87h	1074h/	**DDRIO.DQ2_PTRCTL1:**
87h	1078h/	**DDRIO.DQ2_DBCTL0:**
87h	107ch/	**DDRIO.DQ2_DBCTL1:**
87h	1080h/	**DDRIO.DQ2_LATCTL0_B0:**
87h	1084h/	**DDRIO.DQ2_LATCTL0_B1:**
87h	1088h/	**DDRIO.DQ2_LATCTL1:**
87h	108ch/	**DDRIO.DQ2_ONDURCTL_B0:**
87h	1090h/	**DDRIO.DQ2_ONDURCTL_B1:**
87h	1094h/	**DDRIO.DQ2_OVRCTL_B0:**
87h	1098h/	**DDRIO.DQ2_OVRCTL_B1:**
87h	109ch/	**DDRIO.DQ2_DQCTL:**
87h	10a0h/	**DDRIO.DQ2_RK2RKCHG_PTRCTRL_B0:**
87h	10a4h/	**DDRIO.DQ2_RK2RKCHG_PTRCTRL_B1:**
87h	10a8h/	**DDRIO.DQ2_RK2RKCTL:**
87h	10ach/	**DDRIO.DQ2_RK2RK_PTRCTL:**
87h	10b0h/	**DDRIO.DQ2_RK2RKLAT_B0:**
87h	10b4h/	**DDRIO.DQ2_RK2RKLAT_B1:**
87h	10b8h/	**DDRIO.DQ2_CLKALIGN_REG0:**
87h	10bch/	**DDRIO.DQ2_CLKALIGN_REG1:**
87h	10c0h/	**DDRIO.DQ2_CLKALIGN_REG2:**
87h	10c4h/	**DDRIO.DQ2_CLKALIGN_STS0:**
87h	10c8h/	**DDRIO.DQ2_CLKALIGN_STS1:**
87h	10cch/	**DDRIO.DQ2_COMPSLV_1_B0:**
87h	10d0h/	**DDRIO.DQ2_COMPSLV_1_B1:**
87h	10d4h/	**DDRIO.DQ2_COMPSLV_2_B0:**

Port	Reg / Mem	Description
87h	10d8h/	**DDRIO.DQ2_COMPSLV_2_B1:**
87h	10dch/	**DDRIO.DQ2_COMPSLV_3_B0:**
87h	10e0h/	**DDRIO.DQ2_COMPSLV_3_B1:**
87h	1800h/	**DDRIO.DQ3_OBSCKEBBCTL:**
87h	1804h/	**DDRIO.DQ3_DLLTXCTL:**
87h	1808h/	**DDRIO.DQ3_DLLRXCTL:**
87h	180ch/	**DDRIO.DQ3_MDLLCTL:**
87h	1810h/	**DDRIO.DQ3_B0RXIOBUFCTL:**
87h	1814h/	**DDRIO.DQ3_B0VREFCTL:**
87h	1818h/	**DDRIO.DQ3_B0RXOFFSET0:**
87h	181ch/	**DDRIO.DQ3_B0RXOFFSET1:**
87h	1820h/	**DDRIO.DQ3_B1RXIOBUFCTL:**
87h	1824h/	**DDRIO.DQ3_B1VREFCTL:**
87h	1828h/	**DDRIO.DQ3_B1RXOFFSET1:**
87h	182ch/	**DDRIO.DQ3_B1RXOFFSET0:**
87h	1830h/	**DDRIO.DQ3_DFTCTL:**
87h	1834h/	**DDRIO.DQ3_DQTRAINSTS:**
87h	1838h/	**DDRIO.DQ3_DLLPICODER0B1:**
87h	183ch/	**DDRIO.DQ3_DLLPICODER0B0:**
87h	1840h/	**DDRIO.DQ3_DLLPICODER1B1:**
87h	1844h/	**DDRIO.DQ3_DLLPICODER1B0:**
87h	1848h/	**DDRIO.DQ3_DLLPICODER2B1:**
87h	184ch/	**DDRIO.DQ3_DLLPICODER2B0:**
87h	1850h/	**DDRIO.DQ3_DLLPICODER3B1:**
87h	1854h/	**DDRIO.DQ3_DLLPICODER3B0:**
87h	1858h/	**DDRIO.DQ3_RXDQSPICODEB1:**
87h	185ch/	**DDRIO.DQ3_RXDQSPICODEB0:**
87h	1860h/	**DDRIO.DQ3_RXDQPICODEB1R32:**
87h	1864h/	**DDRIO.DQ3_RXDQPICODEB1R10:**
87h	1868h/	**DDRIO.DQ3_RXDQPICODEB0R32:**
87h	186ch/	**DDRIO.DQ3_RXDQPICODEB0R10:**
87h	1870h/	**DDRIO.DQ3_PTRCTL0:**
87h	1874h/	**DDRIO.DQ3_PTRCTL1:**
87h	1878h/	**DDRIO.DQ3_DBCTL0:**
87h	187ch/	**DDRIO.DQ3_DBCTL1:**

Port	Reg/Mem	Description
87h	1880h/	**DDRIO.DQ3_LATCTL0_B0:**
87h	1884h/	**DDRIO.DQ3_LATCTL0_B1:**
87h	1888h/	**DDRIO.DQ3_LATCTL1:**
87h	188ch/	**DDRIO.DQ3_ONDURCTL_B0:**
87h	1890h/	**DDRIO.DQ3_ONDURCTL_B1:**
87h	1894h/	**DDRIO.DQ3_OVRCTL_B0:**
87h	1898h/	**DDRIO.DQ3_OVRCTL_B1:**
87h	189ch/	**DDRIO.DQ3_DQCTL:**
87h	18a0h/	**DDRIO.DQ3_RK2RKCHG_PTRCTRL_B0:**
87h	18a4h/	**DDRIO.DQ3_RK2RKCHG_PTRCTRL_B1:**
87h	18a8h/	**DDRIO.DQ3_RK2RKCTL:**
87h	18ach/	**DDRIO.DQ3_RK2RK_PTRCTL:**
87h	18b0h/	**DDRIO.DQ3_RK2RKLAT_B0:**
87h	18b4h/	**DDRIO.DQ3_RK2RKLAT_B1:**
87h	18b8h/	**DDRIO.DQ3_CLKALIGN_REG0:**
87h	18bch/	**DDRIO.DQ3_CLKALIGN_REG1:**
87h	18c0h/	**DDRIO.DQ3_CLKALIGN_REG2:**
87h	18c4h/	**DDRIO.DQ3_CLKALIGN_STS0:**
87h	18c8h/	**DDRIO.DQ3_CLKALIGN_STS1:**
87h	18cch/	**DDRIO.DQ3_COMPSLV_1_B0:**
87h	18d0h/	**DDRIO.DQ3_COMPSLV_1_B1:**
87h	18d4h/	**DDRIO.DQ3_COMPSLV_2_B0:**
87h	18d8h/	**DDRIO.DQ3_COMPSLV_2_B1:**
87h	18dch/	**DDRIO.DQ3_COMPSLV_3_B0:**
87h	18e0h/	**DDRIO.DQ3_COMPSLV_3_B1:**
87h	4800h/	**DDRIO.CMD_OBSCKEBBCTL:**
87h	4804h/	**DDRIO.CMD_RES0:**
87h	4808h/	**DDRIO.CMD_DLLTXCTL:**
87h	480ch/	**DDRIO.CMD_DLLRXCTL:**
87h	4810h/	**DDRIO.CMD_MDLLCTL:**
87h	4814h/	**DDRIO.CMD_RCOMP_ODT:**
87h	4820h/	**DDRIO.CMD_DLLPICODER0:**
87h	4824h/	**DDRIO.CMD_DLLPICODER1:**
87h	4828h/	**DDRIO.CMD_RES4:**
87h	482ch/	**DDRIO.CMD_RES5:**

Port	Reg / Mem	Description
87h	4830h/	**DDRIO.CMD_RES6:**
87h	4834h/	**DDRIO.CMD_RES7:**
87h	4838h/	**DDRIO.CMD_RES8:**
87h	4840h/	**DDRIO.CMD_CFG_REG0:**
87h	4844h/	**DDRIO.CMD_POINTER_REG:**
87h	4848h/	**DDRIO.CMD_RESERVED0:**
87h	484ch/	**DDRIO.CMD_RESERVED1:**
87h	4850h/	**DDRIO.CMD_CLKALIGN_REG0:**
87h	4854h/	**DDRIO.CMD_CLKALIGN_REG1:**
87h	4858h/	**DDRIO.CMD_CLKALIGN_REG2:**
87h	485ch/	**DDRIO.CMD_PM_CONFIG0:**
87h	4860h/	**DDRIO.CMD_PM_DLYREG0:**
87h	4864h/	**DDRIO.CMD_PM_DLYREG1:**
87h	4868h/	**DDRIO.CMD_PM_DLYREG2:**
87h	486ch/	**DDRIO.CMD_PM_DLYREG3:**
87h	4870h/	**DDRIO.CMD_PM_DLYREG4:**
87h	4874h/	**DDRIO.CMD_CLKALIGN_STS0:**
87h	4878h/	**DDRIO.CMD_CLKALIGN_STS1:**
87h	487ch/	**DDRIO.CMD_PM_STS0:**
87h	4880h/	**DDRIO.CMD_PM_STS1:**
87h	4884h/	**DDRIO.CMD_COMPSLV:**
87h	4888h/	**DDRIO.CMD_VISA:**
87h	488ch/	**DDRIO.CMD_BONUSCMD0_IO:**
87h	4890h/	**DDRIO.CMD_BONUSCMD1_IO:**
87h	5800h/	**DDRIO.CLKCTL_OBSCKEBBCTL:**
87h	5804h/	**DDRIO.CLKCTL_RCOMP_IO:**
87h	5808h/	**DDRIO.CLKCTL_DLLTXCTL:**
87h	580ch/	**DDRIO.CLKCTL_DLLRXCTL:**
87h	5810h/	**DDRIO.CLKCTL_MDLLCTL:**
87h	5814h/	**DDRIO.CLKCTL_RCOMP_ODT:**
87h	5818h/	**DDRIO.CLKCTL_RES2:**
87h	581ch/	**DDRIO.CLKCTL_RES3:**
87h	5820h/	**DDRIO.CLKCTL_DLLPICODER0:**
87h	5824h/	**DDRIO.CLKCTL_DLLPICODER1:**
87h	5828h/	**DDRIO.CLKCTL_RES4:**

Port	Reg / Mem	Description
87h	582ch/	**DDRIO.CLKCTL_RES5:**
87h	5830h/	**DDRIO.CLKCTL_DDR3RESETCTL:**
87h	5834h/	**DDRIO.CLKCTL_RES7:**
87h	5838h/	**DDRIO.CLKCTL_CFG_REG0:**
87h	5840h/	**DDRIO.CLKCTL_CFG_REG1:**
87h	5844h/	**DDRIO.CLKCTL_POINTER_REG:**
87h	5848h/	**DDRIO.CLKCTL_RESERVED0:**
87h	584ch/	**DDRIO.CLKCTL_RESERVED1:**
87h	5850h/	**DDRIO.CLKCTL_CLKALIGN_REG0:**
87h	5854h/	**DDRIO.CLKCTL_CLKALIGN_REG1:**
87h	5858h/	**DDRIO.CLKCTL_CLKALIGN_REG2:**
87h	585ch/	**DDRIO.CLKCTL_PM_CONFIG0:**
87h	5860h/	**DDRIO.CLKCTL_PM_DLYREG0:**
87h	5864h/	**DDRIO.CLKCTL_PM_DLYREG1:**
87h	5868h/	**DDRIO.CLKCTL_PM_DLYREG2:**
87h	586ch/	**DDRIO.CLKCTL_PM_DLYREG3:**
87h	5870h/	**DDRIO.CLKCTL_PM_DLYREG4:**
87h	5874h/	**DDRIO.CLKCTL_CLKALIGN_STS0:**
87h	5878h/	**DDRIO.CLKCTL_CLKALIGN_STS1:**
87h	587ch/	**DDRIO.CLKCTL_PM_STS0:**
87h	5880h/	**DDRIO.CLKCTL_PM_STS1:**
87h	5884h/	**DDRIO.CLKCTL_COMPSLV_1:**
87h	5888h/	**DDRIO.CLKCTL_COMPSLV_2:**
87h	588ch/	**DDRIO.CLKCTL_COMPSLV_3:**
87h	5890h/	**DDRIO.CLKCTL_VISA:**
87h	5894h/	**DDRIO.CLKCTL_BONUSCTL_IO:**
87h	5898h/	**DDRIO.CLKCTL_BONUSCLK_IO:**
87h	7800h/	**DDRIO.PLL_MPLLCTRL:**
87h	7810h/	**DDRIO.PLL_MPLLCSR0:**
87h	7814h/	**DDRIO.PLL_MPLLCSR1:**
87h	7820h/	**DDRIO.PLL_MPLLCSR2:**
87h	7828h/	**DDRIO.PLL_MPLLDFT:**
87h	7830h/	**DDRIO.PLL_MPLLMONCTL:**
87h	7838h/	**DDRIO.PLL_MPLLMON1CTL:**
87h	783ch/	**DDRIO.PLL_MPLLMON2CTL:**

Port	Reg/Mem	Description
87h	7850h/	**DDRIO.PLL_SFRTRIM:**
87h	7858h/	**DDRIO.PLL_MPLLDFTOUT:**
87h	785ch/	**DDRIO.PLL_MPLLDFTOUT1:**
87h	7860h/	**DDRIO.PLL_RES1:**
87h	7864h/	**DDRIO.PLL_RES2:**
87h	7868h/	**DDRIO.PLL_RES3:**
87h	786ch/	**DDRIO.PLL_RES4:**
87h	7870h/	**DDRIO.PLL_RES5:**
87h	7874h/	**DDRIO.PLL_RES6:**
87h	7878h/	**DDRIO.PLL_RES7:**
87h	787ch/	**DDRIO.PLL_RES8:**
87h	7880h/	**DDRIO.PLL_MASTERRSTN:**
87h	7884h/	**DDRIO.PLL_PLLLOCKDEL:**
87h	7888h/	**DDRIO.PLL_SFRDEL:**
87h	78C0h/	**DDRIO.PLL_OBSCTRL:**
87h	78f0h/	**DDRIO.PLL_VISACTRL0:**
87h	78f4h/	**DDRIO.PLL_VISACTRL1:**
87h	78f8h/	**DDRIO.PLL_VISACTRL2:**
87h	78fch/	**DDRIO.PLL_VISACTRL3:**
89h	0h/	**GPIO.IODFXSpeed:**
89h	1h/	**GPIO.IOMuxGRP0Control:**
89h	2h/	**GPIO.IOMuxGRP1Control:**
89h	3h/	**GPIO.RCOMPOverideDataReg:**
89h	4h/	**GPIO.IOProbe:**
89h	5h/	**GPIO.IOhfpll:**
89h	6h/	**GPIO.IOStrapRead:**
89h	7h/	**GPIO.GPIOMVRCOMPConfig0:**
89h	8h/	**GPIO.GPIOMVRCOMPConfig3:**
89h	9h/	**GPIO.GPIOHVRCOMPConfig0:**
89h	ah/	**GPIO.GPIOHVRCOMPConfig3:**
89h	bh/	**GPIO.GPIOPadConfig0:**
89h	ch/	**GPIO.GPIOLVPadConfig1:**

1.11 Intel Atom Processor D2000 series and N2000 Series Full Register List

1.11.1 AEC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 00h/0h/
MMIO: Base/Offset:
IO: Base/Offset:

IOSF primary channel router" Enhanced Configuration Space ; CDVThe Lincroft SCH supports PCI Express enhanced configuration space, which is mapped into PCI memory space at a 256Mbyte offset given by the upper four bits of the AEC register

Bit	Access	Default Value	Description
31:28	RW	0h	**ECBase:** NOTE: "Processor Interface" HECREG[31:28] need to be same as "IOSF primary channel router" AEC[31:28]... When ECBase matches the upper four bits of a system memory address (under 4G) that has been forwarded to the "IOSF primary channel router" and enhanced configuration operations are enabled, the corresponding operation is treated as an enhanced configuration space access .
27:1	RO	0h	**RESERVED:**
0	RW	0b	**ECEnable:** NOTE: "Processor Interface" HECREG[0] need to be same as "IOSF primary channel router" AEC[0]... enables enhanced configuration operation

1.11.2 BEMON0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 03h/E0h/
MMIO: Base/Offset:
IO: Base/Offset:

EMON Control register for counter 0

Bit	Access	Default Value	Description
31:23	RO	0h	**RESERVED:**
22	RW	0h	**EMON_ENABLE:** Enable Emon
21:17	RO	0h	**RESERVED1:**
16:8	RW	0h	**BEMON0_EventMask:** Event Mask for Event counter 0
7:5	RO	0h	**RESERVED2:**
4:0	RW	00h	**BEMON0_EventID:** Event ID for Event counter 0. Only bits 3:0 are used in "DRAM buffering and arbitration unit".

1.11.3 BEMON1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 03h/E1h/
MMIO: Base/Offset:
IO: Base/Offset:

EMON Control register for counter 1

Bit	Access	Default Value	Description
31:23	RO	0h	**RESERVED:**
22	RW	0h	**EMON_ENABLE:** Enable Emon
21:17	RO	0h	**RESERVED1:**
20:8	RW	0h	**BEMON1_EventMask:** Event Mask for Event counter 1
7:5	RO	0h	**RESERVED2:**
4:0	RW	00h	**BEMON1_EventID:** Event ID for Event counter 1. Only bits 3:0 are used in “DRAM buffering and arbitration unit”.

1.11.4 BEMON2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 03h/E2h/
MMIO: Base/Offset:
IO: Base/Offset:

EMON Control register for counter 2

Bit	Access	Default Value	Description
31:23	RO	0h	**RESERVED:**
22	RW	0h	**EMON_ENABLE:** Enable Emon
21:17	RO	0h	**RESERVED1:**
20:8	RW	0h	**BEMON2_EventMask:** Event Mask for Event counter 2
7:5	RO	0h	**RESERVED2:**
4:0	RW	00h	**BEMON2_EventID:** Event ID for Event counter 2. Only bits 3:0 are used in “DRAM buffering and arbitration unit”.

1.11.5 BEMON3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 03h/E3h/
MMIO: Base/Offset:
IO: Base/Offset:

EMON Control register for counter 3

Bit	Access	Default Value	Description
31:23	RO	0h	**RESERVED:**
22	RW	0h	**EMON_ENABLE:** Enable Emon
21:17	RO	0h	**RESERVED1:**
20:8	RW	0h	**BEMON3_EventMask:** Event Mask for Event counter 3
7:5	RO	0h	**RESERVED2:**
4:0	RW	00h	**BEMON3_EventID:** Event ID for Event counter 3. Only bits 3:0 are used in “DRAM buffering and arbitration unit”.

1.11.6 BIST_HEADER_TYPE_AND_MASTER_LATENCY_TIMER_CACHELINE

PCI: B/D/F/Reg: 0/0/0/0Ch
SBI: Port/Reg/Mem: 08h/03h/
MMIO: Base/Offset:
IO: Base/Offset:

Header Type. Latency timer functionality

Bit	Access	Default Value	Description
31:24	RO	0b	**PCI_BIST:** Hardwired to 0 standard value for no PCI BIST
23:16	RO	00h	**PCI_HEADER_TYPE:** Hardwired to 8'h00 standard value for PCI type 0 header
15:8	RO	00h	**PCI_LATENCY_TIMER:** Hardwired to 8'h00.
7:0	RO	00h	**PCI_CACHELINE_SIZE:** Hardwired to 8'h00.

1.11.7 CLASS_CODE_AND_REVISION_ID

PCI: B/D/F/Reg: 0/0/0/08h
SBI: Port/Reg/Mem: 08h/02h/
MMIO: Base/Offset:
IO: Base/Offset:

Class Code and Revision ID

Bit	Access	Default Value	Description
31:8	RO	060000h	**CLASS_CODE:** Hardwired to {060000h
7:0	RO	strapRID[7:0]	**REVISION_ID:** Hardwired to { strapRID[7:0]

1.11.8 ID

PCI: B/D/F/Reg: 0/0/0/00h
SBI: Port/Reg/Mem: 08h/00h/
MMIO: Base/Offset:
IO: Base/Offset:

D0: PCI Device ID and Vendor ID

Bit	Access	Default Value	Description
31:16	RO	{ {0000_1011_1111_0b, fus_ncl_fuses_bus_zcznfwh[2:0]} }	**DEVICE_IDENTIFICATION_NUMBER:** DID: Identifier assigned to the Device 0 Host Bridge PCI device. The lower 3 bits of this register are determined by fuse fus_HostDevID_nczfwoh and the upper 13 bits are strapped at the Lincroft top level.
15:0	RO	8086h	**VENDOR_IDENTIFICATION_NUMBER:** VID: PCI standard identification for Intel.

1.11.9 MANUFACTURING_ID

PCI: B/D/F/Reg: 0/0/0/F8h
SBI: Port/Reg/Mem: 08h/3Eh/
MMIO: Base/Offset:
IO: Base/Offset:

Manufacturing ID

Bit	Access	Default Value	Description
31:24	RO	00h	**RESERVED:** Hardwired to the reset value.
23:0	RO	From straps	**MANUFACTURING_ID:** Hardwired to strapMANID[23:0].

1.11.10 MESSAGESIDEBAND_DATA_REGISTER

PCI: B/D/F/Reg: 0/0/0/D4h
SBI: Port/Reg/Mem: 08h/35h/
MMIO: Base/Offset:
IO: Base/Offset:

Message Data Register

Bit	Access	Default Value	Description
31:0	RW	00000000h	**MESSAGE_DATA_REGISTER:** MDR: If the MCR is programmed with a message bus register write command, then the contents of the MDR are used as the write data. The MDR must be written before the MCR is written with a message bus register write command. If the MCR is programmed with a message bus register read command, then the read return data is placed in the MDR. The MDR register can be read by the host after the MCR is written with a message bus register read command.

1.11.11 MESSAGE_CONTROLSIDEBAND_PACKET_REGISTER

PCI: B/D/F/Reg: 0/0/0/D0h
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset:

Message ControlSideband Packet Register

Bit	Access	Default Value	Description
31:0	WO	N/A	**MESSAGE_CONTROL_REGISTER:** MCR: This is not a real register. A write access to this address location causes a message to be sent through the M unit. ; Bits 31:24 = message bus opcode. ; Bits 23:16 = message bus port. ; Bits 15:8 = message bus address. ; Bits 3:0 = message bus byte enables.

1.11.12 PCI_STATUS_AND_PCI_COMMAND

PCI: B/D/F/Reg: 0/0/0/04h
SBI: Port/Reg/Mem: 08h/01h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO	00000007h	**PCI_STATUS_AND_PCI_COMMAND:** Hardwired to 32'h00000007

1.11.13 SCRATCHPAD_REGISTER

PCI: B/D/F/Reg: 0/0/0/F0h
SBI: Port/Reg/Mem: 08h/3Ch/
MMIO: Base/Offset:
IO: Base/Offset:

Scratchpad Register

Bit	Access	Default Value	Description
31:0	RW	00000000h	**SCRATCHPAD_REGISTER:** Spare bits

1.11.14 SIDEBAND_PACKET_REGISTER_EXTENSION

PCI: B/D/F/Reg: 0/0/0/D8h
SBI: Port/Reg/Mem: 08h/36h/
MMIO: Base/Offset:
IO: Base/Offset:

The Sideband Packet Register lacks the upper address or offset bits necessary to create some necessary transactions over IOSF sideband. This register is the home for those extensions. Its contents are used to fill in the upper address or offset bits of an IOSF sideband request and are cleared upon a write to the Sideband Packet Register.

Bit	Access	Default Value	Description
31:8	WO	N/A	**SIDEBAND_ADDRESS_EXTENSION:** Bits 31:8 of the transaction to be created when a write to configuration register 0xD0 is executed. The contents of this register field is cleared at the conclusion of a configuration write to 0xD0.
7:0	RO	00h	**RESERVED:**

1.11.15 SSID

PCI: B/D/F/Reg: 0/0/0/2Ch
SBI: Port/Reg/Mem: 08h/0Bh/
MMIO: Base/Offset:
IO: Base/Offset:

SubsystemID

Bit	Access	Default Value	Description
31:0	RO	strapSSID[31:0]	**STRAPSSID:** The value in this field is a copy of the SSID register programmed by the graphics device driver or BIOS in the Device 2 PCI header. To change the subsystem ID, write to Device 2 SSID instead of to this SSID.

1.11.16 DFX.GMCH_PERF_CAPABILITIES

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F0h/
MMIO: Base/Offset:
IO: Base/Offset:

Perfmon Capabilities Register and Clock gating override

Bit	Access	Default Value	Description
31	RW	0b	**PERFMON_CORECLK_GATING_DISABLE:** ; 1 = Disable clock gating for coreclk in perfmon. ; 0 = Enable clock gating for coreclk in perfmon ; This is a debug feature -- DO NOT Publish this bit in C-Spec
30:1	RO	00000000h	**RESERVED:** Reserved
0	RO	1b	**GMCH_PERF_AVAILABLE:** Need to Check if this bit can be RW ; 1=GMCH.PERFMON registers are available. ; 0=not available. Writes to GMCH.PERFMON registers are ignored. Reads return all 0's

1.11.17 DFX.GMCH_PERF_EVTSEL0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/E0h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL0

Bit	Access	Default Value	Description
31:24	RW	00000000b	**COUNTER_MASK:** Counter Mask
23	RW	0b	**INVERT:** 1 Enable 0 Disable
22	RW	0b	**ENABLE:** 1 Enable 0 Disable
21	RO	0b	**RESERVED:** Reserved
20	RW	0b	**INTERRUPT:** 1 Enable ; 0 Disable
19	RO	0b	**RESERVED:** Reserved
18	RW	0b	**EDGE_DETECT:** 1 Enable 0 Disable
17:16	RO	00b	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.18 DFX.GMCH_PERF_EVTSEL1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/E1h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL1

Bit	Access	Default Value	Description
31:24	RW	00000000b	**COUNTER_MASK:** Counter Mask
23	RW	0b	**INVERT:** 1 Enable ; 0 Disable
22	RW	0b	**ENABLE:** 1 Enable ; 0 Disable
21	RO	0b	**RESERVED:** Reserved
20	RW	0b	**INTERRUPT:** 1 Enable ; 0 Disable
19	RO	0b	**RESERVED:** Reserved
18	RW	0b	**EDGE_DETECT:** 1 Enable ; 0 Disable
17:16	RO	00b	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.19 DFX.GMCH_PERF_EVTSEL2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/E2h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL2

Bit	Access	Default Value	Description
31:24	RW	00000000b	**COUNTER_MASK:** Counter Mask
23	RW	0b	**INVERT:** 1 Enable 0 Disable
22	RW	0b	**ENABLE:** 1 Enable 0 Disable
21	RO	0b	**RESERVED:** Reserved
20	RW	0b	**INTERRUPT:** 1 Enable 0 Disable
19	RO	0b	**RESERVED:** Reserved
18	RW	0b	**EDGE_DETECT:** 1 Enable 0 Disable
17:16	RO	00b	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.

Bit	Access	Default Value	Description
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.20 DFX.GMCH_PERF_EVTSEL3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/E3h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL2

Bit	Access	Default Value	Description
31:24	RW	00000000b	**COUNTER_MASK:** Counter Mask
23	RW	0b	**INVERT:** 1 Enable 0 Disable
22	RW	0b	**ENABLE:** 1 Enable 0 Disable
21	RO	0b	**RESERVED:** Reserved
20	RW	0b	**INTERRUPT:** 1 Enable 0 Disable
19	RO	0b	**RESERVED:** Reserved
18	RW	0b	**EDGE_DETECT:** 1 Enable 0 Disable
17:16	RO	00b	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.21 DFX.GMCH_PERF_FIXED_CTR0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/E8h/
MMIO: Base/Offset:
IO: Base/Offset:

Fixed Counter 0 -- counts coreclk cycles when enabled

Bit	Access	Default Value	Description
31:0	RW	00000000h	**GMCH_PERF_FIXED_CTR0:** Fixed Counter 0

1.11.22 DFX.GMCH_PERF_FIXED_CTR_CTRL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F4h/
MMIO: Base/Offset:
IO: Base/Offset:

Fixed Counter Control

Bit	Access	Default Value	Description
31:2	RO	00000000h	**RESERVED:** Reserved
1	RW	0b	**ENABLE_PMI_FIXED_CTR0:** 1 Enable PMI on Overflow 0 Disable
0	RW	0b	**ENABLE_FIXED_CTR0:** 1 Enable 0 Disable

1.11.23 DFX.GMCH_PERF_GLOBAL_CTRL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F1h/
MMIO: Base/Offset:
IO: Base/Offset:

Perfmon fixed and General Counter Control

Bit	Access	Default Value	Description
31:17	RO	0000h	**RESERVED:** Reserved
16	RW	0b	**ENABLE_FIXED_CTR0:** 1 Enable ; 0 Disable
15:4	RO	000h	**RESERVED:** Reserved
3	RW	1b	**ENABLE_GP_CTR3:** Enable global counter 3 ; 1 Enable ; 0 Disable
2	RW	1b	**ENABLE_GP_CTR2:** Enable global counter 2 ; 1 Enable ; 0 Disable
1	RW	1b	**ENABLE_GP_CTR1:** Enable global counter 1 ; 1 Enable ; 0 Disable
0	RW	1b	**ENABLE_GP_CTR0:** Enable global counter 0 ; 1 Enable ; 0 Disable

1.11.24 DFX.GMCH_PERF_GLOBAL_OVF_CTRL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F3h/
MMIO: Base/Offset:
IO: Base/Offset:

Perfmon fixed and General Counter Overflow Clear

Bit	Access	Default Value	Description
31:17	WO	0000h	**RESERVED:** Reserved
16	WO	0b	**CLEAR_OVERFLOW_FIXED_CTR0:** 1 Clear ; 0 Default
15:4	WO	000h	**RESERVED:** Reserved
3	WO	0b	**CLEAR_OVERFLOW_GP_CTR3:** 1 Clear ; 0 Default
2	WO	0b	**CLEAR_OVERFLOW_GP_CTR2:** 1 Clear ; 0 Default
1	WO	0b	**CLEAR_OVERFLOW_GP_CTR1:** 1 Clear ; 0 Default
0	WO	0b	**CLEAR_OVERFLOW_GP_CTR0:** 1 Clear ; 0 Default

1.11.25 DFX.GMCH_PERF_GLOBAL_STATUS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F2h/
MMIO: Base/Offset:
IO: Base/Offset:

Perfmon fixed and General Counter Status

Bit	Access	Default Value	Description
31:17	RO	0000h	**RESERVED:** Reserved
16	RW	0b	**OVERFLOW_FIXED_CTR0:** 1 Overflow ; 0 Default
15:4	RO	000h	**RESERVED:** Reserved
3	RW	0b	**OVERFLOW_GP_CTR3:** 1 Overflow ; 0 Default
2	RW	0b	**OVERFLOW_GP_CTR2:** 1 Overflow ; 0 Default
1	RW	0b	**OVERFLOW_GP_CTR1:** 1 Overflow ; 0 Default
0	RW	0b	**OVERFLOW_GP_CTR0:** 1 Overflow ; 0 Default

1.11.26 DFX.GMCH_PERF_GP_CTR0_H

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/FCh/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 0 Upper Half

Bit	Access	Default Value	Description
31:6	RO	0000h	**RESERVED:** Reserved
5:0	RW	00000000h	**GMCH_PERF_GP_CTR0_H:** General Purpose Counter 0 Upper Half

1.11.27 DFX.GMCH_PERF_GP_CTR0_L

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F8h/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 0 Lower Half

Bit	Access	Default Value	Description
31:0	RW	00000000h	**GMCH_PERF_GP_CTR0_L:** General Purpose Counter 0 Lower Half

1.11.28 DFX.GMCH_PERF_GP_CTR1_H

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/FDh/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 1 Upper Half

Bit	Access	Default Value	Description
31:6	RO	0000h	**RESERVED:** Reserved
5:0	RW	00h	**GMCH_PERF_GP_CTR1_H:** General Purpose Counter 1 Upper Half

1.11.29 DFX.GMCH_PERF_GP_CTR1_L

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/F9h/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 1 Lower Half

Bit	Access	Default Value	Description
31:0	RW	00000000h	**GMCH_PERF_GP_CTR1_L:** General Purpose Counter 1 Lower Half

1.11.30 DFX.GMCH_PERF_GP_CTR2_H

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/FEh/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 2 Upper Half

Bit	Access	Default Value	Description
31:6	RO	0000h	**RESERVED:** Reserved
5:0	RW	00h	**GMCH_PERF_GP_CTR2_H:** General Purpose Counter 2 Upper Half

1.11.31 DFX.GMCH_PERF_GP_CTR2_L

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/FAh/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 2

Bit	Access	Default Value	Description
31:0	RW	00000000h	**GMCH_PERF_GP_CTR2_L:** General Purpose Counter 2 Lower Half

1.11.32 DFX.GMCH_PERF_GP_CTR3_H

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/FFh/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 3 Upper Half

Bit	Access	Default Value	Description
31:6	RO	0000h	**RESERVED:** Reserved
5:0	RW	00h	**GMCH_PERF_GP_CTR3_H:** General Purpose Counter 3 Upper Half

1.11.33 DFX.GMCH_PERF_GP_CTR3_L

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 05h/FBh/
MMIO: Base/Offset:
IO: Base/Offset:

General Purpose Counter 3

Bit	Access	Default Value	Description
31:0	RW	00000000h	**GMCH_PERF_GP_CTR3_L:** General Purpose Counter 3 Lower Half

1.11.34 DISPLAY_CONTROLLER.ADPA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61100h
MMIO: Base/Offset: MMADR/61100h
IO: Base/Offset:

Description CRT port control dprrega.v adp_Q

Bit	Access	Default Value	Description
31	RW		**ADPA_ENABLE:** This bit enables or disables the DAC output. It has no effect on the horizontal or vertical sync outputs. 1 Enable. This bit enables analog port DAC 0 Disable the DAC and go to a low power state. Can be bypassed by DFx by dfx_dsp_crtdacen but in order to enable the dfx_dsp_crtdacoff must be reset
30	RW		**PIPE_SELECT:** Determines which display pipe will feed this DAC port. This only applies to dual display pipe devices. It is reserved in all other devices. 0 Pipe A 1 Pipe B
29:16	RO		**RESERVED0:** Software must preserve the contents of these bits.
15	RW		**ADPA_HSYNC_AND_VSYNC_POLARITY_SELECT:** VGA VSYNC and HSYNC polarity bits are ignored on this port when this bit is clear. This should only be set if this port is used for VGA display in the VGA native mode. 1 Use VGA registers to select VSYNC and HSYNC Polarities. VGA Native Mode 0 Use bits 4 and 3 of this register ADPA to select VSYNC and HSYNC Polarities.
14	RO		**RESERVED1:** Software must preserve the contents of this field.
13:12	RO		**RESERVED2:**
11:10	RW		**MONITOR_DPMS:** for CRT port When the graphics device is in D0 these bits force the HSYNC VSYNC output signal to the state specified in the polarity selection or allow the standard timing generated syncs to continue. These bits enable proper handling of DPMS monitors that support the D1 or D2 states during display device power management by toggling sync signals required. This field should always be loaded with the

Bit	Access	Default Value	Description
			display device D state during display power management operations. 00 Monitor in D0 Monitor On. will not affect sync pulses 01 Monitor in D2. Monitor Suspend HSYNC pulses VSYNC does not. 10 Monitor in D1. Monitor Standby VSYNC pulses HSYNC does not 11 Monitor in D3. Monitor Off Neither HSYNC nor VSYNC pulses
9:5	RO		**RESERVED3:**
4	RW		**VSYNC_POLARITY_CONTROL:** The output VSYNC polarity is controlled either by the VGA control bits or this bit when in VGA modes. This is used to implement display modes that require inverted polarity syncs and to set the disabled state of the VSYNC signal. 1 Active high. 0 Active low.
3	RW		**HSYNC_POLARITY_CONTROL:** According to the ADPA polarity select bit the HSYNC polarity is controlled by either the VGA sync polarity register bit or this bit. 1 Active high. 0 Active low.
2:0	RO		**RESERVED4:** Software must preserve the contents of these bits.

1.11.35 DISPLAY_CONTROLLER.AUD_CNTL_ST

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620B4h
MMIO: Base/Offset: MMADR/620B4h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**RESERVED0:** read as zero
30:29	RO		**DIP_PORT_SELECT:** This read only bit reflects which port is used to transmit the DIP data. This can only change when DIP is disabled. A reserved setting reflects a disabled DIP. If one or more audio related DIP packets is enabled and audio is enabled on a HDMI port these bits will reflect the HDMI port to which audio is directed. 00 Reserved 01 HDMI B 10 HDMI C 11 Reserved
28:25	RO		**RESERVED_FOR_LATER_DIP_TYPE_IF_NEEDED1:** Must be 0.
24:21	RO		**DIP_TYPE_ENABLE_STATUS:** These bits reflects the DIP types enabled. It can be updated while the port is enabled. Within 2 vblank periods the DIP is guaranteed to have been transmitted. Disabling an DIP type results in setting the contents of that DIP buffer to zero. A reserved setting reflects a disabled DIP. XXX1 Audio DIP enable status Default disabled XX1X Generic 1 ACP DIP enable status Default disabled X1XX Generic 2 DIP enable status can be used by ISRC1 or ISRC2 Default disabled 1XXX Reserved
20:18	RW		**DIP_BUFFER_INDEX:** This field is used during read of different DIPs and during read or write of ELD data. These

Bit	Access	Default Value	Description
			bits are used as an index to their respective DIP or ELD buffers. When the index is not valid the contents of the DIP will return all 0 s. 000 Default Audio DIP 31 bytes of address space 13 bytes of data 001 Generic 1 ACP Data Island Packet 31 bytes of address space 11 bytes of data 010 Generic 2 ISRC1 Data Island Packet 31 bytes of address space 31 bytes of data 011 Generic 3 ISRC2 Data Island Packet 31 bytes of address space 31 bytes of data 1XX reserved
17:16	RO		**DIP_TRANSMISSION_FREQUENCY:** These bits reflect the frequency of DIP transmission for the DIP buffer type designated in bits 20 18. When writing DIP data this value is also latched when the first DW of the DIP is written. When read this value reflects the DIP transmission frequency for the DIP buffer designated in bits 20 18. 00 Disabled Default 01 Reserved 10 Send once 11 Best effort Send at least every other vsync
15	RW		**CP_READY:** This R W bit reflects the state of CP request from the audio unit. When an audio CP request has been serviced it must be reset to 1 by the video software to indicate that the CP request has been serviced. 0 CP request pending or not ready to receive requests default 1 CP request ready CP_ready bit is programmable through Bit 14 for DevCL DevBLC . CP_ready bit is programmable through Bit 15 for DevCTG . Bit 15 Reserved for DevCL DevBLC .
14	RW		**ELD_VALID:** This R W bit reflects the state of the ELD data written to the ELD RAM. After writing the ELD data the video software must set this bit to 1 to indicate that the ELD data is valid. At audio codec initialization or on a hotplug event this bit is set to 0 by the video software. This bit is reflected in the audio pin complex widget as the ELD valid status bit. 0 ELD data invalid default when writing ELD data set 0 by software 1 ELD data valid Set by video software only ELD bit is programmable through Bit 13 for DevCL DevBLC . ELD bit is programmable through Bit 14 for DevCTG .
13:9	RO		**ELD_BUFFER_SIZE:** 10000 This field reflects the size of the ELD buffer in DWORDs 13 9 reflects ELD buffer size for DevCTG . 12 9 reflects ELD buffer size for DevCL DevBLC .
8:5	RW		**ELD_ACCESS_ADDRESS:** Selects the DWORD address for access to the ELD buffer 48 bytes . The value wraps back to zero when incremented past the max addressing value 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.
4	RW		**ELD_ACK:** Acknowledgement from the audio driver that ELD read has been completed
3:0	RW		**DIP_RAM_ACCESS_ADDRESS:** Selects the DWORD address for access to the DIP buffers. The value wraps back to zero when it incremented past the max addressing value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

1.11.36 DISPLAY_CONTROLLER.AUD_CONFIG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62000h
MMIO: Base/Offset: MMADR/62000h
IO: Base/Offset:

This register configures the audio output.

Bit	Access	Default Value	Description
31:26	RO		**RESERVED0:**
25	RW		**N_PROGRAMMING_ENABLE:** This bit enables programming of N values for non CEA modes. Please note that the pipe to which audio is attached must be disabled when changing this field.
24:20	RW		**UPPER_N_VALUE:** These are bits 16 12 of programmable N values for non CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the pipe to which audio is attached must be disabled when changing this field.
19:16	RW		**PIXEL_CLOCK:** This pixel clock value should match the DPLL programming for the pipe to which audio is attached. This value is used for generating N_CTS packets see description in the above paragraph. Note The pipe on which audio is attached must be disabled when changing this field. 0000 25.2 1.001 MHz 0001 25.2 MHz Program this value for pixel clocks not listed in this field 1000 148.5 1.001 MHz 1001 148.5 MHz 1010 1111 Reserved
15:4	RW		**LOWER_N_VALUE:** These are bits 11 0 of programmable N values for non CEA modes. Bit 25 of this register must also be written in order to enable programming. Please note that the pipe to which audio is attached must be disabled when changing this field.
3	RW		**DISABLE_NCTS:** Set this bit to disable NCTS generation for CTM modes. This is to enable prediction of CRC in CTM modes.
2	RW		**FABRICATION_EN_BIT:** This bit indicates whether internal fabrication of audio samples is enabled during a link underrun. 0 default audio fabrication disabled 1 audio fabrication enabled
1	RW		**PRO_ALLOWED:** By default the audio device is configured to consumer mode and does not allow the mode to be changed to professional mode by an HD Audio verb. When Pro is allowed by setting this configuration bit the HD Audio codec allows a verb to set the device into professional mode. Note Setting this configuration bit does not change the default Pro bit value to be 1. Pro must be set to 1 through the normal process using a verb. 0 Consumer use only default 1 Professional use allowed
0	RO		**AUDIO_ENABLE_FUSE_STATUS:** This bit reflects the status of the audio fuse. 0 default Audio enabled 1 Audio disabled

1.11.37 DISPLAY_CONTROLLER.AUD_CONV_CHCNT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62120h
MMIO: Base/Offset: MMADR/62120h
IO: Base/Offset:

HDMI converter Channel Mapping verb. Read only Reference HDMI SDVO EDS 0.79 Section 5.3.13 HDMI Channel to Converter Channel Mapping

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15:14	RO		**HBR_ENABLED_DEVELK:** This reflects the current HBR settings. DevCTG Reserved
13:12	RO		**RESERVED1:**
11:8	RO		**CONVERTOR_CHANNEL_COUNT_DEVCTG:** This reflects the Convertor Channel Count programmed through Intel HD Audio.
7:4	RO		**CONVERTER_CHANNEL_MAP:** The number in this field reflects the HD audio channel to which the HDMI channel in bits 3 0 is mapped. This field is read only
3:0	RO		**HDMI_INDEX_:** 7 of this register.

1.11.38 DISPLAY_CONTROLLER.AUD_CTS_ENABLE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62128h
MMIO: Base/Offset: MMADR/62128h
IO: Base/Offset:

These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.

Bit	Access	Default Value	Description
31:21	RO		**RESERVED0:**
20	RO		**ENABLE_CTS_PROGRAMMING:** When set will enable CTS programming.
19:0	RO		**CTS_VALUES:** These are bits 19 0 of programmable CTS values for non CEA modes. Bit 21 of this register must also be written in order to enable programming. Please note that the pipe to which audio is attached must be disabled when changing this field.

1.11.39 DISPLAY_CONTROLLER.AUD_DEBUG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62010h
MMIO: Base/Offset: MMADR/62010h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:1	RO		**RESERVED0:** Read only.
0	RW		**FUNCTION_RESET:** This bit indicates that an audio function reset occurred through the reset signal on the HD audio bus. Clearing this status bit is accomplished by writing a 1 to this bit through MMIO.

1.11.40 DISPLAY_CONTROLLER.AUD_FUNCGRP_SUBN_CNT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62044h
MMIO: Base/Offset: MMADR/62044h
IO: Base/Offset:

These values are returned from the device as the Subordinate Node Count response to a Get Audio Function Group command.

Bit	Access	Default Value	Description
31:25	RO		**RESERVED0:**
24:16	RO		**STARTING_NODE_NUMBER:** Starting node ID of the subordinate node set. This field is hardwired to 0x2.
15:8	RO		**RESERVED1:**
7:0	RO		**TOTAL_NUMBER_OF_NODES:** Total number of subordinate nodes. This field is hardwired to 0x2

1.11.41 DISPLAY_CONTROLLER.AUD_FUNC_GRP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62040h
MMIO: Base/Offset: MMADR/62040h
IO: Base/Offset:

These values are returned from the device as the Function Group Type response to a Get Audio Function Group command.

Bit	Access	Default Value	Description
31:9	RO		**RESERVED0:**
8	RO		**UNSOL_CAPABLE:** Indicates that this node is capable of generating an unsolicited response. This bit is hardwired to 0. All the widget are not capable of generating unsolicited response.

Bit	Access	Default Value	Description
7:0	RO		**NODE_TYPE:** Type of audio node This field is hardwired to 0x1 Audio function group

1.11.42 DISPLAY_CONTROLLER.AUD_GRP_CAP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62048h
MMIO: Base/Offset: MMADR/62048h
IO: Base/Offset:

These values are returned from the device as the Audio Function Group Capabilities response to a Get Audio Function Group command.

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16	RO		**RESERVED1:**
15:12	RO		**RESERVED2:**
11:8	RO		**RESERVED3:**
7:4	RO		**RESERVED4:**
3:0	RO		**OUTPUT_DELAY:** The number of samples between when the sample is received from the HD Audio link and when it appears as an analog signal at the pin. This field is default 4

1.11.43 DISPLAY_CONTROLLER.AUD_HDMIW_HDMIEDID

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6210Ch
MMIO: Base/Offset: MMADR/6210Ch
IO: Base/Offset:

These registers contain the HDMI data block from the EDID. The graphics driver reads the EDID and writes the structure to these registers. The vendor specific data block may be longer than 8 bytes but the driver must not write more than 48 bytes to the buffer. The EDID format is Version 3 within the CEA 861B specification. The HDMI Vendor Specific Data Block is described in version 1.1 of the HDMI specification. These values are returned from the device as the HDMI Vendor Specific Data Block response to a Get HDMI Widget command. Writing sequence Video software sets ELD invalid and sets the ELD access address to 0 or to the desired DWORD to be written. Video software writes ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD write wrapping around to address 0 when the max buffer address size of 0xF has been reached. Please note that software must write an entire DWORD at a time. Please note that the audio driver checks the valid bit with each byte read of the ELD. This means that the video driver can unilaterally write ELD irrespective of audio driver ELD read status. Reading sequence Video software sets the ELD access address to 0 or to the desired DWORD to be read. Video software reads ELD data 1 DWORD at a time. The ELD access address autoincrements with each DWORD read wrapping around to address 0 when the max buffer address size of 0xF has been reached.

Bit	Access	Default Value	Description
31:0	RW		**EDID_HDMI_DATA_BLOCK:** Please note that the contents of this buffer are not cleared when ELD is disabled. The contents of this buffer are cleared during GFX reset

1.11.44 DISPLAY_CONTROLLER.AUD_HDMIW_INFOFR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62118h
MMIO: Base/Offset: MMADR/62118h
IO: Base/Offset:

When the IF type or DWORD index is not valid the contents of the DIP will return all 0 s. These values are programmed by the audio driver in an HDMI Widget Set command. They are returned one byte at a time from the device on the HD audio bus as the HDMI DIP response to a Get HDMI Widget command. To fetch a specific byte the audio driver should send an HDMI Widget HDMI DIP Index Pointer Set command to set the index then fetch the indexed byte using the HDMI DIP get. Video driver read sequence for debug only Video software sets DIP type to the appropriate DIP and sets the DIP access address to the desired DWORD. Video software reads DIP data 1 DWORD at a time. The DIP access address autoincrements with each DWORD write wrapping around to address 0 when the max buffer address size of 0xF has been reached.

Bit	Access	Default Value	Description
31:0	RO		**DATA_ISLAND_PACKET_DATA:** This reflects the contents of the DIP indexed by the DIP access address. The contents of this buffer are cleared during function reset or HD audio link reset.

1.11.45 DISPLAY_CONTROLLER.AUD_HDMIW_STATUS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620D4h
MMIO: Base/Offset: MMADR/620D4h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**CDCLK_DOTCLK_FIFO_UNDERRUN:** This bit indicates an underrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by reading this value through the HD audio bus or writing a 1 to this bit through MMIO.
30	RW		**CDCLK_DOTCLK_FIFO_OVERRUN:** This bit indicates an overrun in the FIFO inside the clock crossing logic between CDCLK and DOTCLK. Clearing this status bit is accomplished by reading this value through the HD audio bus or writing a 1 to this bit through MMIO.
29	RW		**BCLK_CDCLK_FIFO_UNDERRUN:** This bit indicates an underrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by reading this value through the HD audio bus or writing a 1 to this bit through MMIO.
28	RW		**BCLK_CDCLK_FIFO_OVERRUN:** This bit indicates an overrun in the FIFO inside the clock crossing logic between BCLK and CDCLK. Clearing this status bit is accomplished by reading this value through the HD audio bus or writing a 1 to this bit through MMIO.
26:0	RO		**RESERVED0:**

1.11.46 DISPLAY_CONTROLLER.AUD_OUT_CH_STR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62080h
MMIO: Base/Offset: MMADR/62080h
IO: Base/Offset:

These values are returned from the device as the Channel ID and Stream ID response to a Get Audio Output Converter Widget command.

Bit	Access	Default Value	Description
31:8	RO		**RESERVED0:**
7:4	RO		**STREAM_ID:** Represents the link stream used by the converter for data input or output. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default 0 stream 0
3:0	RO		**LOWEST_CHANNEL_NUMBER:** Represents the lowest channel used by the converter. This value is set in the Channel ID and Stream ID through the Set Audio Output Converter Widget command. Default 0

1.11.47 DISPLAY_CONTROLLER.AUD_OUT_CWCAP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62070h
MMIO: Base/Offset: MMADR/62070h
IO: Base/Offset:

These values are returned from the device as the Audio Output Converter Widget Capabilities response to a Get Audio Output Converter Widget command. Previous default value 00000211h DevCL DevBLC

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:20	RO		**WIDGET_TYPE:** Functionality of the widget node. This field is hardwired to 0 Audio output
19:16	RO		**RESERVED1:** Hardware always returns 0 for this value.
15:13	RO		**MULTICHANCNT_13:** 1 DevCTG These bits indicate multichannel capability. Number of audio channels supported MultiChanCnt 3 0 1 Hardwired to 011 Reserved DevCL DevBLC
12	RO		**RESERVED2:**
11	RO		**RESERVED3:** Hardware always returns 0 for this value.
10	RO		**RESERVED4:** Hardware always returns 0 for this value.
9	RO		**DIGITAL:** Indicates that a widget supports a digital stream. This bit is hardwired to 1 digital supported
8	RO		**CONN_LIST:** Indicates whether a connection list is present on the widget. This field is hardwired to 0 The

Bit	Access	Default Value	Description
			only connection for the widget is to the HD Audio link
7	RO		**UNSOL_CAPABLE:** The audio widget supports unsolicited responses. This bit is hardwired to 0 Does not support unsolicited responses
6	RO		**RESERVED5:** Hardware always returns 0 for this value.
5	RO		**RESERVED6:**
4	RO		**FORMAT_OVERRIDE:** The widget contains format information and the Supported Formats and Supported PCM Bits Rates should be queried for the widget s format capabilities. This field is hardwired within the device. Value 1 Widget contains format information
3	RO		**RESERVED7:** Hardware always returns 0 for this value.
2	RO		**RESERVED8:** Hardware always returns 0 for this value.
1	RO		**RESERVED9:** Hardware always returns 0 for this value.
0	RO		**STEREO_DEVCL:** Determines if the widget is a stereo or mono widget. This bit is hardwired to 1 The widget is a stereo widget MultiChanCnt 1 0 DevCTG These bits indicate multichannel capability. Number of audio channels supported MultiChanCnt 3 0 1 Hardwired to 1

1.11.48 DISPLAY_CONTROLLER.AUD_OUT_DIG_CNVT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6207Ch
MMIO: Base/Offset: MMADR/6207Ch
IO: Base/Offset:

These values are returned from the device as the Digital Converter response to a Get Audio Output Converter Widget command.

Bit	Access	Default Value	Description
31:15	RO		**RESERVED0:**
14:8	RO		**CATEGORY_CODE:** S PDIF IEC Category Code. This value is set in the Digital Converter 1 through the Set Audio Output Converter Widget command. Default 0
7	RO		**LEVEL:** S PDIF IEC Generation Level. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default 0
6	RO		**PRO:** This bit indicates professional or consumer use of channel. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. This value can only be set to 1 if the Pro Allowed bit is set in the audio configuration register.
5	RO		**NON_AUDIO:** Data is non PCM format. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.

Bit	Access	Default Value	Description
4	RO		**COPY:** Copyright asserted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.
3	RO		**PRE:** Filter pre-emphasis. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.
2	RO		**VCFG:** Validity Configuration. Determines S PDIF transmitter behavior when data is not being transmitted. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default 0
1	RO		**V:** Affects the validity flag transmitted in each subframe and enables the S PDIF transmitter to maintain connection during error or mute conditions. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command. Default 0
0	RO		**DIGEN:** Enables digital transmission through this node. This value is set in the Digital Converter 2 through the Set Audio Output Converter Widget command.

1.11.49 DISPLAY_CONTROLLER.AUD_OUT_PCMSIZE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62074h
MMIO: Base/Offset: MMADR/62074h
IO: Base/Offset:

These values are returned from the device as the PCM Size and Rates response to a Get Audio Output Converter Widget command. Previous default value 001E0170h DevCL DevBLC

Bit	Access	Default Value	Description
31:21	RO		**RESERVED0:**
20	RO		**B32:** Indicates that 32 bit audio formats are supported. This bit is hardwired to 1 32 bit audio formats are not supported . Writes to this bit are ignored.
19	RO		**B24:** Indicates that 24 bit audio formats are supported. Default 1 24 bit audio formats are supported
18	RO		**B20:** Indicates that 20 bit audio formats are supported. Default 1 20 bit audio formats are supported
17	RO		**B16:** Indicates that 16 bit audio formats are supported. Default 1 16 bit audio formats are supported
16	RO		**RESERVED1:** Hardware always returns 0 for this value. Writes to this bit are ignored.
15:12	RO		**RESERVED2:**
11	RO		**RESERVED3:** Hardware always returns 0 for this value. Writes to these bits are ignored.
10	RO		**R11:** 192 kHz rate supported Default 0 DevCL DevBLC

Bit	Access	Default Value	Description
			Default 1 DevCTG
9	RO		**R10:** 176.4 kHz rate supported Default 0 DevCL DevBLC Default 1 DevCTG
8	RO		**R9:** Indicates that 96.0 kHz rate is supported. Default 1 96.0 supported
7	RO		**R8:** Indicates that 88.2 kHz rate is supported. This bit is hardwired to 0 88.2 kHz unsupported . DevCL DevBLC This bit is hardwired to 1 88.2kHz supported DevCTG Writes to this bit are ignored.
6	RO		**R7:** Indicates that 48.0 kHz is supported. Default 1 48.0 kHz supported
5	RO		**R6:** Indicates that 44.1 kHz is supported. Default 1 44.1 kHz supported
4	RO		**R5:** Indicates that 32.0 kHz is supported. Default 1 32.0 kHz supported
3:0	RO		**RESERVED4:** Hardware always returns 0 for this value. Writes to these bits are ignored.

1.11.50 DISPLAY_CONTROLLER.AUD_OUT_STR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62078h
MMIO: Base/Offset: MMADR/62078h
IO: Base/Offset:

These values are returned from the device as the Stream Formats response to a Get Audio Output Converter Widget command.

Bit	Access	Default Value	Description
31:3	RO		**RESERVED0:**
2	RO		**AC3:** Indicates that the widget supports AC3 compressed audio. Default 1 AC3 supported
1	RO		**RESERVED1:** Hardware always returns 0 for this value. Writes to this bit are ignored.
0	RO		**PCM:** Indicates that the widget supports PCM formatted data. Default 1 PCM supported

1.11.51 DISPLAY_CONTROLLER.AUD_OUT_STR_DESC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62084h
MMIO: Base/Offset: MMADR/62084h
IO: Base/Offset:

These values are returned from the device as the Stream Descriptor Format response to a Get Audio Output Converter Widget command.

Bit	Access	Default Value	Description
31:15	RO		**RESERVED0:**
14	RO		**SAMPLE_BASE_RATE:** Sampling base rate of audio stream 0 48 kHz 1 44.1 kHz This bit is hardwired to 0 48 KHz
13:11	RO		**SAMPLE_BASE_RATE_MULT:** Audio stream sample base rate multiple 000 48 kHz 44.1 kHz or less 001 x2 96 kHz 88.2 kHz 32 kHz 100 111 Reserved This field is hardwired to 000 48 KHz
10:8	RO		**SAMPLE_BASE_RATE_DIVISOR:** Audio stream sample base rate divisor 000 Divide by 1 48 kHz 44.1 kHz 001 Divide by 2 24 kHz 22.05 kHz 010 Divide by 3 16 kHz 32 kHz 011 Divide by 4 11.025 kHz 100 Divide by 5 9.6 kHz 101 Divide by 6 8 kHz 110 Divide by 7 111 Divide by 8 6 kHz This field is hardwired to 000 indicates divide by 1 which results in 48 KHz
7	RO		**RESERVED1:**
6:4	RO		**BITS_PER_SAMPLE:** 000 8 bits. The data will be packed in memory in 8 bit containers on 16 bit boundaries 001 16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundaries 100 20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 010 24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 011 32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundaries 101 111 Reserved This field is hardwired to 0x3 Indicates 24 bits
3:0	RO		**NUMBER_OF_CHANNELS_IN_A_STREAM:** Number of channels in each frame of the stream 0000 1 0001 2 1111 16 This field is hardwired to 0x2 3 channels in each frame

1.11.52 DISPLAY_CONTROLLER.AUD_PINW_CAP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620A0h
MMIO: Base/Offset: MMADR/620A0h
IO: Base/Offset:

These values are returned from the device as the Pin Complex Widget Capabilities response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:20	RO		**WIDGET_TYPE:** This field defines the functionality of the widget node. This field is hardwired to 0x4 Pin Complex
19:16	RO		**RESERVED1:** Hardware always returns 0s for this value.
15:13	RO		**MULTICHANNEL3:** 1 DevCTG Default 011 Reserved DevCL DevBLC
12	RO		**PROTECTION_CAPABLITY:** This bit reflects whether the audio output is capable of supporting HDCP. It is hardwired to 1
11	RO		**RESERVED2:** Hardware always returns 0 for this value.
10	RO		**RESERVED3:** Hardware always returns 0 for this value.
9	RO		**DIGITAL:** This bit indicates that a widget supports digital stream. This bit is hardwired to 1 digital widgets supported
8	RO		**CONN_LIST:** This bit indicates whether a connection list is present on the widget. This bit is hardwired to 1 Connection List Length parameter and the Connection List Entry controls should be queried to discover the input connections.
7	RO		**UNSOL_CAPABLE:** This bit indicates whether the audio widget supports unsolicited responses. This value is set in the Unsolicited Enable through the Set Pin Widget command. 0 Unsolicited responses are not supported 1 Unsolicited responses are supported default
6	RO		**RESERVED4:** Hardware always returns 0 for this value.
5	RO		**OUTPUT_AMP_CAPABILITIES:**
4	RO		**FORMAT_OVERRIDE:** If Format Override is a 1 the widget contains format information and the Supported Formats and Supported PCM Bits Rates should be queried for the widget s format capabilities. If this bit is a 0 then the Audio Function node must contain default amplifier parameters and that node s format related parameters should be queried to determine the format parameters. This bit is hardwired to 1 widget contains format information
3	RO		**RESERVED5:** Hardware always returns 1 for this value.
2	RO		**OUT_AMP_PRESENT:** Hardware always returns 1 for this value.

Bit	Access	Default Value	Description
1	RO		**RESERVED6:** Hardware always returns 0 for this value.
0	RO		**MULTICHANNELCNT0_DEVCTG:** This bit determines if the widget is a multi channel Widget This bit is hardwired to 1 MultiChannel Widget Stereo DevCL DevBLC This bit determines if the widget is a stereo or mono widget. This bit is hardwired to 1 stereo widget

1.11.53 DISPLAY_CONTROLLER.AUD_PINW_CNTR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620B0h
MMIO: Base/Offset: MMADR/620B0h
IO: Base/Offset:

These values are returned from the device as the Pin Widget Control response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31:9	RO		**RESERVED0:**
8	RO		**AMP_MUTE_STATUS:** This read only bit reflects the mute status of the amplifier 0 Amp not muted 1 default Amp muted
7	RO		**RESERVED1:** Hardware always returns 0 for this value.
6	RO		**OUT_ENABLE:** This bit reflects the state of the output path of the Pin Widget. When 0 audio is disabled . Default 1
5	RO		**RESERVED2:** Hardware always returns 0 for this value.
4:3	RO		**RESERVED3:**
2:0	RO		**RESERVED_DEVCL4:** Hardware always returns 0 for this value. Encoded Stream Type DevELK 000 Default samples 001 One bit stream 010 DST stream 011 MLP stream either FBA or FBB HDMI Packet type will be set to 0x09 Others Reserved

1.11.54 DISPLAY_CONTROLLER.AUD_PINW_CONFIG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620BCh
MMIO: Base/Offset: MMADR/620BCh
IO: Base/Offset:

These values are returned from the device as the Config Default response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31:30	RO		**PORT_CONNECTIVITY:** Indicates the external connectivity of the pin complex. Default 0x0
29:24	RO		**LOCATION:** Indicates the physical location of the jack or device to which the pin complex is connected Default 0x18 HDMI
23:20	RO		**DEFAULT_DEVICE:** Indicates the intended use of the jack or device Default 0x5 SPDIF out
19:16	RO		**CONNECTION_TYPE:** Indicates the type of physical connection Default 0x6 Other digital
15:12	RO		**COLOR:** Indicates the color of the physical jack for use by software Default 0x0 Unknown
11:8	RO		**MISC:** Indicate other information about the jack. If the LSB of this field is set it indicates that the jack has no presence detect capability Default 0x0 Jack detect
7:4	RO		**DEFAULT_ASSOCIATION:** Used by software to group pin complexes together into functional blocks to support multichannel operation Default 0x1
3:0	RO		**SEQUENCE:** Indicates the order of jacks in the association group Default 0x0

1.11.55 DISPLAY_CONTROLLER.AUD_PINW_CONNLNG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620A8h
MMIO: Base/Offset: MMADR/620A8h
IO: Base/Offset:

These values are returned from the device as the Connection List Length response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31:8	RO		**RESERVED0:**
7	RO		**LONG_FORM:** This bit indicates whether the items in the connection list are long form or short form . This bit is hardwired to 0 items in connection list are short form
6:0	RO		**CONNECTION_LIST_LENGTH:** This field indicates the number of items in the connection list. If this field is 1 there is only one hardwired input possible which is read from the Connection List and there is no Connection Select Control. This field is hardwired to 0x1

1.11.56 DISPLAY_CONTROLLER.AUD_PINW_CONNLST

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620ACh
MMIO: Base/Offset: MMADR/620ACh
IO: Base/Offset:

These values are returned from the device as the Connection List Entry response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31:24	RO		**CONNECTION_LIST_ENTRY_B3:** This field is hardwired within the device. Value 0
23:16	RO		**CONNECTION_LIST_ENTRY_B2:** This field is hardwired within the device. Value 0
15:8	RO		**CONNECTION_LIST_ENTRY_B1:** This field is hardwired within the device. Value 0
7:0	RO		**CONNECTION_LIST_ENTRY_B0:** This field is hardwired within the device. Value 0x2 Indicates connection to Audio Output Converter

1.11.57 DISPLAY_CONTROLLER.AUD_PINW_UNSOLRESP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620B8h
MMIO: Base/Offset: MMADR/620B8h
IO: Base/Offset:

These values are returned from the device as the Unsolicited Response Enable response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31	RO		**ENABLE_UNSOLICITED_RESPONSE:** This bit reflects the Unsolicited Responses are enabled by the audio software. 0 Unsolicited responses not enabled Default 1 Unsolicited responses enabled
30:12	RO		**RESERVED0:**
11:7	RO		**CP_SUBTAG:** Reflects the subtag of the CP unsolicited response sent by audio hardware to audio software. Please note that the ELD valid subtag is always 0 so it is not reported. 0 presence detect ELD valid
6	RO		**RESERVED1:**
5:0	RO		**TAG:** This tag will be sent on the top six bits 31 26 of every Unsolicited response generated by this node addressing the appropriate audio driver. This value which is opaque to the codec and is used by software to determine what codec node generated the unsolicited response.

1.11.58 DISPLAY_CONTROLLER.AUD_PIN_CAP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//620A4h
MMIO: Base/Offset: MMADR/620A4h
IO: Base/Offset:

These values are returned from the device as the Pin Capabilities response to a Get Pin Widget command.

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16	RO		**RESERVED1:** Hardware always returns 0 for this value.
15:8	RO		**RESERVED2:** Hardware always returns 0s for this value.
7	RO		**HDMI_CAPABLE:** Indicates ability to transmit HDMI packets with video Hardware always returns 1 for this value
6	RO		**RESERVED3:** Hardware always returns 0 for this value.
5	RO		**RESERVED4:** Hardware always returns 0 for this value.
4	RO		**OUTPUT_CAPABLE:** This bit indicates whether the pin

Bit	Access	Default Value	Description
			complex supports output. This value is set in the Pin Widget Control through the Set Pin Widget command. 0 Pin is Not capable of output 1 Pin is capable of output Default
3	RO		**RESERVED5:** Hardware always returns 0 for this value.
2	RO		**PRESENCE_DETECT_CAPABLE:** This bit indicates whether the pin complex can perform presence detect to determine whether there is anything plugged in. Presence Detect does not indicate what is plugged in only that something is plugged in. This bit is hardwired to 1 Can perform presence detect
1	RO		**RESERVED6:** Hardware always returns 0 for this value.
0	RO		**RESERVED7:** Hardware always returns 0 for this value.

1.11.59 DISPLAY_CONTROLLER.AUD_PWRST

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6204Ch
MMIO: Base/Offset: MMADR/6204Ch
IO: Base/Offset:

These values are returned from the device as the Power State response to a Get Audio Function Group command.

Bit	Access	Default Value	Description
31:4	RO		**RESERVED0:**
5:4	RO		**DEVICE_POWER_STATE:** Current power state of the device 00 D0 01 10 Unsupported 11 D3 Default
3:2	RO		**RESERVED1:**
1:0	RO		**DEVICE_POWER_STATE_SETTING:** Power state that was set on the device 00 D0 01 10 Unsupported 11 D3 Default

1.11.60 DISPLAY_CONTROLLER.AUD_RID

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62024h
MMIO: Base/Offset: MMADR/62024h
IO: Base/Offset:

These values are returned from the device as the Revision ID response to a Get Root Node command.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:20	RO		**MAJOR_REVISION:** The major revision number left of the decimal of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value 0x1
19:16	RO		**MINOR_REVISION:** The minor revision number rights of the decimal or dot number of the HD Audio Spec to which the codec is fully compliant. This field is hardwired within the device. Value 0x0
15:8	RO		**REVISION_ID:** The vendor s revision number for this given Device ID. This field is hardwired within the device. Value 0x0
7:0	RO		**STEPPING_ID:** An optional vendor stepping number within the given Revision ID. This field is hardwired within the device. Value 0x0

1.11.61 DISPLAY_CONTROLLER.AUD_ROOT_SUBN_CNT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62028h
MMIO: Base/Offset: MMADR/62028h
IO: Base/Offset:

These values are returned from the device as the Subordinate Node Count response to a Get Root Node command.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** unused
23:16	RO		**STARTING_NODE_NUMBER:** Starting node ID of the subordinate node set. This field is hardwired within the device. Value 1
15:8	RO		**RESERVED1:**
7:0	RO		**TOTAL_NUMBER_OF_NODES:** Number of nodes in the subordinate node set. This field is hardwired within the device. Value 1

1.11.62 DISPLAY_CONTROLLER.AUD_SID

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62054h
MMIO: Base/Offset: MMADR/62054h
IO: Base/Offset:

These values are returned from the device as the Subsystem ID response to a Get Audio Function Group command.

Bit	Access	Default Value	Description
31:0	RO		**BOARD_IMPLEMENTATION_ID:** This provides information about the hardware implementation including system board information. This field should be written by system BIOS. For this product the value should be set to 0x80860101

1.11.63 DISPLAY_CONTROLLER.AUD_SUPPWR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62050h
MMIO: Base/Offset: MMADR/62050h
IO: Base/Offset:

These values are returned from the device as the Supported Power States response to a Get Audio Function Group command.

Bit	Access	Default Value	Description
31:4	RO		**RESERVED0:**
3	RO		**D3:** Device supports D3 power state. This bit is hardwired to 1 D3 supported
2	RO		**RESERVED1:** Hardware always returns 0 for this value.
1	RO		**RESERVED2:** Hardware always returns 0 for this value.
0	RO		**D0:** Device supports D0 power state. This bit is hardwired to 1 D0 supported

1.11.64 DISPLAY_CONTROLLER.AUD_VID_DID

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//62020h
MMIO: Base/Offset: MMADR/62020h
IO: Base/Offset:

These values are returned from the device as the Vendor ID Device ID response to a Get Root Node command. Previous default values 808629FBh DEVCL 80862801h DEVBLC

Bit	Access	Default Value	Description
31:16	RO		**VENDOR_ID:** Used to identify the codec within the PnP system. This field is hardwired within the device. Value 0x8086
15:0	RO		**DEVICE_ID:** Constant used to identify the codec within the PnP system. This field is set by the device hardware. 0x29FB DevCL 0x2801 DevBLC 0x2802 DevCTG

1.11.65 DISPLAY_CONTROLLER.BCLRPAT_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60020h
MMIO: Base/Offset: MMADR/60020h
IO: Base/Offset:

This register value determines what color should be sent to the display in the border region the space between the end of active and the beginning of blank and the end of blank and the beginning of active.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**PIPE_A_BORDER_RED_CHANNEL_VALUE:**
15:8	RW		**PIPE_A_BORDER_GREEN_CHANNEL_VALUE:**
7:0	RW		**PIPE_A_BORDER_BLUE_CHANNEL_VALUE:**

1.11.66 DISPLAY_CONTROLLER.BCLRPAT_B

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61020h
MMIO: Base/Offset: MMADR/61020h
IO: Base/Offset:

This register determines the color sent during the border region the periods between the end of blank and the start of active and the end of active and the start of blank. Also same color will be sent during pseudo border period. VGA border color is determined by the VGA border overscan color register.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**PIPE_B_RED_CHANNEL_COLOR_VALUE:**
15:8	RW		**PIPE_B_GREEN_CHANNEL_COLOR_VALUE:**
7:0	RW		**PIPE_B_BLUE_CHANNEL_COLOR_VALUE:**

1.11.67 DISPLAY_CONTROLLER.BLC_PWM_CLT2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61250h
MMIO: Base/Offset: MMADR/61250h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**PWM_ENABLE:** This bit enables the PWM counter logic 0 PWM disabled drives 0 always 1 PWM enabled
30	RW		**BLM_LEGACY_MODE:** 0 PWM Duty Cycle is derived from the Backlight Duty Cycle only 1 PWM Duty Cycle is a combination of Backlight Duty Cycle and Legacy Backlight Control LBPC Note 1 implies the Duty Cycle if BPC 7 0 lt gt xFF then BPCR 15 0 BPC 7 0 Else BPCR 15 0
29	RW		**PWM_PIPE_ASSIGNMENT:** This bit assigns PWM to a pipe. The PWM counter will run off of this pipe s PLL. The PWM function must be disabled in order to change the value of this field. 0 Pipe A 1 Pipe B
28	RW		**BACKLIGHT_POLARITY:** 0 Active High 1 Active Low
27	RO		**RESERVED0:**
26	RW		**PHASE_IN_INTERRUPT_STATUS:** This bit will be set by hardware when a Phase In interrupt has occurred. Software will clear this bit by writing a 1 which will reset the interrupt generation. DevCL A B Reserved
25	RW		**PHASE_IN_ENABLE:** Setting this bit enables a PWM phase in based on the programming of the Phase In registers below. This bit clears itself when the phase in is completed.
24	RW		**PHASE_IN_INTERRUPT_ENABLE:** Setting this bit

Bit	Access	Default Value	Description
			enables an interrupt to be generated when the PWM phase in is completed.
23:16	RW		**PHASE_IN_TIME_BASE:** This field determines the number of VBLANK events that pass before one increment occurs. 0 invalid 1 1 vblank 2 2 vblanks etc.
15:8	RW		**PHASE_IN_COUNT:** This field determines the number of increment events in this phase in. Writes to this register should only occur when hardware phase ins are disabled. Reads to this register can occur any time where the value in this field indicates the number of increment events remaining to fully apply a phase in request as hardware automatically decrements this value. A value of 0 is invalid. In order to write the same value to this field for the second time one must write a dummy value to this field for example 0 before writing the real value for the second time.
7:0	RW		**PHASE_IN_INCREMENT:** This field indicates the amount to adjust the PWM duty cycle register on each increment event. This is a two s complement number.

1.11.68 DISPLAY_CONTROLLER.BLC_PWM_CTL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61254h
MMIO: Base/Offset: MMADR/61254h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:16	RW		**BACKLIGHT_MODULATION_FREQUENCY:**
15:0	RW		**BACKLIGHT_DUTY_CYCLE:**

1.11.69 DISPLAY_CONTROLLER.BLM_HIST_CTL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61260h
MMIO: Base/Offset: MMADR/61260h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**IMAGE_ENHANCEMENT_HISTOGRAM_ENABLED:** This bit enables the Image Enhancement histogram logic to collect data. 0 Image histogram is disabled 1 The Image histogram is enabled. When this bit is changed from a zero to a one histogram calculations will begin after the next VBLANK of the assigned pipe.
30	RW		**IMAGE_ENHANCEMENT_MODIFICATION_TABLE_ENABLED:** This bit enables the Image Enhancement modification table. 0 disabled 1 enabled. When this bit is changed from a zero to a one modifications begin after the next VBLANK of

Bit	Access	Default Value	Description
			the assigned pipe.
29	RW		**IMAGE_ENHANCEMENT_PIPE_ASSIGNMENT:** This bit assigns the IE function to a pipe. IE events will be synchronized to the VBLANK of the selected pipe. The IE function must be disabled in order to change the value of this field. 0 Pipe A 1 Pipe B
28:25	RO		**RESERVED0:** Always write as 0 s.
24	RW		**HISTOGRAM_MODE_SELECT:** 0 YUV Luma Mode 1 HSV Intensity Mode Reserved on DevCL
23:16	RW		**SYNC_TO_PHASE_IN_COUNT:** This field indicates the phase in count number on which the Image Enhancement table will be loaded if the Sync to Phase in is enabled.
15	RO		**RESERVED1:** Always write as 0.
14:13	RW		**ENHANCEMENT_MODE:** 00 Direct look up mode 01 Additive mode 10 Multiplicative mode Reserved on DevCL 11 Reserved
12	RW		**SYNC_TO_PHASE_IN:** Setting this bit enables the double buffered registers to be loaded on the phase in count value specified instead of the next vblank.
11	RW		**BIN_REGISTER_FUNCTION_SELECT:** This field indicates what data is being written to or read from the bin data register. 0 Bin Threshold Count. A read from the bin data register returns that bin s threshold value from the most recent vblank load event guardband threshold trip . Valid range for the Bin Index is 0 to 31. 1 Bin Image Enhancement Value. Valid range for the Bin Index is 0 to 32
10:7	RO		**RESERVED2:** Always write as 0 s.
6:0	RO		**BIN_REGISTER_INDEX:** This field indicates the bin number whose data can be accessed through the bin data register. This value is automatically incremented by a read or a write to the bin data register if the busy bit is not set.

1.11.70 DISPLAY_CONTROLLER.CBR1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70400h
MMIO: Base/Offset: MMADR/70400h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:**
28:26	WO		**VGA_OOO_QUEUE_DEPTH:** 0xx Disable out of order stall logic for VGA 100 Enable out of order VGA stall depth of 64 101 Enable out of order VGA stall depth of 48 110 Enable out of order VGA stall depth of 32 111 Enable out of order VGA stall depth of 16
25	WO		**PLLB_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe B to be disabled before the PLL is shut down
24	WO		**PLLA_SAFE_SHUTDOWN_OVERRIDE:** This bit disables the dependency for pipe A to be disabled before the PLL is shut down
23:22	RO		**RESERVED1:**
21	WO		**ELPIN_409_SELECT:** This bit is used to select one of the elpin 409 bug fixes
20	RO		**RESERVED2:**
19	WO		**CR12_WRITE_COUNTER_RESET:**
18	RO		**RESERVED3:**
17	WO		**MONITOR_DETECTION:** This bit is used to test the monitor detection. Do not program unless directed.
16	WO		**INVERT_DPO_FIELD:** Invert DPO interlaced field output. This bit is used to invert the field sense input to the planes from DPO.
15	RO		**RESERVED4:**
14	WO		**HPD_TEST_MODE:** load programmable value for filter and long pulse value of HPD register 0x70408.
13	WO		**SDVOC_SELECT:** sdvoc deglitch logic output select
12	WO		**SDVOB_SELECT:** sdvob deglitch logic output select
11	WO		**VGA_STALL:** Stall native mode VGA when frequency is over 50 MHz. This bit is only used during VGA native mode.
10	RO		**RESERVED5:** DevCL Dev Intel Atom Processor D2000 and N2000 Series Disable Crestline C0 fix for requests performance
9	WO		**PIXEL_SIZE:** This bit changes the VGA pixel width and height calculations.
8	WO		**IMMEDIATE_ASYNCHRONOUS_FLIPS:** This bit causes asynchronous flips to complete immediately upon the start

Bit	Access	Default Value	Description
			of the vertical blank period. When enabling this feature frame start should also be moved to the end of the vertical blank period by setting the frame start position bit.
7	WO		**PIPE_B_FRAME_START_POSITION:** This bit changes the position of frame start on pipe B. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking.
6	WO		**PIPE_B_PALETTE_WRITE_ENABLE:** Disables anti collision logic in the palette during non blanking periods on pipe B.
5	WO		**PIPE_A_PALETTE_WRITE_ENABLE:** Disables anti collision logic in the palette during non blanking periods on pipe A
4	RO		**RESERVED6:**
3	WO		**PIPE_A_FRAME_START_POSITION:** This bit changes the position of frame start on pipe A. This feature is used in conjunction with the immediate asynchronous flips bit to enable fast asynchronous flips during vertical blanking.
2:0	RO		**RESERVED7:**

1.11.71 DISPLAY_CONTROLLER.CBR2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70404h
MMIO: Base/Offset: MMADR/70404h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	WO		**DPRDDB_VGAENRST_DIS:** Enable rise and fall detection of DPRvgadis for DDB reset dprddb_vgaenrst_dis
30:28	RO		**RESERVED0:**
27	WO		**DCN_447625:** x8 support for hybrid GFX Kwasi requested dpr_dpio_x8_conc_sel
26	WO		**DPIOMB0UNIT:** ignoring EDP logic when enabling Lanes by the dptc_otxoenb
25	WO		**DPSEL_OVERRIDE:** when this chicken bit is set override the selects to 0 dpsel_override
24	WO		**DITHERING_ENHANCE_DISABLE:** Anh need for dithering enhance dithering_enhance_disable
23	WO		**EDGE:** edgeA Bvblank edgeDPSA Bvblank curA Bedgevblank
22	WO		**DPRAUDM_EARLY_HDE_DISABLE:** Chicken bit to Audio unit to disable early RAM FIFO read in 2 channel mode DPRAUDM_early_hde_disable

Bit	Access	Default Value	Description
21	WO		**DPLR:** Selects cdclk for pwm logic pwm logic uses hrawclk by default
20	WO		**DPRAUDM_CKGATE_PKTCNTRL_IDLE_DIS:** Chicken bit to disable audclk gating when pktcontrol FSM is idle DPRAUDM_ckgate_pktcntrl_idle_dis
19	WO		**DPR_DPIO_PORTOFF_NOT_HBLK_CHICKEN:** This bit is needed to qualify the port off with hblank to take care of fragmented audio packet sent off.
18	WO		**MMIO_WRITE_EVENT:**
17	WO		**DBLATEN_ARMED_CURA_B:**
16	WO		**HPD_INTR_FIX:** Freezes hpdb_intr_fix hpdc_intr_fix hpdd_intr_fix
15	RO		**RESERVED1:**
14	WO		**PORT_B_LANES_READY_IGNORE:**
13	WO		**PORT_C_LANES_READY_IGNORE:**
12	WO		**DPLLS_OK_IGNORE:**
11	WO		**RSVD**
10	WO		**DPR_VS_AFLIPTOTAL_CHICKEN:** This chicken bit bypasses the current logic used for calculating the number of requests to make for an asynchronous flip. It will be helpful because the current logic is very difficult to validate.
9	WO		**DPR_VS_BYTEEN_CHICKEN:** This chicken bit bypasses the current logic used for selecting the proper byte enables. It is intended to address byte enables during asynchronous flips but it was easier to bypass the entire byte enable circuit instead. HSD bug 1932963. dpr_vs_byteen_chicken
8	WO		**DPR_VS_AFLIPADDR_CHICKEN:** This chicken bit bypasses the current logic used for selecting the starting fetch address of an asynchronous flip. HSD bug 1932964. dpr_vs_aflipaddr_chicken
7:6	WO		**DPRDDB_SYNC_SELECT:** When set vsync reset is asserted and when clear no reset is asserted. dprddb_novsyncreset
5	WO		**DDBMUNIT:** C0 ECO1 chicken bit defaulted to fix enable
4	WO		**HDCP:** EGLK A5 ECO1 Fix. Read Data Fix For RMBus Protocol.
3:2	WO		**DPRVGA_DPBSTALL_UL_THRESHOLD:** VGATEST2 issue fix Stall throttling done during horiz_blank and UL mode is asserted.
1	WO		**DPRAUDM_SAMPLE_PRESENT_DISABLE:** When set this bit will disable the sample present bits being set in layout 1 mode of Audio. Default is to enable sample present on Audio. DPRAUDM_sample_present_disable

Bit	Access	Default Value	Description
0	WO		**REGA_LOADCOUNT_CRTDETECT:**

1.11.72 DISPLAY_CONTROLLER.CBR3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7040Ch
MMIO: Base/Offset: MMADR/7040Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:25	WO		**DPTPIPEB_CHICKEN_BITS:** not used
24:18	WO		**DPTPIPEA_CHICKEN_BITS:** not used
17	WO		**PIPEBCLKGATEEN:** Enables reg_pipeBclkgateen_cd reg_pipeBclkgateen_db
16	WO		**PIPEACLKGATEEN:** Enables reg_pipeAclkgateen_cd reg_pipeAclkgateen_da
15	RW		**MENC16:** Chicken to cause MENC to output just 16 Manchester 0s for sync otherwise 26
14	WO		**MENC_NEVERENDING:** Chicken to cause MENC to output never-ending sync 0s for electrical testing
13	WO		**FREQUENCY_WINDOWING:** Chicken to tighten the frequency windowing
12	WO		**GOOD_SYNC:** Chicken to check for only 8 good sync 0s instead of 12
11:10	WO		**SELECT_CDCLK_COUNT_FOR_DEGLITCH:** 11 1 16 2X bit clock divider value 31.125ns 10 1 8 2X bit clock divider value 62.5ns 01 1 4 2X bit clock divider value 125ns 00 25 GMBUS type 50ns at 500MHz cdclk
9	WO		**CHICKEN_UNGATECLK:** 1 Ungate clock 0 Automatic clock gating
8	WO		**CHICKEN_MULTIEDGEERROR:** 1 Multiple edges in window is an error 0 Multiple edges in window is okay
7:6	WO		**READBACK:** 11 Readback of bit clock divide field gives the error type 01 Readback gives the recovered clock frequency 00 Readback gives the programmed clock frequency
5:4	WO		**AUXD_GMBUS_CONNECTION:** Selects GMBUS connection for AUXD
3:2	WO		**AUXC_GMBUS_CONNECTION:** Selects GMBUS connection for AUXC
1:0	WO		**AUXB_GMBUS_CONNECTION:** Selects GMBUS connection for AUXB

1.11.73 DISPLAY_CONTROLLER.CCBR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70408h
MMIO: Base/Offset: MMADR/70408h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	WO		**HPD_AND_CRT_DETECT_TEST_MODES:**

1.11.74 DISPLAY_CONTROLLER.CRCCTRLALPHAA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6005Ch
MMIO: Base/Offset: MMADR/6005Ch
IO: Base/Offset:

Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

1.11.75 DISPLAY_CONTROLLER.CRCCTRLALPHAB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6105Ch
MMIO: Base/Offset: MMADR/6105Ch
IO: Base/Offset:

Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

1.11.76 DISPLAY_CONTROLLER.CRCCTRLBLUEA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60058h
MMIO: Base/Offset: MMADR/60058h
IO: Base/Offset:

Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

1.11.77 DISPLAY_CONTROLLER.CRCCTRLBLUEB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61058h
MMIO: Base/Offset: MMADR/61058h
IO: Base/Offset:

Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

1.11.78 DISPLAY_CONTROLLER.CRCCTRLGREENA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60054h
MMIO: Base/Offset: MMADR/60054h
IO: Base/Offset:

Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

1.11.79 DISPLAY_CONTROLLER.CRCCTRLGREENB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61054h
MMIO: Base/Offset: MMADR/61054h
IO: Base/Offset:

Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

1.11.80 DISPLAY_CONTROLLER.CRCCTRLREDA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60050h
MMIO: Base/Offset: MMADR/60050h
IO: Base/Offset:

The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. For any changes to the CRC controls you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. Border area is always included in the CRC calculation. There are five CRC calculators Red Green Blue Residual1 and Residual2 DevCTG Dev Intel Atom Processor D2000 series and N2000 Series each with an 8 bit data input and 23 bit CRC result. For Display Port CRC DevCTG Dev Intel Atom Processor D2000 series and N2000 Series the 40 bit lane data is spread across the inputs of all five of the CRC calculators. For Pipe the 30 bit pixel data is spread across the inputs of four of the CRC calculators. The fifth is unused and will be ignored for expected CRC comparison and error generation. Pipe CRC should not be run when Display Port or TV is enabled on this pipe.

Bit	Access	Default Value	Description
31	RW		**ENABLE_COLOR_CRC:** Enables the CRC calculations. After being enabled for the first time you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. 0 CRC Calculations are disabled 1 CRC Calculations are enabled
30:28	RW		**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 000 Pipe A Not available when DisplayPort or TV is enabled on this pipe 001 sDVOB 30 bit format 010 sDVOC 30 bit format 011 DisplayPort D 40 bit format DevCTG 100 TV Encoder outputs 30 bit format 101 TV filter outputs 30 bit format 110 DisplayPort B 40 bit format DevCTG Dev Intel Atom Processor D2000

Bit	Access	Default Value	Description
			series and N2000 Series 111 DisplayPort C 40 bit format DevCTG Dev Intel Atom Processor D2000 series and N2000 Series
27:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

1.11.81 DISPLAY_CONTROLLER.CRCCTRLREDB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61050h
MMIO: Base/Offset: MMADR/61050h
IO: Base/Offset:

The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. For any changes to the CRC controls you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. Border area is always included in the CRC calculation. See description of CRCCtrlColorA for more details

Bit	Access	Default Value	Description
31	RW		**ENABLE_COLOR_CHANNEL_CRC:** After being enabled for the first time you need to wait for two VBLANK events for a valid CRC result. After that a CRC will be generated each frame. 0 CRC Calculations are disabled 1 CRC Calculations are enabled
30:28	RW		**CRC_SOURCE_SELECT:** These bits select the source of the data to put into the CRC logic. 000 Pipe B Not available when DisplayPort or TV is enabled on this pipe 001 sDVOB 30 bit format 010 sDVOC 30 bit format 011 DisplayPort D 40 bit format DevCTG 100 TV Encoder outputs 30 bit format 101 TV Filter outputs 30 bit format 110 DisplayPort B 40 bit format DevCTG 111 DisplayPort C 40 bit format DevCTG
27:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

1.11.82 DISPLAY_CONTROLLER.CRCCTRLRESIDUE2A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60070h
MMIO: Base/Offset: MMADR/60070h
IO: Base/Offset:

Calculation is enabled in the CRCCtrlRedA register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. Status indications are in the PIPEASTAT register.

1.11.83 DISPLAY_CONTROLLER.CRCCTRLRESIDUE2B

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61070h
MMIO: Base/Offset: MMADR/61070h
IO: Base/Offset:

Calculation is enabled in the CRCCtrlColorA Red register. The value read is obtained from a double buffer of this register that is updated on VSync except when a CRC error is detected. Border area is always included in the CRC calculation. The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Write as zero
22:0	RW		**EXPECTED_CRC_VALUE:** Expected CRC Value for the Color Channel. This is the value used to generate the CRC error status and interrupt. Resultant CRC values are compared to this register after the completion of a CRC calculation. The status bit is in the PIPEBSTAT register.

1.11.84 DISPLAY_CONTROLLER.CRCRESALPHAA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6006Ch
MMIO: Base/Offset: MMADR/6006Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

1.11.85 DISPLAY_CONTROLLER.CRCRESALPHAB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6106Ch
MMIO: Base/Offset: MMADR/6106Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

1.11.86 DISPLAY_CONTROLLER.CRCRESBLUEA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60068h
MMIO: Base/Offset: MMADR/60068h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

1.11.87 DISPLAY_CONTROLLER.CRCRESBLUEB

PCI: B/D/F/Reg:

SBI: Port/Reg/Mem: 06h//61068h
MMIO: Base/Offset: MMADR/61068h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

1.11.88 DISPLAY_CONTROLLER.CRCRESGREENA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60064h
MMIO: Base/Offset: MMADR/60064h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

1.11.89 DISPLAY_CONTROLLER.CRCRESGREENB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61064h
MMIO: Base/Offset: MMADR/61064h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

1.11.90 DISPLAY_CONTROLLER.CRCRESREDA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60060h
MMIO: Base/Offset: MMADR/60060h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

1.11.91 DISPLAY_CONTROLLER.CRCRESREDB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61060h
MMIO: Base/Offset: MMADR/61060h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

1.11.92 DISPLAY_CONTROLLER.CRCRESRESIDUAL2B

PCI: B/D/F/Reg:

SBI: Port/Reg/Mem: 06h//61080h
MMIO: Base/Offset: MMADR/61080h
IO: Base/Offset:

The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation. The result of a CRC on an empty frame will be 7FFFFFh.

1.11.93 DISPLAY_CONTROLLER.CRCRESRESIDUE2A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60080h
MMIO: Base/Offset: MMADR/60080h
IO: Base/Offset:

The value in the residual registers will not necessarily be zero during 8bpc CRC calculations.

Bit	Access	Default Value	Description
31:23	RO		**RESERVED0:** Read only
22:0	RO		**COLOR_CHANNEL_CRC_RESULT_VALUE:** This field contains the resultant CRC value for the particular Color Channel at the end of a frame. A status bit can be used as an indication that the data is the valid result of a CRC calculation.

1.11.94 DISPLAY_CONTROLLER.CRTIO_DFX

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61104h
MMIO: Base/Offset: MMADR/61104h
IO: Base/Offset:

Description CRT port control dprrega.v crt_dfx

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15	RW		**CHOPPING_ENABLE:** Chopping enable for BG circuit
14:12	RW		**BONUS_FOR_DPR:**
11:8	RW		**MODESEL:**
7:4	RW		**BONUS_FOR_CRT:**

Bit	Access	Default Value	Description
3:0	RO		**DIAGNOSTIC:** Observe signals at CRTIO

1.11.95 DISPLAY_CONTROLLER.CURABASE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70084h
MMIO: Base/Offset: MMADR/70084h
IO: Base/Offset:

This register specifies the graphics memory address at which the cursor image data is located. Writes to this register acts like a trigger that enables atomic updates of the cursor registers. When updating the cursor registers this register should be written last in the sequence. This register should be written even if the actual contents did not change to allow the holding registers to move to the active registers on the next VBLANK. For legacy cursor modes this register is sufficient to specify the address of the entire cursor. For ARGB modes this register specifies the address of the first page of the cursor data.

Bit	Access	Default Value	Description
31:4	RW		**CURSOR_BASE_ADDRESS:** 4 of the graphics address of the base of the cursor. On DevBW and DevCL if the cursor is a popup this field specifies bits 31 4 of the physical address of the base of the cursor and bits 35 32 of the address are specified in the LSBs of this register. Popup cursor mode is selected within the CURACNTR register. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory it cannot be tiled. When performing 180 rotation this offset must be the difference between the last pixel of the last line of the cursor data in its un-rotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress.
3:0	RW		**POPUP_CURSOR_BASE_ADDRESS_MSBS:** 32 of the popup cursor physical address. If popup mode is not selected this field is ignored.

1.11.96 DISPLAY_CONTROLLER.CURACNTR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70080h
MMIO: Base/Offset: MMADR/70080h
IO: Base/Offset:

This register and all other cursor registers will remain in their holding register readable after a write. The holding registers are transferred into the active registers on the asserting edge of Vertical Blank only after a write cycle to the base address register has completed. DevBLC and DevCTG For hires modes Cursor A is connected to pipe A only. For VGA popup it follows the VGA pipe select.

Bit	Access	Default Value	Description
31:30	RO		**RESERVED0:** Write as zero.
29:28	RW		**DEVBW_DEVCL_DEVCDV_PIPE_SELECT:** A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned when both display pipes are being used it can be switched at any time the hardware will synchronize the switch. 00 HW cursor is attached to Display Pipe A. This is the default after reset. 01 HW cursor is attached to Display Pipe B. 10 Reserved for pipe C 11 Reserved for pipe D DevBLC and DevCTG Reserved Write as zero.
27	RW		**POPUP_CURSOR_ENABLED:** 0 Cursor A is hi res 1 Cursor A is popup
26	RW		**CURSOR_GAMMA_ENABLE:** This bit only has an effect when using the cursor in a non VGA mode. In VGA pop up operation the cursor data will always bypass the gamma palette unit. 0 Cursor pixel data bypasses gamma correction or palette default . 1 Cursor pixel data is gamma to be corrected in the pipe.
25:16	RO		**RESERVED1:** Write as zero
15	RW		**ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit software must also set the base address to the lower right corner of the un-rotated image. Only 32 bits per pixel cursors can be rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 No rotation 1 180 Rotation of 32 bit per pixel cursors
14:6	RO		**RESERVED2:**
5	RW		**CURSOR_MODE_SELECT_BIT:** See following table.
4	RO		**RESERVED3:**
3	RO		**RESERVED4:**
2:0	RW		**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

1.11.97 DISPLAY_CONTROLLER.CURAPALET

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70090h

MMIO: Base/Offset: MMADR/70090h
IO: Base/Offset:

These palette registers can be accessed through this MMIO interface register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. The two bit index selects one of the four colors or two of the colors when in the AND XOR cursor mode. The cursor palette provides color information when using one of the indexed modes. The two bit index selects one of the four colors or two of the colors when in the AND XOR cursor mode.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** Write as zero.
23:16	RW		**RED_OR_Y_VALUE:** These registers specify the cursor palette. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.
15:8	RW		**GREEN_OR_U_VALUE:**
7:0	RW		**BLUE_OR_V_VALUE:**

1.11.98 DISPLAY_CONTROLLER.CURAPOS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70088h
MMIO: Base/Offset: MMADR/70088h
IO: Base/Offset:

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically requires that the base address be written and is double buffered.

Bit	Access	Default Value	Description
31	RW		**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13 bit value that specifies the horizontal position of cursor. default is 0 . For normal high resolution display modes the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup the entire cursor must be positioned over the active area of the VGA image.
30:28	RO		**RESERVED0:** Write as zero.
27:16	RW		**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0 This register provides the magnitude bits of a signed 12 bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. default is 0 . For use as a VGA Popup the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA Border Enable bit in the VGA Config register includes the border in what is considered the active area . For HDMI modes where the vertical zoom is greater than 1x the position is specified using the zoomed

Bit	Access	Default Value	Description
			grid. When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation.
15	RW		**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13 bit value that specifies the horizontal position of cursor. default is 0 . . For normal high resolution display modes the cursor must have at least a single pixel positioned over the active screen. For use as a VGA Popup the entire cursor must be positioned over the active area of the VGA image. Enabling the border in VGA Border Enable bit in the VGA Config register includes the border in what is considered the active area .
14:12	RO		**RESERVED1:** Write as zero.
11:0	RW		**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0 These 12 bits provide the signed 13 bit value that specifies the horizontal position of cursor. The sign bit is provided by bit 15 of this register. default is 0 For HDMI modes where the horizontal zoom is greater than 1x the position is specified using the zoomed grid. When performing 180 rotation this field specifies the horizontal position of the lower right corner relative to the end of the active video area in the un-rotated orientation.

1.11.99 DISPLAY_CONTROLLER.CURARESV

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7008Ch
MMIO: Base/Offset: MMADR/7008Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO		**RESERVED0:**

1.11.100 DISPLAY_CONTROLLER.CURBBASE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//700C4h
MMIO: Base/Offset: MMADR/700C4h
IO: Base/Offset:

This register specifies the memory address at which the cursor data is located. Writes to this register should be done with 32 bit accesses and acts as a trigger to atomically update the cursor register set. For legacy cursor modes this register is sufficient to specify the address of the entire cursor. The address is the graphics address. For ARGB modes this register specifies the address of the first page of the cursor data.

Bit	Access	Default Value	Description
31:0	RW		**CURSOR_BASE_ADDRESS:** This register specifies the graphics address of the entire cursor. It also acts as a trigger event to force the update of active registers on the

Bit	Access	Default Value	Description
			next display event. The cursor surface address must be 4K byte aligned. The cursor must be in linear memory it cannot be tiled. When performing 180 rotation this offset must be the difference between the last pixel of the last line of the cursor data in its un-rotated orientation and the cursor surface address. A write to this register also acts as a trigger event to force the update of active registers from the staging registers on the next display event. Each cursor register is double buffered. The CPU writes to a set of holding registers. The active registers are updated from the holding registers following the leading edge of the vertical blank pulse. The update is postponed until the next vblank if a write cycle is active to any of the cursor registers at the time of the vblank. The update is also postponed if a write sequence is in progress.

1.11.101 DISPLAY_CONTROLLER.CURBCNTR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//700C0h
MMIO: Base/Offset: MMADR/700C0h
IO: Base/Offset:

The hardware cursor registers are memory mapped and accessible through 32 bit 16 bit or 8 bit accesses. They are all including the palette registers double buffered. Writes to cursor registers are done to a holding register. The actual register update will occur based on the assigned pipes VBLANK. It is recommended that the base register be accessed through a 32 bit write only. To update all cursor registers atomically a sequence that ends with a base address register write should be used. DevBLC and DevCTG Cursor B is connected to pipe B only.

Bit	Access	Default Value	Description
31:30	RO		**RESERVED0:** Write as zero.
29:28	RW		**PIPE_SELECT_DEVBW_DEVCL_DEVCDV:** A state machine handles the synchronization of the switch to both vertical blank signals. So as far as the software is concerned when both display pipes are being used it can be switched at any time the hardware will synchronize the switch. 00 HW cursor is attached to Display Pipe A. This is the default after reset. 01 HW cursor is attached to Display Pipe B. 10 Reserved for to Display Pipe C. 11 Reserved for to Display Pipe D. Reserved DevBLC and DevCTG Write as zero.
27	RO		**RESERVED1:** Write as zero.
26	RW		**CURSOR_GAMMA_ENABLE:** 1 Cursor pixel data is gamma to be corrected.
25:16	RO		**RESERVED2:**
15	RW		**ROTATION:** This mode causes the cursor to be rotated 180 . In addition to setting this bit software must also set the base address to the lower right corner of the un-rotated image. Only 32 bits per pixel cursors can be

Bit	Access	Default Value	Description
			rotated. This field must be zero when the cursor format is 2 bits per pixel. 0 No rotation 1 180 Rotation of 32 bit per pixel cursors
14:6	RO		**RESERVED3:** Write as zero
5	RW		**CURSOR_MODE_SELECT_BIT:** See following table.
4:3	RO		**RESERVED4:**
2:0	RW		**CURSOR_MODE_SELECT:** These three bits together with bit 5 select the mode for cursor as shown in the following table.

1.11.102 DISPLAY_CONTROLLER.CURBPOS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//700C8h
MMIO: Base/Offset: MMADR/700C8h
IO: Base/Offset:

This register specifies the screen position of the cursor. The origin of the cursor position is always the upper left corner of the active image for the display pipe that the cursor is assigned. This register can be loaded atomically and is double buffered. The load register is transferred into the active register on the leading edge of Vertical Blank of the pipe cursor is currently assigned after the trigger has been set.

Bit	Access	Default Value	Description
31	RW		**CURSOR_Y_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13 bit value that specifies the horizontal position of cursor. default is 0 . . For normal high resolution display modes the cursor must have at least a single pixel positioned over the active screen.
30:28	RO		**RESERVED0:** Write as zero.
27:16	RW		**CURSOR_Y_POSITION_MAGNITUDE_BITS_11:** 0 This register provides the magnitude bits of a signed 13 bit value that specifies the vertical position of cursor. The sign bit of this value is provided by bit 31of this register. default is 0 When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation.
15	RW		**CURSOR_X_POSITION_SIGN_BIT:** This bit provides the sign bit of a signed 13 bit value that specifies the horizontal position of cursor. default is 0 . . For normal high resolution display modes the cursor must have at least a single pixel positioned over the active screen. For HDMI modes where the vertical zoom is greater than 1x the position is specified using the zoomed grid.
14:12	RO		**RESERVED1:** Write as zero.
11:0	RW		**CURSOR_X_POSITION_MAGNITUDE_BITS_11:** 0 These 12 bits provide the signed 13 bit value that specifies the horizontal position of cursor. The sign bit is provided

Bit	Access	Default Value	Description
			by bit 15 of this register. default is 0 For HDMI modes where the horizontal zoom is greater than 1x the position is specified using the zoomed grid. When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation.

1.11.103 DISPLAY_CONTROLLER.CURBRESV

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//700CCh
MMIO: Base/Offset: MMADR/700CCh
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO		**RESERVED0:**

1.11.104 DISPLAY_CONTROLLER.CURB_PALET

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//700D0h
MMIO: Base/Offset: MMADR/700D0h
IO: Base/Offset:

These palette registers can be accessed through this MMIO interface or through a legacy mode using the VGA palette register locations combined with an enable bit. This is the preferred method. The cursor palette provides color information when using one of the indexed modes. In the two bit AND XOR cursor modes the two bit index selects one of the four colors or two of the colors when in the mode. RGB data is full range unsigned numbers. YUV data will be unsigned for the Y and excess 128 notation for the UV values. The data can be pre gamma corrected and bypass the gamma correction logic or passed through the gamma corrector.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** Write as zero.
23:16	RW		**RED_OR_Y:**
15:8	RW		**GREEN_OR_U_VALUE:**
7:0	RW		**BLUE_OR_V_VALUE:**

1.11.105 DISPLAY_CONTROLLER.DCLRC0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721D0h
MMIO: Base/Offset: MMADR/721D0h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:**
26:18	RW		**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast for YUV modes and for source data in RGB format is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary .
17:8	RO		**RESERVED1:**
7:0	RW		**BRIGHTNESS:** This field provides the brightness adjustment with a 8 bit 2 s compliment value ranging 128 127 . This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8 bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of 255 255 . Bypassing Brightness for YUV formats and for source data in RGB format is accomplished by programming this field to 0.

1.11.106 DISPLAY_CONTROLLER.DCLRC1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721D4h
MMIO: Base/Offset: MMADR/721D4h
IO: Base/Offset:

The sum of the absolute value of SH_SIN and SH_COS must be limited to less than 8. ABS SH_SIN ABS SH_COS lt 8

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:**
26:16	RW		**SATURATION_AND_HUE_SIN:** This 11 bit signed fixed point number is in 2 s compliment s3i.7f format with the MSB as the sign next 3 MSBs as the integer value and the last 7 LSBs as the fraction value. This field can be used in two modes. When full range YUV data is operated on this field contains the saturation value. When the range limited YCbCr data is used software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor 128 112 . Similar to the contrast field there is no limit for saturation reduction saturation 0 means all pixels become the same value. However increasing contrast can only be increased by a factor less than 8. For example the largest contrast with value of 0x7.7F can bring input range 0 32 to a full display color range of 0 255 . Bypassing Hue even for source data in RGB format is accomplished by programming this field to 0.0.

Bit	Access	Default Value	Description
15:10	RO		**RESERVED1:**
9:0	RW		**SATURATION_AND_HUE_COS:** This unsigned fixed point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value. This field can be used in two modes. When full range YUV data is operated on this field contains the saturation value. When the range limited YCbCr data is used software should program this field with the product of the saturation multiplier value multiplied by the CbCr range scale factor 128 112 . Similar to the contrast field there is no limit for saturation reduction saturation 0 means all pixels become the same value. However increasing contrast can only be increased by a factor less than 8. For example the largest contrast with value of 0x7.7F can bring input range 0 32 to a full display color range of 0 255 . Bypassing Saturation even for source data in RGB format is accomplished by programming this field to 1.0.

1.11.107 DISPLAY_CONTROLLER.DCLRKM

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30154h
MMIO: Base/Offset: MMADR/30154h
IO: Base/Offset:

This register value is mirrored from DDR in addres 54h R W . The memory Adress Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31	RO		**OVERLAY_DESTINATION_COLOR_KEY_ENABLE:** Destination keying when enabled forces the overlay surface Z order to be below the primary display. Pixels that match the key value see above become transparent and the overlay becomes visible at that pixel. The combination of source key enabled and destination key enabled is not a useful operational mode. 1 destination color key is enabled 0 destination color key is disabled
30	RO		**ENABLE_CONSTANT_ALPHA:** Overlay constant alpha provides a way to apply an alpha value to all overlay pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the overlay might still be used to generate video output. 0 Overlay Constant Alpha is disabled 1 Overlay Constant Alpha is enabled
29:24	RO		**RESERVED0:** MBZ
23:0	RO		**DESTINATION_COLOR_KEY_MASK:** 23 16 Red 15 08 Green 07 00 Blue 0 Bits that are active participants in the compare. 1 Bits that are not active participants in the compare. A mask of all ones will disable the color key compare as if all color channel values match .

1.11.108 DISPLAY_CONTROLLER.DCLRKV

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30150h
MMIO: Base/Offset: MMADR/30150h
IO: Base/Offset:

This register value is mirrored from DDR in addres 50h R W . The memory Adress Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:0	RO		**DESTINATION_COLOR_KEY_VALUE:** Destination keying causes the color of the display primary or secondary to become transparent if it is within the overlay window and matches the destination color key. The key color is specified In the format of the destination surface data converted to 24 bits which is limited to either the primary Display A or secondary display Display B . Destination keying is used only when overlay and Display Plane A or overlay and Display Plane B are on the same pipe. If both Display A and Display B are present on the same pipe as the overlay overlay destination keying only applies to Display A. Color Channel Value 23 16 Red 15 08 Green 07 00 Blue

1.11.109 DISPLAY_CONTROLLER.DOVSTA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30008h
MMIO: Base/Offset: MMADR/30008h
IO: Base/Offset:

This read only register indicates status for the overlay. Since the Overlay pipe can be assigned to either display pipe references to display are either the pipe A timing generator or the pipe B timing generator depending on which the Overlay logic is currently slaved to.

Bit	Access	Default Value	Description
31	RO		**OVERLAY_REGISTER_UPDATE_STATUS:** This status bit is only applicable to the case that software writes OVADD via either MMIO or Command Stream to trigger hardware to load the on chip overlay registers from the memory back buffer. This bit is cleared to zero by hardware when OVADD is written. It is set to one when the hardware completes loading the on chip registers. This bit in effect acknowledges that a buffer flip has completed. When flipping the overlay from one active display pipe to the other this occurs when the VBLANK of the target display pipe following the VBLANK of the current display pipe has occurred. 0 Overlay Register Update register has been written however display VBLANK event has not yet occurred and Overlay Registers have not been loaded from memory. 1 Overlay Register has not been updated since the last VBLANK event. This is the power on default value.
30:22	RO		**RESERVED0:** MBZ
21:20	RO		**OVERLAY_CURRENT_BUFFER:** This field indicates which overlay buffer is currently being displayed. It is updated at display VBLANK. The update occurs before display VBLANK interrupt. 00 Buffer 0 01 Buffer 1 1x Reserved
19	RO		**OVERLAY_CURRENT_FIELD:** This bit indicates the overlay source field currently displayed. It is updated at display VBLANK occurring before display VBLANK interrupt. It is only valid in interleaved buffer or Field mode. In non interleaved buffer or Frame mode this bit is always 0. See bit 5 of the Command Register for more on Field Frame modes . 0 Field 0 1 Field 1
18	RO		**RESERVED1:** MBZ
17	RO		**OVERLAY_HARDWARE_ERROR:** This status bit indicates that there has been an error detected during Overlay operation. It is set when the data underrun condition is detected. It s cleared by reading this register. This bit can be used in diagnostic tests to determine if there is enough memory bandwidth for a given resolution.
16	RO		**RESERVED2:**
15	RO		**RESERVED3:** MBZ
14	RO		**NOT_ACTIVE_DISPLAY_PIXEL:** This bit indicates the Display Horizontal Blank Active state of the graphics pipe

Bit	Access	Default Value	Description
			that the overlay is associated with. The Display Horizontal Blank includes the horizontal Border It is updated in real time set by the leading edge of Overlay s display HBLANK and cleared by the trailing edge of the HBLANK. 0 HBLANK inactive 1 HBLANK active
13	RO		**RESERVED4:** MBZ
12	RO		**NOT_ACTIVE_DISPLAY_SCAN_LINE:** This bit indicates the Display Vertical Blank Active state of the graphics pipe that the overlay is associated with. The Display Vertical Blank includes the vertical Border. This field is updated in real time set by leading edge of display VBLANK and cleared by the trailing edge of VBLANK. 0 VBLANK inactive 1 VBLANK active
11:0	RO		**RESERVED5:** MBZ

1.11.110 DISPLAY_CONTROLLER.DOVSTAEX

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3000Ch
MMIO: Base/Offset: MMADR/3000Ch
IO: Base/Offset:

This read only register provides extended status information about the overlay. The format is RESERVED.

Bit	Access	Default Value	Description
31:0	RO		**RESERVED0:** MBZ

1.11.111 DISPLAY_CONTROLLER.DPALETTE_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//0A000h
MMIO: Base/Offset: MMADR/0A000h
IO: Base/Offset:

Table 8206 1 8209 2. 8 Bit Mode

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**PIPE_A_RED_PALETTE_ENTRY:**
15:8	RW		**PIPE_A_GREEN_PALETTE_ENTRY:**
7:0	RW		**PIPE_A_BLUE_PALETTE_ENTRY:**

1.11.112 DISPLAY_CONTROLLER.DPALETTE_B

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//0A800h

MMIO: Base/Offset: MMADR/0A800h
IO: Base/Offset:

8 Bit Mode

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** Read Only.
23:16	RW		**PIPE_B_RED_PALETTE_ENTRY:**
15:8	RW		**PIPE_B_GREEN_PALETTE_ENTRY:**
7:0	RW		**PIPE_B_BLUE_PALETTE_ENTRY:**

1.11.113 DISPLAY_CONTROLLER.DPB_AUX_CH_CTL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64110h
MMIO: Base/Offset: MMADR/64110h
IO: Base/Offset:

Description AuxB control dprrega_b0.v auxb_ctl_rdback Programming note Do not change any fields while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31	RW		**SEND_BUSY:** Setting this bit to a one initiates the transaction when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	RW		**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event.
29	RW		**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	RW		**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event.
27:26	RW		**TIME_OUT_TIMER_VALUE:** 00 400us default 01 600us 10 800us 11 1600us The time count depends on the 2X bit clock divider bits 10 0 being programmed for 2MHz.
25	RW		**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted not in multiples of a full byte or more than 20 bytes. SW must write a 1 to this bit to clear the event.
24:20	RW		**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit including the header . It also indicates the number of bytes received in a transaction including the header . This field is valid only when the done bit is set and timeout or receive error has not occurred. Sync Stop are not part of the message or the message size. The read value will not be valid while Busy bit 31 is

Bit	Access	Default Value	Description
			asserted. Message sizes of 0 or gt 20 are not allowed.
19:16	RW		**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider bits 10 0 being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example For 12us precharge program 6 12us 2us .
15	RW		**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the AKSV buffer for HDCP authentication or all from the AUX Data registers. Set this bit before initiating a transaction to write AKSV to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header then the DP_AUX_CH_AKSV_HI then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the AKSV buffer simultaneously. 0 Default Use AUX Data registers for regular data transmission 1 Use AKSV Buffer for part of the data transmission.
14	RW		**INVERT_MANCHESTER:** 1 Manchester code rising edge mid clk signifies one test mode 0 Manchester code rising edge mid clk signifies zero default
13	RW		**SYNC_ONLY_CLOCK_RECOVERY:** 1 Only recover clock during sync pattern test mode 0 Recover clock during sync pattern and data phase default
12	RW		**DISABLE_DE_GLITCH:** 1 Disable serial input de glitch logic test mode 0 Enable serial input de glitch logic default
11	RW		**DOUBLE_PRECHARGE:** 1 Precharge time is doubled 0 Precharge time is as programmed
10:0	RW		**X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz 0.5us . DevCTG A the input clock is cdclk. DevCTG B Dev Intel Atom Processor D2000 series and N2000 Series the input clock is hrawclk 200MHz Example For300MHz input clock and desired2MHz 2X bit clock program 150 300MHz 2MHz .

1.11.114 DISPLAY_CONTROLLER.DPB_AUX_CH_DATA1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64114h
MMIO: Base/Offset: MMADR/64114h
IO: Base/Offset:

Description AuxB Data1 dprrega_b0.v auxb_dpr_data1 ql_auxb_d1 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA131:** 0 The first DWORD of the message. The Msbyte is transmitted first. Reads will give the response data after transaction complete.

1.11.115 DISPLAY_CONTROLLER.DPB_AUX_CH_DATA2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64118h
MMIO: Base/Offset: MMADR/64118h
IO: Base/Offset:

Description AuxB Data2 dprrega_b0.v auxb_dpr_data2 ql_auxb_d2 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA231:** 0 The second DWORD of the message. The Msbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

1.11.116 DISPLAY_CONTROLLER.DPB_AUX_CH_DATA3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6411Ch
MMIO: Base/Offset: MMADR/6411Ch
IO: Base/Offset:

Description AuxB Data3 dprrega_b0.v auxb_dpr_data3 ql_auxb_d3 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA331:** 0 The third DWORD of the message. The Msbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

1.11.117 DISPLAY_CONTROLLER.DPB_AUX_CH_DATA4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64120h
MMIO: Base/Offset: MMADR/64120h
IO: Base/Offset:

Description AuxB Data4 dprrega_b0.v auxb_dpr_data4 ql_auxb_d4 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA431:** 0 The fourth DWORD of the message. The Msbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

1.11.118 DISPLAY_CONTROLLER.DPB_AUX_CH_DATA5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64124h
MMIO: Base/Offset: MMADR/64124h
IO: Base/Offset:

Description AuxB Data5 dprrega_b0.v auxb_dpr_data5 ql_auxb_d5 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA531:** 0 The fifth DWORD of the message. The Msbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

1.11.119 DISPLAY_CONTROLLER.DPC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64200h
MMIO: Base/Offset: MMADR/64200h
IO: Base/Offset:

Description Display Port C control dprrega_b0.v ql_displayc1 Please note that DisplayPort C uses the same lanes as HDMIC. Therefore HDMIC and DisplayPort C cannot be enabled simultaneously.

Bit	Access	Default Value	Description
31	RW		**DISPLAYPORT_C_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. 1 Enable. This bit enables the Display Port C interface. 0 Disable and tristates the Display Port C interface.
30	RW		**PIPE_SELECT:** This bit determines from which display pipe

Bit	Access	Default Value	Description
			the source data will originate. Pipe selection takes place on the Vblank after being written 0 Pipe A 1 Pipe B
29:28	RW		**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled Repetition of D10.2 characters Default. 01 Pattern 2 enabled Repetition of K28.5 D11.6 K28.5 D11.6 D10.2 D10.2 D10.2 D10.2 D10.2 D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled Transmit BS followed by VB ID with NoVideoStream_flag set to 1 five times 11 Link not in training Send normal pixels
27:25	RW		**VOLTAGE_SWING_LEVEL_SET_DEVCTG:** These bits are used for setting the voltage swing for pattern 1 defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 0.4V DEFAULT 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED Dev Intel Atom Processor D2000 series and N2000 Series Reserved
24:22	RW		**PRE_EMPHASIS_LEVEL_SET_DEVCTG:** These bits are used for setting link pre emphasis for pattern 2 as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. 000 no pre emphasis default 001 3.5dB pre emphasis 1.5x 010 6dB pre emphasis 2x 011 9.5dB pre emphasis 3x RESERVED 1xx RESERVED Dev Intel Atom Processor D2000 series and N2000 Series Reserved
21:19	RW		**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 001 x2 Mode. 010 RESERVED 011 x4 Mode. 1xx RESERVED
18	RW		**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 Default Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re enabled
17:16	RO		**RESERVED0:** MBZ
15	RW		**PORT_REVERSAL_DEVCTG:** Locked once port is enabled. Updates when the port is disabled then re enabled Dev Intel Atom Processor D2000 series and N2000 Series Reserved
14	RO		**RESERVED1:** MBZ
13	RW		**CLOCK_OUTPUT_ENABLE:** This bit enables the bit clock output on the display port. It is for test purposes only and is output on lane 15 of the PEG interface. Please note that clock output can be enabled only on one DP port at a time. 0 Default Clock output disabled 1 Clock output enabled
12	RW		**SCRAMBLING_DISABLE_DEVCTG_B_STEP_ONLY_DEVCDV:** This bit disables scrambling for this port. 0 Scrambling enabled Default 1 Scrambling disabled no SR after

Bit	Access	Default Value	Description
			initialization at loop 2 of training
11:9	RO		**RESERVED2:** MBZ
8	RW		**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs. 0 Apply full 0 255 color range to the output Default 1 Apply 16 235 color range to the output
7	RO		**RESERVED3:** MBZ
6	RO		**RESERVED_FOR_AUDIO_OUTPUT_ENABLE4:**
5	RW		**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own but must be used in conjunction with HDCP registers. Programming note HDCP can only be selected on one port at a time. If two or more ports are selected encryption will be disabled. 0 Default No HDCP encryption on this port 1 Enable HDCP on this port
4:3	RW		**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes these bits have no effect. In native VGA modes sync polarity is determined by VRshr3c2d76b 7 6 the VGA polarity bits in VGA control. 00 VS and HS are active low inverted 01 VS is active low inverted HS is active high 10 VS is active high HS is active low inverted 11 Default VS and HS are active high
2	RW		**DIGITAL_DISPLAY_C_DETECTED:** Read only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port sDVO B C data line at boot. 0 digital display not detected during initialization 1 digital display detected during initialization Default
1:0	RO		**RESERVED5:** MBZ

1.11.120 DISPLAY_CONTROLLER.DPC_AUX_CH_CTL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64210h
MMIO: Base/Offset: MMADR/64210h
IO: Base/Offset:

Description AuxC Data1 dprrega_b0.v auxc_dpr_data1 ql_auxc_d1 Programming note Do not change any fields while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31	RW		**SEND_BUSY:** Setting this bit to a one initiates the transaction when read this bit will be a 1 until the transmission completes. The transaction is completed when the response is received or when a timeout occurs. Do not write a 1 again until transaction completes. Writes of 0 will be ignored.
30	RW		**DONE:** A sticky bit that indicates the transaction has completed. SW must write a 1 to this bit to clear the event.

Bit	Access	Default Value	Description
29	RW		**INTERRUPT_ON_DONE:** Enable an interrupt in the hotplug status register when the transaction completes or times out.
28	RW		**TIME_OUT_ERROR:** A sticky bit that indicates the transaction has timed out. SW must write a 1 to this bit to clear the event.
27:26	RW		**TIME_OUT_TIMER_VALUE:** 00 400us default 01 600us 10 800us 11 1600us The time count depends on the 2X bit clock divider bits 10 0 being programmed for 2MHz.
25	RW		**RECEIVE_ERROR:** A sticky bit that indicates that the data received was corrupted not in multiples of a full byte or more than 20 bytes. SW must write a 1 to this bit to clear the event.
24:20	RW		**MESSAGE_SIZE:** This field is used to indicate the total number bytes to transmit including the header . It also indicates the number of bytes received in a transaction including the header . This field is valid only when the done bit is set and timeout or receive error has not occurred. Sync Stop are not part of the message or the message size. The read value will not be valid while Busy bit 31 is asserted. Message sizes of 0 or gt 20 are not allowed.
19:16	RW		**PRECHARGE_TIME:** Used to determine the precharge time for the Aux Channel drivers. The value is the number of microseconds times 2. This depends on the 2X bit clock divider bits 10 0 being programmed for 2MHz. Default is 5 decimal which gives 10us of precharge. Example For 12us precharge program 6 12us 2us .
15	RW		**AUX_AKSV_BUFFER_SELECT:** This bit selects whether some of the data to be written over Display Port AUX comes from the AKSV buffer for HDCP authentication or all from the AUX Data registers. Set this bit before initiating a transaction to write AKSV to the Display Port sink. All AUX protocol must be followed and Message Size set to 9 bytes. The first DWord transmitted will be from the AUX Data Register 1 for the header then the DP_AUX_CH_AKSV_HI then the last byte from DP_AUX_CH_AKSV_LO. The sink response is read back as usual from the AUX Data registers. More than one AUX channel can select to use the AKSV buffer simultaneously. 0 Default Use AUX Data registers for regular data transmission 1 Use AKSV Buffer for part of the data transmission.
14	RW		**INVERT_MANCHESTER:** 1 Manchester code rising edge mid clk signifies one test mode 0 Manchester code rising edge mid clk signifies zero default
13	RW		**SYNC_ONLY_CLOCK_RECOVERY:** 1 Only recover clock during sync pattern test mode 0 Recover clock during sync pattern and data phase default
12	RW		**DISABLE_DE_GLITCH:** 1 Disable serial input de glitch logic test mode 0 Enable serial input de glitch logic default
11	RW		**DOUBLE_PRECHARGE:** 1 Precharge time is doubled 0 Precharge time is as programmed

Bit	Access	Default Value	Description
10:0	RW		**X_BIT_CLOCK_DIVIDER:** Used to determine the 2X bit clock the Aux Channel logic runs on. This value divides the input clock frequency down to 2X bit clock rate. The 2X bit clock rate is ideally 2MHz 0.5us . DevCTG A the input clock is cdclk. DevCTG B the input clock is hrawclk. Example For300MHz input clock and desired2MHz 2X bit clock program 150 300MHz 2MHz .

1.11.121 DISPLAY_CONTROLLER.DPC_AUX_CH_DATA1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64214h
MMIO: Base/Offset: MMADR/64214h
IO: Base/Offset:

Description AuxC Data1 dprrega_b0.v auxc_dpr_data1 ql_auxc_d1 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA131:** 0 The first DWord of the message. The MSbyte is transmitted first. Reads will give the response data after transaction complete.

1.11.122 DISPLAY_CONTROLLER.DPC_AUX_CH_DATA2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64218h
MMIO: Base/Offset: MMADR/64218h
IO: Base/Offset:

Description AuxC Data2 dprrega_b0.v auxc_dpr_data2 ql_auxc_d2 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA231:** 0 The second DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 4. Reads will give the response data after transaction complete.

1.11.123 DISPLAY_CONTROLLER.DPC_AUX_CH_DATA3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6421Ch
MMIO: Base/Offset: MMADR/6421Ch
IO: Base/Offset:

Description AuxC Data3 dprrega_b0.v auxc_dpr_data3 ql_auxc_d3 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA331:** 0 The third DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 8. Reads will give the response data after transaction complete.

1.11.124 DISPLAY_CONTROLLER.DPC_AUX_CH_DATA4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64220h
MMIO: Base/Offset: MMADR/64220h
IO: Base/Offset:

Description AuxC Data4 dprrega_b0.v auxc_dpr_data4 ql_auxc_d4 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA431:** 0 The fourth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 12. Reads will give the response data after transaction complete.

1.11.125 DISPLAY_CONTROLLER.DPC_AUX_CH_DATA5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64224h
MMIO: Base/Offset: MMADR/64224h
IO: Base/Offset:

Description AuxC Data5 dprrega_b0.v auxc_dpr_data5 ql_auxc_d5 The read value will not be valid while Busy bit 31 is asserted.

Bit	Access	Default Value	Description
31:0	RW		**AUX_CH_DATA531:** 0 The fifth DWord of the message. The MSbyte is transmitted first. Only used if the message size is greater than 16. Reads will give the response data after transaction complete.

1.11.126 DISPLAY_CONTROLLER.DPIO_DATA_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//02104h 02107h
MMIO: Base/Offset: MMADR/02104h 02107h
IO: Base/Offset:

Description Data of DPIO indirect

Bit	Access	Default Value	Description
31:0	RW		**SIDEBAND_DATA:** Sideband data register. When the operation triggered by writing to DPIO Packet register is read transaction the completion read data is stored in this register and is valid when the Busy bit of the DPIO Packet Register is cleared. When the operation triggered by writing to DPIO Packet register is write transaction the write data used for the transaction is taken from this register

1.11.127 DISPLAY_CONTROLLER.DPIO_PACKET_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//02100 02103h
MMIO: Base/Offset: MMADR/02100 02103h
IO: Base/Offset:

Description Control and Address of DPIO indirect

Bit	Access	Default Value	Description
31:16	RW		**DPIO_OFFSET:** The Offset DPIO register internal offset to be used by the triggered transaction
15:2	RO		**RESERVED0:**
1	RW		**DPIO_READ_WRITE:** The DPIO read write attribute to be used by the triggered transaction. Writing 0b to this field will trigger read transaction. Writing 1b to this field will trigger write transaction
0	RW		**DPIO_BUSY:** A status bit to be polled by SW before next DPIO access. When this bit is set none of the DPIO can be written. In case of read transaction data will be ready at DPIO Data Register only when this bit is cleared

1.11.128 DISPLAY_CONTROLLER.DPLLAMD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//0601Ch
MMIO: Base/Offset: MMADR/0601Ch
IO: Base/Offset:

Description Pipe A multiply cpdmmreg.v reg15_lt

Bit	Access	Default Value	Description
31:30	RO		**RESERVED0:**
23:22	RO		**RESERVED1:**
21:16	RW		**DPLL_A_HDMI_DIVIDER:** VGA When the source is VGA these bits specify the HDMI divider. The format of this field is the same as that of the hi res divider.
15:14	RO		**RESERVED2:**
13:8	RW		**DPLL_A_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register multiplication factor 1 Default 000000 1X Range 0 63 1X 64X
7:6	RO		**RESERVED3:**
5:0	RW		**DPLL_A_SDVO_HDMI_MULTIPLIER_VGA:** When the source is VGA these bits specify the HDMI multiplier. The format of this field is the same as that of the hi res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register multiplication factor 1 Default 000011 4X Range 0 63 1X 64X

1.11.129 DISPLAY_CONTROLLER.DPLLA_CTRL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//06014h
MMIO: Base/Offset: MMADR/06014h
IO: Base/Offset:

Description DPLL A Control cpdmmreg.v reg03_lt

Bit	Access	Default Value	Description
31	RW		**DPLL_A_VCO_ENABLE:** Disabling the PLLA will cause the display dot clock to stop. 0 DPLLA is disabled in its lowest power state default 1 DPLLA is enabled and operational 42usec until lock without calibration and 110usec for calibration
30	RO		**DEVCDV_RESERVED0:** DPLLA Serial DVO High Speed IO clock Enable
29	RW		**REFA_CLOCK_ENABLE_DEVCDV:** Indicate the reference clock of PLL A is enable 0 Disable default 1 Enable
28	RW		**VGA_MODE_DISABLE:** When in native VGA modes writes to the VGA MSR register causes the value in the selected by MSR bits VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 VGA MSR lt 3 2 gt Clock Control bits

Bit	Access	Default Value	Description
			select DPLL A Frequency 1 Disable VGA Control
27:26	RO		**DEVCDV_RESERVED1:** DPLLA Mode Select Configure the DPLLA for various supported Display Modes 00 Reserved 01 DPLLA in DAC Serial DVO UDI Integrated TV mode 10 DPLLA in LVDS mode Mobile devices ONLY otherwise RESERVED 11 DP
25:24	RO		**DEVCDV_RESERVED2:** FPA0 FPA1 P2 Clock Divide For DPLLA in LVDS mode BITS 27 26 10
23:16	RO		**DEVCDV_RESERVED3:** FPA0 FPA1 P1 Post Divisor Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b Divide by one 00000010b Divide by two 00000100b Divide by three 00001000b Divide by four 00010000b Divide by five 00100000b Divide by six 01000000b Divide by seven 10000000b Divide by Eight All other values are illegal and should not be used
15	RO		**RESERVED4:** Write as zero PLLA Lock Dev Intel Atom Processor D2000 series and N2000 Series RO 1 PLLA Lock 0 PLLA unlock
14:13	RO		**DEVCDV_RESERVED5:** PLL Reference Input Select The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder. 00 DREFCLK default is 96 MHz 01 External 25MHz 10 SDVO TVCLKIN 11 Spread spectrum input clock
12:9	RO		**DEVNCDV_RESERVED6:** Parallel to Serial Load Pulse phase selection Programmable select bits to choose the relative phase of the high speed 10X DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays phase 0 represents 1 flop delay of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 use clock phase 4 0101 use clock phase 5 0110 use clock phase 6 Default value 0111 use clock phase 7 1000 use clock phase 8 1001 use clock phase 9 1010 use clock phase 10 1011 use clock phase 11 1100 use clock phase 12 1101 use clock phase 13 Phases 0 through 3 are not available for Load Pulse selection. DevCL The following programming is recommended for Crestline based on PV timing analysis 1101 use clock phase 13 DevBLC DevCTG Reserved. Programming for load pulse is in PXP AFE config space.
8	RO		**DEVBW_DEVCL_DEVBLC_RESERVED7:** DevCTG Dev Intel Atom Processor D2000 series and N2000 Series Display Rate Switch pipe A Switching this bit transition 0 to 1 or 1 to 0 causes the DSP HW to disable and then enable the DPLL during vblank 2 row in order to switch the

Bit	Access	Default Value	Description
			frequency at the DPLL new dividers stored at the DPIO which is double buffered This bit is only available when bits 17 16 of the PIPEACONF register are 00
7:0	RO		**DEVBW_DEVCL_DEVBLC_CDV_RESERVED8:** DevCTG FPA1 P1 Post Divisor Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b Divide by one 00000010b Divide by two 00000100b Divide by three 00001000b Divide by four 00010000b Divide by five 00100000b Divide by six 01000000b Divide by seven 10000000b Divide by Eight All other values are illegal and should not be used

1.11.130 DISPLAY_CONTROLLER.DPLLBMD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//06020h
MMIO: Base/Offset: MMADR/06020h
IO: Base/Offset:

Description Pipe B multiplier cpdmmreg.v reg16_lt

Bit	Access	Default Value	Description
31:30	RO		**RESERVED0:**
23:22	RO		**RESERVED1:**
21:16	RW		**DPLL_B_HDMI_DIVIDER:** VGA When the source is VGA these bits specify the HDMI divider. The format of this field is the same as that of the hi res divider.
15:14	RO		**RESERVED2:**
13:8	RW		**DPLL_B_SDVO_HDMI_MULTIPLIER_HI_RES:** This field determines the data multiplier for sDVO and is also applied to CRT. In order to keep the clock rate to a more narrow range of rates the multiplier is set and the Display PLL programmed to a multiple of the display mode s actual clock rate. This is unrelated to the pixel multiply that is selectable per plane. 6x and higher multipliers can only be used for HDMI mode. Value in this register multiplication factor 1 Default 000011 4X Range 0 63 1X 64X
7:6	RO		**RESERVED3:**
5:0	RW		**DPLL_B_SDVO_HDMI_MULTIPLIER_VGA:** When the source is VGA these bits specify the HDMI multiplier. The format of this field is the same as that of the hi res multiplier. 6x and higher multipliers can only be used for HDMI mode. Value in this register multiplication factor 1 Default 000000 1X Range 0 63 1X 64X

1.11.131 DISPLAY_CONTROLLER.DPLLB_CTRL

PCI: B/D/F/Reg:

SBI: Port/Reg/Mem: 06h//06018h
MMIO: Base/Offset: MMADR/06018h
IO: Base/Offset:

Description DPLL B Control cpdmmreg.v reg04_lt

Bit	Access	Default Value	Description
31	RW		**DPLL_B_VCO_ENABLE:** Disabling the PLLB will cause the display dot clock to stop. 0 DPLLB is disabled in its lowest power state default 1 DPLLB is enabled and operational 42usec until lock without calibration and 110usec for calibration
30	RO		**DEVCDV_RESERVED0:** DPLLB Serial DVO High Speed IO clock Enable
29	RW		**REFB_CLOCK_ENABLE_DEVCDV:** Indicate the reference clock of PLL A is enable 0 Disable default 1 Enable
28	RW		**VGA_MODE_DISABLE:** When in native VGA modes writes to the VGA MSR register causes the value in the selected by MSR bits VGA clock control register to be loaded into the active register. This allows the VGA clock select to select the pixel frequency between the two standard VGA pixel frequencies. 0 VGA MSR lt 3 2 gt Clock Control bits select DPLL A Frequency 1 Disable VGA Control
27:26	RO		**DEVCDV_RESERVED1:** DPLLB Mode Select Configure the DPLLB for various supported Display Modes 00 Reserved 01 DPLLA in DAC Serial DVO UDI Integrated TV mode 10 DPLLA in LVDS mode Mobile devices ONLY otherwise RESERVED 11 DP
25:24	RO		**DEVCDV_RESERVED2:** FPB0 FPB1 P2 Clock Divide For DPLLB in LVDS mode BITS 27 26 10
23:16	RO		**DEVCDV_RESERVED3:** FPB0 FPB1 P1 Post Divisor Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b Divide by one 00000010b Divide by two 00000100b Divide by three 00001000b Divide by four 00010000b Divide by five 00100000b Divide by six 01000000b Divide by seven 10000000b Divide by Eight All other values are illegal and should not be used
15	RO		**RESERVED4:** Write as zero PLLB Lock Dev Intel Atom Processor D2000 series and N2000 Series RO 1 PLLB Lock 0 PLLB unlock
14:13	RO		**DEVCDV_RESERVED5:** PLL Reference Input Select The PLL reference should be selected based on the display device that is being driven. The standard reference clock is used for CRT modes using the analog display port or LCD panels for both the sDVO connected transmitter or the integrated LVDS. TV Clock in should be selected when driving an sDVO connected TV encoder. 00 DREFCLK default is 96 MHz 01 External 25MHz 10 SDVO TVCLKIN 11 Spread spectrum input clock
12:9	RO		**DEVCDV_RESERVED6:** Parallel to Serial Load Pulse

Bit	Access	Default Value	Description
			phase selection Programmable select bits to choose the relative phase of the high speed 10X DPLL clock used for generating the parallel to serial load pulse for digital display port on PCIe. The relative phase is the number of flop delays phase 0 represents 1 flop delay of the 1X parallel data synchronization signal in the 10X clock domain. The earliest selectable clock phase is 4. A phase selection of 10 or greater simply extends the flop delay count to sample delayed data. 0100 use clock phase 4 0101 use clock phase 5 0110 use clock phase 6 Default value 0111 use clock phase 7 1000 use clock phase 8 1001 use clock phase 9 1010 use clock phase 10 1011 use clock phase 11 1100 use clock phase 12 1101 use clock phase 13 Phases 0 through 3 are not available for Load Pulse selection. DevCL The following programming is recommended for Crestline based on PV timing analysis 1101 use clock phase 13 DevBLC DevCTG Reserved. Programming for load pulse is in PXP AFE config space.
8	RO		**DEVBW_DEVCL_DEVBLC_RESERVED7:** DevCTG Dev Intel Atom Processor D2000 series and N2000 Series Display Rate Switch pipe B Switching this bit transition 0 to 1 or 1 to 0 causes the DSP HW to disable and then enable the DPLL during vblank 2 row in order to switch the frequency at the DPLL new dividers stored at the DPIO which is double buffered This bit is only available when bits 17 16 of the PIPEACONF register are 00
7:0	RO		**DEVBW_DEVCL_DEVBLC_CDV_RESERVED8:** DevCTG FPB1 P1 Post Divisor Writes to this byte cause the staging register contents to be written into the active register when in the VGA mode of operation. This will also occur when the VGA MSR register is written. 00000001b Divide by one 00000010b Divide by two 00000100b Divide by three 00001000b Divide by four 00010000b Divide by five 00100000b Divide by six 01000000b Divide by seven 10000000b Divide by Eight All other values are illegal and should not be used

1.11.132 DISPLAY_CONTROLLER.DP_AUX_CH_AKSV_HI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64130h
MMIO: Base/Offset: MMADR/64130h
IO: Base/Offset:

Description AuxB AKSV High dprrega_b0.v dpr_aux_AKSV_hi This is programmed with the lower 4 bytes of AKSV. DP_AUX_AKSV_LO should be programmed with the highest byte of AKSV. More than one AUX channel can select to use the AKSV buffer simultaneously. This will become the second DWORD of the message when AKSV buffer is selected. The first DWORD will come from the DP_AUX_CH_DATA1 register.

Bit	Access	Default Value	Description
31:24	WO		**AKSV_BITS_7:** 0
23:16	WO		**AKSV_BITS_15:** 8

15:8	WO		**AKSV_BITS_23:** 16
7:0	WO		**AKSV_BITS_31:** 24

1.11.133 DISPLAY_CONTROLLER.DP_AUX_CH_AKSV_LO

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64134h
MMIO: Base/Offset: MMADR/64134h
IO: Base/Offset:

Description AuxB AKSV High dprrega_b0.v dpr_aux_AKSV_lo This is programmed with the highest byte of AKSV. DP_AUX_AKSV_HI should be programmed with the lower 4 bytes of AKSV. More than one AUX channel can select to use the AKSV buffer simultaneously.

Bit	Access	Default Value	Description
31:8	RO		**RESERVED0:** MBZ
7:0	RW		**AKSV_BITS_39:** 32

1.11.134 DISPLAY_CONTROLLER.DP_B

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//64100h
MMIO: Base/Offset: MMADR/64100h
IO: Base/Offset:

Description Display Port B control dprrega_b0.v ql_displayb1 Please note that DisplayPort B uses the same lanes as HDMIB. Therefore HDMIB and DisplayPort B cannot be enabled simultaneously. Calculation of TU is as follows For modes that divide into the link frequency evenly Active TU payload capacity. Please note that this is the same ratio as data m n Payload capacity dot clk bytes per pixel ls_clk of lanes

Bit	Access	Default Value	Description
31	RW		**DISPLAYPORT_B_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. 1 Enable. This bit enables the Display Port B interface. 0 Disable and tristates the Display Port B interface.
30	RW		**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. Pipe selection takes place on the Vblank after being written 0 Pipe A 1 Pipe B
29:28	RW		**LINK_TRAINING_PATTERN_ENABLE:** These bits are used for link initialization as defined in the DisplayPort specification. Please note that the link must first be configured prior to sending training patterns. 00 Pattern 1 enabled Repetition of D10.2 characters Default. 01 Pattern 2 enabled Repetition of K28.5 D11.6 K28.5 D11.6 D10.2 D10.2 D10.2 D10.2 D10.2 D10.2. Please note that the entire pattern must complete before another pattern is sent. Scrambling initialization and disparity init commence at the end of the last iteration of pattern 2. 10 Idle Pattern enabled Transmit BS followed by VB ID with NoVideoStream_flag set

Bit	Access	Default Value	Description
			to 1 five times 11 Link not in training Send normal pixels
27:25	RW		**VOLTAGE_SWING_LEVEL_SET_DEVCTG:** These bits are used for setting the voltage swing for pattern 1 defined as Vdiff_pp in the DisplayPort specification. They mirror registers in the PCI express configuration at Intel Atom Processor D2000 series and N2000 Series moved to register at the DPIO 000 0.4V DEFAULT 001 0.6V 010 0.8V 011 1.2V RESERVED 1xx RESERVED Dev Intel Atom Processor D2000 series and N2000 Series Reserved
24:22	RW		**PRE_EMPHASIS_LEVEL_SET_DEVCTG:** These bits are used for setting link pre emphasis for pattern 2 as defined in the DisplayPort specification. They mirror registers in the PCI express configuration. At Intel Atom Processor D2000 series and N2000 Series this field move to register in the DPIO. 000 no pre emphasis default 001 3.5dB pre emphasis 1.5x 010 6dB pre emphasis 2x 011 9.5dB pre emphasis 3x RESERVED 1xx RESERVED Dev Intel Atom Processor D2000 series and N2000 Series Reserved
21:19	RW		**PORT_WIDTH_SELECTION:** This bit selects the number of lanes to be enabled on the DisplayPort link. Port width selection takes place on the Vblank after being written. Port width change must be done as a part of mode set. 001 x2 Mode. 010 RESERVED 011 x4 Mode. 1xx RESERVED
18	RW		**ENHANCED_FRAMING_ENABLE:** This bit selects enhanced framing. It must be set when HDCP will be used invoked. 0 Default Enhanced framing disabled 1 Enhanced framing enabled. Locked once port is enabled. Updates when the port is disabled then re enabled
17:16	RO		**RESERVED0:** MBZ
15	RW		**PORT_REVERSAL_DEVCTG:** Locked once port is enabled. Updates when the port is disabled then re enabled Dev Intel Atom Processor D2000 series and N2000 Series Reserved
14	RO		**RESERVED1:** MBZ
13	RW		**CLOCK_OUTPUT_ENABLE:** This bit enables the bit clock output on the display port. It is for test purposes only and is output on lane 15 of the PEG interface. Please note that clock output can be enabled only on one DP port at a time. 0 Default Clock output disabled 1 Clock output enabled
12	RW		**SCRAMBLING_DISABLE_DEVCTG_B_STEP_ONLY_DEV CDV:** This bit disables scrambling for this port. 0 Scrambling enabled Default 1 Scrambling disabled no SR after initialization at loop 2 of training
11:9	RO		**RESERVED2:** MBZ
8	RW		**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs. 0 Apply full 0 255 color range to the output Default 1 Apply 16 235 color range to the output
7	RO		**RESERVED3:** MBZ
6	RO		**RESERVED_FOR_AUDIO_OUTPUT_ENABLE4:**

Bit	Access	Default Value	Description
5	RW		**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own but must be used in conjunction with HDCP registers. Programming note HDCP can only be selected on one port at a time. If two or more ports are selected encryption will be disabled. 0 Default No HDCP encryption on this port 1 Enable HDCP on this port
4:3	RW		**SYNC_POLARITY:** Indicates the polarity of Hsync and Vsync. Please note that in native VGA modes these bits have no effect. In native VGA modes sync polarity is determined by VRshr3c2d76b 7 6 the VGA polarity bits in VGA control. 00 VS and HS are active low inverted 01 VS is active low inverted HS is active high 10 VS is active high HS is active low inverted 11 Default VS and HS are active high
2	RW		**DIGITAL_DISPLAY_B_DETECTED:** Read only bit indicating whether a digital display was detected during initialization. It signifies the level of the GMBUS port 4 sDVO B C data line at boot. 0 digital display not detected during initialization 1 digital display detected during initialization Default
1:0	RO		**RESERVED5:** MBZ

1.11.135 DISPLAY_CONTROLLER.DSPAADDR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7017Ch
MMIO: Base/Offset: MMADR/7017Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_A_START_ADDRESS_BITS:** This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . Write to this register triggers async flip. The async flip address is written into the Display A Base Address register 0x7019C

1.11.136 DISPLAY_CONTROLLER.DSPACNTR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70180h
MMIO: Base/Offset: MMADR/70180h
IO: Base/Offset:

Notes The active set of registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls. If the currently selected pipe is disabled the update is immediate.

Bit	Access	Default Value	Description
31	RW		**DISPLAY_PLANE_A_ENABLE:** When this bit is set the primary plane will generate pixels for display. When set to zero display plane A memory fetches cease and display is blanked from this plane at the next VBLANK event from the pipe that display A is assigned. The display pipe must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 Enable 0 Disable
30	RW		**DISPLAY_A_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane s pixel data only. For 8 bit indexed display data this bit should be set to a one. 0 Display A pixel data bypasses the display pipe gamma correction logic default . 1 Display A pixel data is gamma corrected in the display pipe gamma correction logic.
29:26	RW		**DISPLAY_A_SOURCE_PIXEL_FORMAT:** These bits should only be changed after the plane has been disabled. Pixel formats with an alpha channel 8 8 8 8 should not use source keying. Pixel format of 8 bit indexed uses the palette. Before entering the blender each source format is converted to 10 bits per pixel details are described in the intermediate precision for the blender section of the Display Functions chapter . 000x Reserved. 0010 8 bpp Indexed. 0011 Reserved. 0100 Reserved. 0101 16 bit BGRX 5 6 5 0 pixel format XGA compatible . 0110 32 bit BGRX 8 8 8 8 pixel format. Ignore alpha. 0111 Reserved. 1000 32 bit RGBX 10 10 10 2 pixel format. Ignore alpha. 1001 Reserved. 1010 BGRX 10 10 10 2 1011 Reserved. 1100 64 bit RGBX 16 16 16 16 16 bit floating point pixel format. Ignore alpha. 1101 Reserved. 1110 32 bit RGBX 8 8 8 8 pixel format. Ignore alpha. 1111 Reserved.
25:24	RO		**DISPLAY_A_PIPE_SELECT:** This is read only and selects the display pipe that this plane is assigned to. It is hardwired to pipe A. 00 Select Pipe A default cannot be changed 01 Select Pipe B 10 Reserved for pipe C 11 Reserved for pipe D
23	RW		**KEY_WINDOW_ENABLE:** 0 Source Key applies to entire display plane A 1 Source Key applies to only pixels within the intersection between Display A and Display C DevBLC and DevCTG Reserved
22	RW		**KEY_ENABLE:** 0 Source key is disabled 1 Source key is enabled DevBLC and DevCTG Reserved
21:20	RW		**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the pixel multiply mode the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes 00 No duplication 01 Line pixel Doubling 10 Reserved 11 Pixel Doubling only
19	RO		**RESERVED0:** Software must preserve the contents of this bit.

Bit	Access	Default Value	Description
18	RO		**RESERVED1:** Write as zero
17:16	RO		**RESERVED2:** Software must preserve the contents of this bit.
15	RW		**DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit software must also set the base address to the lower right corner of the un-rotated image. DevCL Do not enable 180 rotation together with Frame Buffer Compression0 No rotation 1 180 rotation
14	RW		**DEVBLC_AND_DEVCTG_DISPLAY_A_TRICKLE_FEED_ENABLE:** 0 Trickle Feed Enabled Display A data requests are sent whenever there is space in the Display Data Buffer. 1 Trickle Feed Disabled Display A data requests are sent in bursts. Note On mobile products this bit will be ignored such that Trickle Feed is always disabled. DevELK Must always be programmed disabled DevBW DevCL Dev Intel Atom Processor D2000 series and N2000 Series Reserved
13	RW		**DEVBLC_AND_DEVCTG_DISPLAY_A_DATA_BUFFER_PARTITIONING_CONTROL:** 0 Display A Data Buffer will encompass Sprite A buffer space when Sprite A is disabled. 1 Display A Data Buffer will not use Sprite A buffer space when Sprite A is disabled. Note When in C3xR Max FIFO mode this bit will be ignored. DevBW DevCL Dev Intel Atom Processor D2000 series and N2000 Series Reserved
12:11	RO		**RESERVED3:**
10	RW		**TILED_SURFACE:** When this bit is set it affects the hardware interpretation of the DSPATILEOFF DSPALINOFF and DSPASURF registers. 0 Display A surface uses linear memory 1 Display A surface uses X tiled memory
9	RW		**DEVBLC_DEVCTG_ASYNCHRONOUS_SURFACE_ADDRESS_UPDATE_ENABLE:** This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 DSPASURF MMIO writes will update synchronous to start of vertical blank default 1 DSPASURF MMIO writes will update asynchronously DevBW DevCL Dev Intel Atom Processor D2000 series and N2000 Series Reserved Write as zero
8:0	RO		**RESERVED4:** Write as zero

1.11.137 DISPLAY_CONTROLLER.DSPAKEYMSK

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70198h
MMIO: Base/Offset: MMADR/70198h
IO: Base/Offset:

This register specifies the key mask to be used with the color value bits to determine if the display source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED_MASK_VALUE:** Specifies the color key mask for the sprite red Cr channel.
15:8	RW		**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green Y channel.
7:0	RW		**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue Cb channel.

1.11.138 DISPLAY_CONTROLLER.DSPAKEYVAL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70194h
MMIO: Base/Offset: MMADR/70194h
IO: Base/Offset:

This register specifies the key color to be used with the mask bits to determine if the display source data matches the key. This register will only have an effect when the display color key is enabled. The overlay destination key value is used for overlay keying when Display A is being used as a primary display with overlay destination keying enabled. This key can be used as a Display C destination key onto Display A.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED_KEY_VALUE:** Specifies the color key value for the sprite red Cr channel.
15:8	RW		**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green Y channel.
7:0	RW		**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue Cb channel.

1.11.139 DISPLAY_CONTROLLER.DSPALINOFF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70184h
MMIO: Base/Offset: MMADR/70184h
IO: Base/Offset:

This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. This register can be written directly through software or by load register immediate command packets in the command stream.

This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_A_OFFSET:** This register provides the panning offset into the display A plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation this offset must be the difference between the last pixel of the last line of the display data in its un-rotated orientation and the display surface address.

1.11.140 DISPLAY_CONTROLLER.DSPARB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70030h
MMIO: Base/Offset: MMADR/70030h
IO: Base/Offset:

Notes: Each active display plane A B or C requires a FIFO to cover for memory latency. The FIFOs all come from a single RAM that is divided into areas for each display plane. The amount of the RAM used by each display plane is defined by this register. The two fields in the register split the display RAM into three portions allocated between display planes A B and C. This register is double buffered and updated on the leading edge of Vertical Blank of the pipe that the planes are assigned to. This register should only be changed when a single pipe is enabled or if all of the Display A B C planes are disabled. It takes effect on the next VBLANK for whichever pipe is currently active. Each display plane needs a minimum FIFO size that is at least MaxLatencyForPlane PixelRate PixelSize 512. All values should be rounded up to the next unit of 64B. Notes A special C3 mode can occur when a single display of Display A and Display B is active and the overlay and Display C are disabled. In that mode when C3 is entered the values in the BSTART and CSTART fields are ignored and the entire RAM is allocated to the single active display plane. Notes DevBW and DevBLC The control granularity of FIFO size is 64 bytes and the total size of the RAM is 384 16 bytes making TOTALSIZE equal to 96. The range of values for CSTART and BSTART is 0 95. Notes DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series The control granularity of FIFO size is 64 bytes and the total size of the RAM is 512 16 bytes making TOTALSIZE equal to 128. The range of values for CSTART and BSTART is 0 127. Notes DevBLC and DevCTG The entire register is reserved. Hardware controls the FIFO sizing automatically. Notes DevIntel Atom Processor D2000 series and N2000 Series FIFO Sizes A 28 B 31 C 37Notes The display dot clock frequency or pixel rate must not exceed 90 of the core display clock. When a primary plane is enabled with 64bpp format and sprite is also enabled on the same pipe the dot clock frequency or pixel rate must be less than 80 of the core display clock.

Bit	Access	Default Value	Description
31:14	RO		**RESERVED0:** Write as zero.
13:7	RW		**CSTART:** This field selects the end of the ram used for display B and the start of the RAM for display C. If display B is unused this field can be set to the same value as BSTART. If display C is unused this field can be set to

			TOTALSIZE 1. It must be programmed to a number greater than or equal to the value in BSTART and less than the total size of the RAM TOTALSIZE . The size of the display B FIFO will be CSTART BSTART 64. The size of the display C FIFO will be TOTALSIZE CSTART 1 64 bytes. DevBLC and DevCTG Reserved Write as zero.
6:0	RW		**BSTART:** This field selects the end of the ram used for display A and the start of the RAM for display B. If display A is unused this field can be set to zero. The value should never exceed the size of the RAM TOTALSIZE . The size of the display A FIFO will be BSTART 64 bytes.

1.11.141 DISPLAY_CONTROLLER.DSPASTRIDE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70188h
MMIO: Base/Offset: MMADR/70188h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_A_STRIDE:** This is the stride for display A in bytes. When using linear memory this must be 64 byte aligned. When using tiled memory this must be 512 byte aligned. This value is used to determine the line to line increment for the display. This register is updated either through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory the actual memory buffer stride is limited to a maximum of 16K bytes. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series The display stride must be power of 2 when doing Asynch Flips. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.

1.11.142 DISPLAY_CONTROLLER.DSPASURF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7019Ch
MMIO: Base/Offset: MMADR/7019Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:**
28:12	RW		**DISPLAY_A_SURFACE_BASE_ADDRESS:** This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory this address must be 256K aligned. This register can be written directly

			through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL This address must be 128K aligned for linear memory.
11:0	RO		**RESERVED1:**

1.11.143 DISPLAY_CONTROLLER.DSPASURFLIVE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//701ACh
MMIO: Base/Offset: MMADR/701ACh
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO		**DISPLAY_A_LIVE_SURFACE_BASE_ADDRESS:**

1.11.144 DISPLAY_CONTROLLER.DSPATILEOFF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//701A4h
MMIO: Base/Offset: MMADR/701A4h
IO: Base/Offset:

This register specifies the panning for the display surface. The surface base address is specified in the DSPASURF register and this register is used to describe an offset from that base address. Bit 10 of DSPACNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPALINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VBLANK only. A change to this register will take effect on the next vblank following the write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the un-rotated orientation.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the un-rotated orientation. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series When display stride is 16KB and doing

Bit	Access	Default Value	Description
			Asynch Flips do not program the offset to give pans of 7680 to 8191 bytes.

1.11.145 DISPLAY_CONTROLLER.DSPBADDR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7117Ch
MMIO: Base/Offset: MMADR/7117Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_B_START_ADDRESS_BITS:** This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . Write to this register triggers async flip The async flip address is written into the Display B Base Address register 0x7119C

1.11.146 DISPLAY_CONTROLLER.DSPBCNTR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71180h
MMIO: Base/Offset: MMADR/71180h
IO: Base/Offset:

The active set of registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls. If the currently selected pipe is disabled the update is immediate.

Bit	Access	Default Value	Description
31	RW		**DISPLAY_B_SPRITE_ENABLE:** This bit will enable or disable the display B sprite. When this bit is set the plane will generate pixels for display. When set to zero memory fetches cease and display is blanked from this plane at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. 1 Enable 0 Disable
30	RW		**DISPLAY_B_SPRITE_GAMMA_ENABLE:** This bit should only be changed after the plane has been disabled. It controls the bypassing of the display pipe gamma unit for this display plane pixel data only. For 8 bit indexed display data this bit should be set to a one. 0 Display B pixel data

Bit	Access	Default Value	Description
			bypasses the pipe gamma correction logic default . 1 Display B pixel data is gamma corrected in the pipe gamma correction logic
29:26	RW		**DISPLAY_B_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite display B. Pixel formats with an alpha channel 8 8 8 8 should not use source keying. Before entering the blender each source format is converted to 10 bits per pixel details are described in the intermediate precision for the blender section of the Display Functions chapter . 000x Reserved. 0010 8 bpp Indexed. 0011 Reserved. 0100 Reserved. 0101 16 bit BGRX 5 6 5 0 pixel format XGA compatible . 0110 32 bit BGRX 8 8 8 8 pixel format. Ignore alpha. 0111 Reserved. 1000 32 bit RGBX 10 10 10 2 pixel format. Ignore alpha. 1001 Reserved. 1010 BGRX 10 10 10 2 1011 Reserved. 1100 64 bit RGBX 16 16 16 16 16 bit floating point pixel format. Ignore alpha. 1101 Reserved. 1110 32 bit RGBX 8 8 8 8 pixel format. Ignore alpha. 1111 Reserved.
25:24	RO		**DISPLAY_B_SPRITE_PIPE_SELECT:** This is read only and selects the display pipe that this plane is assigned to. It is hardwired to pipe B. 00 Select Pipe A 01 Select Pipe B default cannot be changed 10 Reserved for pipe C 11 Reserved for pipe D
23	RW		**KEY_WINDOW_ENABLE:** This applies only to devices with a Display Plane C. It determines what area of the screen the source key compare should be applied. This bit is set to one when the color key is used as a destination key for display C. Display plane C must be enabled on the same pipe and display A should not be enabled on this pipe for this to be used. The function is only effective when display C is enabled and defined by Z order to be behind display B. 0 If keying is enabled it applies to the entire display B plane 1 If keying is enabled it applies only to the intersection between display B and display C DevBLC and DevCTG Reserved
22	RW		**SOURCE_KEY_ENABLE:** When used as a sprite or a secondary this enables source color keying. Sprite pixel values that match the key will become transparent. Source keying allows a plane that is behind below this plane to show through where the display B data matches the display B key. This function is overloaded to provide display C destination keying when combined with the key window enable bit.. Setting this bit is not allowed when the display pixel format includes an alpha channel. 0 Sprite source key is disabled default 1 Sprite source key is enabled. DevBLC and DevCTG Reserved
21:20	RW		**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line pixel doubling mode the horizontal pixels are doubled and lines are sent twice. Asynchronous flips are not used in this mode. Programming Notes 00 No duplication 01 Line pixel Doubling 10 Reserved 11 Pixel Doubling only
19:16	RO		**RESERVED0:** Write as zero

Bit	Access	Default Value	Description
15	RW		**DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit software must also set the base address to the lower right corner of the un-rotated image. DevCL Do not enable 180 rotation together with Frame Buffer Compression 0 No rotation 1 180 rotation
14	RW		**DEVBLC_DEVCTG_DISPLAY_B_TRICKLE_FEED_ENABLE:** 0 Trickle Feed Enabled Display B data requests are sent whenever there is space in the Display Data Buffer. 1 Trickle Feed Disabled Display B data requests are sent in bursts. Note On mobile products this bit will be ignored such that Trickle Feed is always disabled. DevELK Must always be programmed disabled DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Reserved
13	RW		**DEVBLC_DEVCTG_DISPLAY_B_DATA_BUFFER_PARTITIONING_CONTROL:** 0 Display B Data Buffer will encompass Sprite B buffer space when Sprite B is disabled. 1 Display B Data Buffer will not use Sprite B buffer space when Sprite B is disabled. Note When in C3xR Max FIFO mode this bit will be ignored. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Reserved
12:11	RO		**RESERVED1:**
10	RW		**TILED_SURFACE:** This bit indicates that the display B surface data is in tiled memory. The tile pitch is specified in bytes in the DSPBSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set it affects the hardware interpretation of the DSPBLINOFF DSPBTILEOFF and DSPBSURF registers. 0 Display B surface uses linear memory 1 Display B surface uses X tiled memory
9	RW		**DEVBLC_DEVCTG_ASYNCHRONOUS_SURFACE_ADDRESS_UPDATE_ENABLE:** This bit will enable asynchronous updates of the surface address when written by MMIO. The surface address will change with the next TLB request or when start of vertical blank is reached. Updates during vertical blank may not complete until after the first few active lines are displayed. Restrictions No command streamer initiated surface address updates are allowed when this bit is enabled. Only one asynchronous update may be made per frame. Must wait for vertical blank before again writing the surface address register. 0 DSPBSURF MMIO writes will update synchronous to start of vertical blank default 1 DSPBSURF MMIO writes will update asynchronously DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Reserved Write as zero
8:1	RO		**RESERVED2:** Write as zero
0	RO		**RESERVED3:** Write as zero

1.11.147 DISPLAY_CONTROLLER.DSPBFLPQSTAT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71200h
MMIO: Base/Offset: MMADR/71200h

IO: Base/Offset:

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:** Write as zero RO
15:8	RO		**QUEUE_FREE_ENTRY_COUNT:** This value indicates the number of free entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.
7:0	RO		**QUEUE_OCCUPIED_ENTRY_COUNT:** This value indicates the number of occupied entries in the queue at the time that the register was read. The total number of entries in the queue is the sum of the occupied entry count and the free entry count.

1.11.148 DISPLAY_CONTROLLER.DSPBKEYMSK

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71198h
MMIO: Base/Offset: MMADR/71198h
IO: Base/Offset:

This register specifies the key mask to be used with the color value bits to determine if the sprite source data matches the key when enabled. A zero bit in the mask indicates that the corresponding bit match failure should be ignored when determining if the pixel matches.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED_MASK_VALUE:** Specifies the color key mask for the sprite red Cr channel.
15:8	RW		**GREEN_MASK_VALUE:** Specifies the color key mask for the sprite green Y channel.
7:0	RW		**BLUE_MASK_VALUE:** Specifies the color key mask for the sprite blue Cb channel.

1.11.149 DISPLAY_CONTROLLER.DSPBKEYVAL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71194h
MMIO: Base/Offset: MMADR/71194h
IO: Base/Offset:

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The overlay destination key value is used for overlay keying when Display B is being used as a secondary display with overlay destination keying enabled.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED_KEY_VALUE:** Specifies the color key value for the sprite red Cr channel.
15:8	RW		**GREEN_KEY_VALUE:** Specifies the color key value for the sprite green Y channel.
7:0	RW		**BLUE_KEY_VALUE:** Specifies the color key value for the sprite blue Cb channel.

1.11.150 DISPLAY_CONTROLLER.DSPBLINOFFSET

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71184h
MMIO: Base/Offset: MMADR/71184h
IO: Base/Offset:

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_B_OFFSET:** This register provides the panning offset into the display B plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation this offset must be the difference between the last pixel of the last line of the display data in its un-rotated orientation and the display surface address.

1.11.151 DISPLAY_CONTROLLER.DSPBSTRIDE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71188h
MMIO: Base/Offset: MMADR/71188h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_B_SPRITE_STRIDE:** This is the stride for display B Sprite in bytes. When using linear memory this must be 64 byte aligned. When using tiled memory this must be 512 byte aligned. The maximum value for this register is fixed. This register is updated through a

Bit	Access	Default Value	Description
			command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory the actual memory buffer stride is limited to a maximum of 16K bytes. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series The display stride must be power of 2 when doing Asynch Flips. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series The display stride must be 8KB or greater when doing Asynch Flips together with 180 rotation. The value in this register is updated through the command streamer during a synchronous flip.

1.11.152 DISPLAY_CONTROLLER.DSPBSURF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7119Ch
MMIO: Base/Offset: MMADR/7119Ch
IO: Base/Offset:

Writing to this register triggers the display plane flip. When it is desired to change multiple display B registers this register should be written last as a write to this register will cause all new register values to take effect.

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:**
28:12	RW		**DISPLAY_B_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the DSPBTILEOFF register. When the surface is in linear memory panning is specified using a linear offset in the DSPBLINOFF register. This address must be 4K aligned. When performing asynchronous flips and the display surface is in tiled memory this address must be 256K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL This address must be 128K aligned for linear memory.
11:0	RO		**RESERVED1:**

1.11.153 DISPLAY_CONTROLLER.DSPBSURFLIVE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//711ACh
MMIO: Base/Offset: MMADR/711ACh
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO		**DISPLAY_B_LIVE_SURFACE_BASE_ADDRESS:**

1.11.154 DISPLAY_CONTROLLER.DSPBTILEOFF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//711A4h
MMIO: Base/Offset: MMADR/711A4h
IO: Base/Offset:

This register specifies the panning for the display surface. The surface base address is specified in the DSPBSURF register and this register is used to describe an offset from that base address. Bit 10 of DSPBCNTR specifies whether the display B surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPBLINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VBLANK only. A change to this register will take effect on the next vblank following the write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the un-rotated orientation.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the un-rotated orientation. DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series When display stride is 16KB and doing Asynch Flips do not program the offset to give pans of 7680 to 8191 bytes.

1.11.155 DISPLAY_CONTROLLER.DSPCCNTR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//72180h
MMIO: Base/Offset: MMADR/72180h
IO: Base/Offset:

The active set of basic control registers will be updated on the VBlank of the currently selected pipe after the trigger register the Start Address register or the Control register when plane enable bit transitioning from a zero to a one is written thus providing an atomic update of all display controls with the exception of the Display C

color control registers. If the currently selected pipe is disabled the VBLANK of the active pipe is used. At least one pipe must be enabled and running for the display plane to be enabled.

Bit	Access	Default Value	Description
31	RW		**DISPLAY_C_SPRITE_ENABLE:** This bit will enable or disable the display C sprite. When this bit is set the plane will generate pixels for display to be combined by the blender for the target pipe. When set to zero memory fetches cease and display is blanked from this plane at the next VBLANK event from the pipe that this plane is assigned. At least one of the display pipes must be enabled to enable this plane. There is an override for the enable of this plane in the Pipe Configuration register. This bit only has an effect when the plane is not trusted. When the plane is marked trusted this bit will be overridden and the display disabled when the registers are unlocked. 1 Enable 0 Disable
30	RW		**DISPLAY_C_SPRITE_GAMMA_ENABLE:** There are two gamma adjustments possible in the display C data path. This bit controls the gamma correction in the display pipe not the gamma control in this plane. It affects only the pixel data from this display plane. For pixel format of 8 bit indexed this bit should be set to a one. Gamma correction logic that is contained in the display C logic is disabled by loading the default values into those registers. When this plane is marked as trusted this bit should always be set to zero to force the pipe gamma to be always be bypassed. 0 Display C pixel data bypasses the display pipe gamma correction logic default . 1 Display C pixel data is gamma corrected in the pipe gamma correction logic
29:26	RW		**DISPLAY_C_SOURCE_PIXEL_FORMAT:** This field selects the pixel format for the sprite display C. Pixel formats with an alpha channel should not use source keying. Before entering the blender each source format is converted to 10 bits per pixel details are described in the intermediate precision for the blender section of the Display Functions chapter . 0000 YUV 4 2 2 packed see byte order below . 0001 Reserved 0010 8 bpp Indexed. 0011 Reserved. 0100 Reserved. 0101 16 bit BGRX 5 6 5 0 pixel format XGA compatible . 0110 32 bit BGRX 8 8 8 8 pixel format. Ignore alpha. 0111 32 bit BGRA 8 8 8 8 pixel format with pre multiplied alpha channel. 1000 32 bit RGBX 10 10 10 2 pixel format. Ignore alpha. 1001 32 bit RGBA 10 10 10 2 pixel format 1010 Reserved. 1011 Reserved. 1100 Reserved. 1101 Reserved. 1110 32 bit RGBX 8 8 8 8 pixel format. Ignore alpha. 1111 32 bit RGBA 8 8 8 8
25:24	RW		**DISPLAY_C_SPRITE_PIPE_SELECT:** This selects the display pipe that this plane is assigned to. This bit can change when the sprite is active and causes a flip to the other display pipe. The position and size is still required to fit within the pipe source rectangle. The synchronization is handled in the hardware. 00 Select Pipe A 01 Select Pipe B 10 Reserved for pipe C 11 Reserved for pipe D
23	RO		**RESERVED0:**

Bit	Access	Default Value	Description
22	RW		**SPRITE_SOURCE_KEY_ENABLE:** When used as a sprite in the 16 32 bpp modes without alpha this enables source color keying. Sprite pixel values that match within range the key will become transparent. Setting this bit is not allowed when the display C pixel format includes an alpha channel. DevBW Erratum This bit must always be set to 0 when display C pixel format is YUV 0 Sprite source key is disabled default 1 Sprite source key is enabled.
21:20	RW		**PIXEL_MULTIPLY:** This cause the display plane to duplicate lines and pixels sent to the assigned pipe. In the line pixel doubling mode the horizontal pixels are doubled and lines are sent twice. This is a method of scaling the source image by two both H and V . 00 No line Pixel duplication 01 Line Pixel Doubling 10 Reserved 11 Pixel Doubling only
19	RW		**COLOR_CONVERSION_DISABLED:** This bit enables or disables the color conversion logic. Color conversion is intended to be used with the formats that support YUV formats such as the YUV 4 2 2 packed format and x 8 8 8 and 8 8 8 8 formats. Formats such as RGB5 5 5 and 5 6 5 do not have YUV versions. 0 Pixel data is sent through the conversion logic only applies to YUV formats 1 Pixel data is not sent through the YUV gt RGB conversion logic.
18	RW		**YUV_FORMAT:** This bit specifies the source YUV format for the YUV to RGB color conversion operation. This field is ignored when source data is RGB. 0 ITU R Recommendation BT.601 1 ITU R Recommendation BT.709
17:16	RW		**YUV_BYTE_ORDER:** This field is used to select the byte order when using YUV 4 2 2 data formats. For other formats this field is ignored. 00 YUYV 01 UYVY 10 YVYU 11 VYUY
15	RW		**DISPLAY_ROTATION:** This mode causes the display plane to be rotated 180 . In addition to setting this bit software must also set the base address to the lower right corner of the un-rotated image and calculate the x y offset as relative to the lower right corner. 0 No rotation 1 180 rotation
14:11	RO		**RESERVED1:**
10	RW		**TILED_SURFACE:** This bit indicates that the display C surface data is in tiled memory. The tile pitch is specified in bytes in the DSPCSTRIDE register. Only X tiling is supported for display surfaces. When this bit is set it affects the hardware interpretation of the DSPCTILEOFF DSPCLINOFF and DSPCSURFADDR registers. 0 Display C surface uses linear memory 1 Display C surface uses X tiled memory
9:3	RO		**RESERVED2:** Write as zero
2	RW		**DISPLAY_C_BOTTOM:** This bit will force the display C plane to be on the bottom of the Z order. If the plane is marked as trusted it only applies to the Z order of the trusted planes. 0 Display C Z order is determined by the

Bit	Access	Default Value	Description
			other control bits 1 Display C is forced to be on the bottom of the Z order.
1	RO		**RESERVED3:**
0	RO		**RESERVED4:**

1.11.156 DISPLAY_CONTROLLER.DSPCCONTALPHA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721A8h
MMIO: Base/Offset: MMADR/721A8h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**ENABLE_CONSTANT_ALPHA:** Display C Sprite constant alpha provides a way to apply an alpha value to all video sprite pixels. Each pixel color channel is multiplied by the constant alpha before proceeding to the blender. This can be used to create fade out effects. This is intended for CE device use where the video sprite might still be used to generate video output. 0 Display C Sprite Constant Alpha is disabled 1 Display C Sprite Constant Alpha is enabled
30:8	RO		**RESERVED0:** MBZ
7:0	RW		**DISPLAY_C_SPRITE_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled. A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of sprite with other surfaces.

1.11.157 DISPLAY_CONTROLLER.DSPCKEYMAXVAL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721A0h
MMIO: Base/Offset: MMADR/721A0h
IO: Base/Offset:

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** Write as zero
23:16	RW		**RED_KEY_MAX_VALUE:** Specifies the color key value for the sprite red Cr channel.
15:8	RW		**GREEN_KEY_MAX_VALUE:** Specifies the color key value for the sprite green Y channel.
7:0	RW		**BLUE_KEY_MAX_VALUE:** Specifies the color key value for the sprite blue Cb channel.

1.11.158 DISPLAY_CONTROLLER.DSPCKEYMINVAL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//72194h
MMIO: Base/Offset: MMADR/72194h
IO: Base/Offset:

This register specifies the key color to be used with the mask bits to determine if the sprite source data matches the key. This register will only have an effect when the sprite color key is enabled. The unused bits of the 5 5 5 or 5 6 5 formats must be filled with duplicates of the three or two MSBs of the pixel value.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** Write as zero
23:16	RW		**RED_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite red Cr channel.
15:8	RW		**GREEN_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite green Y channel.
7:0	RW		**BLUE_KEY_MIN_VALUE:** Specifies the color key minimum value for the sprite blue Cb channel.

1.11.159 DISPLAY_CONTROLLER.DSPCKEYMSK

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//72198h
MMIO: Base/Offset: MMADR/72198h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:3	RO		**RESERVED0:** Write as zero
2	RW		**RED_CHANNEL_ENABLE:** Specifies the source color key enable for the red Cr channel.
1	RW		**GREEN_CHANNEL_ENABLE:** Specifies the source color key enable for the green Y channel.
0	RW		**BLUE_CHANNEL_ENABLE:** Specifies the source color key enable for the blue Cb channel

1.11.160 DISPLAY_CONTROLLER.DSPCLINOFF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//72184h
MMIO: Base/Offset: MMADR/72184h
IO: Base/Offset:

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the contents of this register are ignored. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . This

register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_C_OFFSET:** This register provides the panning offset into the display C plane. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset must be at least pixel aligned. This offset is the difference between the address of the upper left pixel to be displayed and the display surface address. When performing 180 rotation this offset must be the difference between the last pixel of the last line of the display data in its un-rotated orientation and the display surface address.

1.11.161 DISPLAY_CONTROLLER.DSPCLK_GATE_D

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//06200h
MMIO: Base/Offset: MMADR/06200h
IO: Base/Offset:

Description clock gating cpdmmreg.v reg12_lt

Bit	Access	Default Value	Description
31	RW		**HDCP_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
30	RW		**DP_PIPEB_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
29	RW		**VSUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
28	RW		**VRH_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
27	RW		**VRD_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
26	RW		**AUD_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
25	RW		**DP_PIPEA_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
24	RW		**DPC_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
23	RW		**TVR_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
22	RW		**TVC_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
21	RW		**TVF_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
20	RW		**TVE_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
19	RW		**DEVBW_AND_DEVCL_DVSUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
18	RW		**DDB_CLOCK_GATING_DISABLE:** 1 Disable clock gating

Bit	Access	Default Value	Description
			function
17	RW		**GMBUSUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
16	RW		**DPR_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
15	RW		**DPF_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
14	RW		**DPLR_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
13	RW		**DPLS_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
12	RW		**DPL_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
11	RW		**DPOUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
10	RW		**DPB_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
9	RW		**DC_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
8	RW		**DPGC_PIPE_B_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
7	RW		**DPGC_PIPE_A_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
6	RW		**DPIOUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
5	RW		**DEVCTG_DPFC_CLOCK_GATING_DISABLE:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Ovft Clock Gating Disable 1 Disable clock gating function
4	RW		**DEVCTG_DPFD_CLOCK_GATING_DISABLE:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Ovb Clock Gating Disable 1 Disable clock gating function
3	RW		**DEVBLC_AND_DEVCTG_DPSUNIT_PIPEB_CLOCK_GATING_DISABLE:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Ovr Clock Gating Disable 1 Disable clock gating function
2	RW		**DEVBLC_AND_DEVCTG_DPSUNIT_PIPEA_CLOCK_GATING_DISABLE:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Ovc Clock Gating Disable 1 Disable clock gating function
1	RW		**DEVBW_DEVCL_DEVCDV_OVUUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function
0	RW		**DEVBW_DEVCL_DEVCDV_OVLUNIT_CLOCK_GATING_DISABLE:** 1 Disable clock gating function

1.11.162 DISPLAY_CONTROLLER.DSPCPOS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7218Ch
MMIO: Base/Offset: MMADR/7218Ch
IO: Base/Offset:

These registers specify the screen position and size of the sprite. This register is double buffered. The load register is transferred into the active register on the asserting edge of Vertical Blank for the pipe that the display is assigned. When using the sprite as a secondary display this should be set to the entire display rectangle.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**SPRITEY_POSITION:** These 12 bits specify the vertical position in lines of the sprite upper left corner relative to the beginning of the active video area. When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**SPRITE_X_POSITION:** These 12 bits specify the horizontal position in pixels of the sprite upper left corner relative the beginning of the active video area. When performing 180 rotation this field specifies the horizontal position of the original lower right corner relative to the original end of the active video area in the un-rotated orientation. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.

1.11.163 DISPLAY_CONTROLLER.DSPCSIZE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//72190h
MMIO: Base/Offset: MMADR/72190h
IO: Base/Offset:

This register specifies the height and width of the sprite in pixels and lines. The rectangle defined by the size and position should never exceed the boundaries of the display rectangle that the sprite is assigned to.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**SPRITE_HEIGHT:** This register field is used to specify the height of the sprite in lines. The value in the register is the height minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**SPRITE_WIDTH:** This register field is used to specify the width of the sprite in pixels. This does not have to be the same as the stride but should be less than or equal to the stride converted to pixels . The value in the register is the width minus one. The defined sprite rectangle must always be completely contained within the displayable area of the screen image. The sprite width is limited to even values

			when YUV source pixel format is used actual width not the width minus one value .

1.11.164 DISPLAY_CONTROLLER.DSPCSTRIDE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//72188h
MMIO: Base/Offset: MMADR/72188h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RW		**DISPLAY_C_SPRITE_STRIDE:** This is the stride for display C Sprite in bytes. When using linear memory this must be 64 byte aligned. When using tiled memory this must be 256 byte aligned. This register is updated through a command packet passed through the command stream or writes to this register. When it is desired to update both this and the start register the stride register must be written first because the write to the start register is the trigger that causes the update of both registers on the next VBLANK event. When using tiled memory the actual memory buffer stride is limited to a maximum of 16K bytes.

1.11.165 DISPLAY_CONTROLLER.DSPCSURF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7219Ch
MMIO: Base/Offset: MMADR/7219Ch
IO: Base/Offset:

Writing to this register triggers the display plane flip. When it is desired to change multiple display C registers this register should be written last as a write to this register will cause all new register values to take effect.

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero
28:12	RW		**DISPLAY_C_SURFACE_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the DSPCTILEOFF register. When the surface is in linear memory panning is specified using a linear offset in the DSPCLINOFF register. This address must be 4K aligned. This register can be written directly through software or by command packets in the command stream. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . The value in this register is updated through the command streamer during synchronous flips. DevBW and DevCL This address must be 128K aligned for

			linear memory.
11:0	RO		**RESERVED1:** Write as zero

1.11.166 DISPLAY_CONTROLLER.DSPCTILEOFF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721A4h
MMIO: Base/Offset: MMADR/721A4h
IO: Base/Offset:

This register specifies the panning for the display surface. The surface base address is specified in the DSPCSURFADDR register and this register is used to describe an offset from that base address. Bit 10 of DSPCCNTR specifies whether the display A surface is in linear or tiled memory. When the surface is in linear memory the offset is specified in the DSPCLINOFF register and the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. If the device supports trusted operation and this plane is not marked trusted the memory pages must not be marked NoDMA . This register can be written directly through software or by load register immediate command packets in the command stream. This register is double buffered by VSYNC only. A change to this register will take effect on the next vsync following the write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**PLANE_START_Y_POSITION:** These 12 bits specify the vertical position in lines of the beginning of the active display plane relative to the display surface. When performing 180 rotation this field specifies the vertical position of the lower right corner relative to the start of the active display plane in the un-rotated orientation.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**PLANE_START_X_POSITION:** These 12 bits specify the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. When performing 180 rotation this field specifies the horizontal position of the lower right corner relative to the start of the active display plane in the un-rotated orientation.

1.11.167 DISPLAY_CONTROLLER.DWINPOS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3012Ch
MMIO: Base/Offset: MMADR/3012Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 2Ch R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** MBZ
27:16	RO		**DESTINATION_VERTICAL_TOP:** The vertical top line

Bit	Access	Default Value	Description
			position of the overlay destination window in lines. Zero means the first active display line. When performing 180 rotation this field specifies the vertical bottom line of the overlay destination window in its un-rotated orientation. The range is 0 4095 .
15:12	RO		**RESERVED1:** MBZ
11:0	RO		**DESTINATION_HORIZONTAL_LEFT:** The horizontal left position of the overlay destination window in pixels. It determines where on the display screen the overlay window will begin. Zero means the first active pixel of the display screen. When performing 180 rotation this field specifies the horizontal right position of the overlay destination window in its un-rotated orientation. The range is 0 4095 .

1.11.168 DISPLAY_CONTROLLER.DWINSZ

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30130h
MMIO: Base/Offset: MMADR/30130h
IO: Base/Offset:

This register value is mirrored from DDR in address 30h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** MBZ
27:16	RO		**DESTINATION_HEIGHT:** Overlay destination window height in lines never specifies scan lines off the active display . For devices with internal panel fitting the single line mode requires this value to be based on the panel height instead of the source height.
15:12	RO		**RESERVED1:** MBZ
11:0	RO		**DESTINATION_WIDTH:** Overlay destination window width in pixels never specifies pixels off the active display

1.11.169 DISPLAY_CONTROLLER.D_STATE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//06104
MMIO: Base/Offset: MMADR/06104
IO: Base/Offset:

Description Power state behavior cpdmmreg.v reg11_lt

Bit	Access	Default Value	Description
31:16	RW		**DPLL_LOCK_TIME:** This is the time required to the DPLL to relock. The counter using the HRAW clk 5nsec and resolution of 5nsec. SEG DPLL lock time is 42usec

Bit	Access	Default Value	Description
15	RO		**RESERVED0:** MBZ
14:8	RW		**DPLL_MIN_POWER_DOWN:** This is the minimum time required the DPLL to be power down until it is allowed to turn it on again. The HW counter using HRAW clk 5nsec and has resolution of 160nsec SEG DPLL required time is 0.5usec
7:4	RO		**RESERVED1:** MBZ
3	RW		**DOT_CLOCK_PLL_POWER_DOWN_IN_D3:** This bit determines whether the PCI Power State Powers down the Dot Clock PLLs when in D3. A 0 on this bit does not power down the DPLLs requiring software to gate them if necessary. When this bit is a 1 the dot PLLs are powered down when in D3. The PCI power state is determined by bits 1 0 of the PCI Power Management Control Status register.
2	RO		**RESERVED2:**
1	RW		**GRAPHICS_CORE_CLOCK_GATING:** This bit determines whether the PCI Power State gates the Graphics Core clocks when in the D3 state. A 0 on this bit does not gate the clocks requiring software to gate them if necessary. When this bit is a 1 the graphics core clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1 0 of the PCI Power Management Control Status register. This register field has no use in current products. DevIntel Atom Processor D2000 series and N2000 Series Reserved
0	RW		**DOT_CLOCK_GATING:** This bit determines whether the PCI Power State gates the Dot clocks when in the D3 state. A 0 on this bit does not gate the clocks requiring software to gate them if necessary. When this bit is a 1 the dot clocks are gated at the outputs of the PLLs when in D3. The PCI power state is determined by bits 1 0 of the PCI Power Management Control Status register.

1.11.170 DISPLAY_CONTROLLER.FW1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70034h
MMIO: Base/Offset: MMADR/70034h
IO: Base/Offset:

These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.

Bit	Access	Default Value	Description
31:23	RW		**DISPLAY_FIFO_SELF_REFRESH_WATERMARK:** Programming Note DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series When calculating watermark values for 15 16bpp display formats assume 32bpp for purposes of calculation using the high

Bit	Access	Default Value	Description
			priority bandwidth analysis spreadsheet.
22	RO		**RESERVED0:**
21:16	RW		**CURSOR_B_FIFO_WATERMARK:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Always program to 8.
15	RO		**RESERVED1:** MBZ
14:8	RW		**DISPLAY_PLANE_B_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display B Stream will generate requests to Memory Value should be as recommended in the high priority bandwidth analysis spreadsheet . DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Always program to 8.
7	RO		**RESERVED2:**
6:0	RW		**DISPLAY_PLANE_A_FIFO_WATERMARK:** Number in 64Bs of space in FIFO above which the Display A Stream will generate requests to Memory Value should be as recommended in the high priority bandwidth analysis spreadsheet . DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Always program to 8.

1.11.171 DISPLAY_CONTROLLER.FW2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70038h
MMIO: Base/Offset: MMADR/70038h
IO: Base/Offset:

These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.

Bit	Access	Default Value	Description
31	RW		**DEVCTG_FBC_SR_WATERMARK_ENABLE:** Enables the FBC watermarks to be used in the fetch calculation 0 disabled 1 enabled DevIntel Atom Processor D2000 series and N2000 Series Reserved
30:28	RW		**DEVCTG_FBC_SR_WATERMARK:** Number of equivalent lines of the primary display SR watermark DevIntel Atom Processor D2000 series and N2000 Series Reserved
27:24	RW		**DEVCTG_FBC_SR_HPLL_WATERMARK:** Number of equivalent lines of the primary display SR HPLL watermark. DevIntel Atom Processor D2000 series and N2000 Series Reserved
23	RO		**RESERVED0:** MBZ
22:16	RW		**DEVBLKC_DEVCTG_DISPLAY_PLANE_SPRITE_B_FIFO_WATERMARK:** DevIntel Atom Processor D2000 series and N2000 Series Reserved
15:14	RO		**RESERVED1:** MBZ

Bit	Access	Default Value	Description
13:8	RW		**CURSOR_A_FIFO_WATERMARK:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Always program to 8.
7	RO		**RESERVED2:** MBZ
6:0	RW		**DEVBLKC_DEVCTG_DISPLAY_PLANE_SPRITE_A_FIFO_WATERMARK:** DevBW DevCL Display Plane C FIFO Watermark. Number in 64Bs of space in FIFO above which the Display C Stream will generate requests to Memory Value should be as recommended in the high priority bandwidth analysis spreadsheet . DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series Always program to 8.

1.11.172 DISPLAY_CONTROLLER.FW3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//7003Ch
MMIO: Base/Offset: MMADR/7003Ch
IO: Base/Offset:

These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO.

Bit	Access	Default Value	Description
31	RW		**ENABLE_HPLL_OFF_DURING_SELF_REFRESH:** 0 Disabled 1 Enabled DevCL This bit may be enabled only if the BLC_PWM_CTL duty cycle register offset 0x61254 is programmed to 100 and non legacy backlight is enabled. This restriction does not apply when I2C is used for back light modulation. DevCL When one or more display pipes are enabled this bit should be disabled before accessing the 6XXXh MMIO register address space. Software must follow these steps Note that the wait on next vblank step requires an enabled display pipe.
30	RO		**RESERVED0:** MBZ
29:24	RW		**CURSOR_FIFO_SELF_REFRESH_WATERMARK:**
23:22	RO		**RESERVED1:** MBZ
21:16	RW		**HPLL_SELF_REFRESH_CURSOR_WATERMARK:**
15:9	RO		**RESERVED2:**
8:0	RW		**HPLL_SELF_REFRESH_DISPLAY_WATERMARK:**

1.11.173 DISPLAY_CONTROLLER.FW4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70070h
MMIO: Base/Offset: MMADR/70070h
IO: Base/Offset:

These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level. For each FIFO there are two watermarks wmark1 and wmark. When FIFO status is above wmark1 hardware generates a status of 0. When FIFO status is between wmark1 and wmark it generates a status of 2. When FIFO status is below wmark it generates a status of 3. The FIFO status is indicated by the blue color. When the FIFO is full its FIFO status is 0. The two wmark levels are shown below

Bit	Access	Default Value	Description
31	RO		**RESERVED0:** MBZ
30:24	RO		**RESERVED1:** MBZ
23	RO		**RESERVED2:** MBZ
22:16	RW		**DEVCDV_DISPLAY_SPRITE_B_FIFO_WATERMARK1:** Display Sprite B FIFO Watermark1. Number in 64Bs of space in FIFO above which the Display Sprite B Stream will generate request with status 2
15:14	RO		**RESERVED3:** MBZ
13:8	RW		**DEVCDV_CURSOR_A_FIFO_WATERMARK1:**
7	RO		**RESERVED4:** MBZ
6:0	RW		**DEVCDV_DISPLAY_SPRITE_A_FIFO_WATERMARK1:** Value should be as recommended in the high priority bandwidth analysis spreadsheet .

1.11.174 DISPLAY_CONTROLLER.FW5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70074h
MMIO: Base/Offset: MMADR/70074h
IO: Base/Offset:

These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.

Bit	Access	Default Value	Description
31	RO		**RESERVED0:** MBZ
30:24	RW		**DEVCDV_DISPLAY_B_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display B Stream will generate request with status 2
23	RO		**RESERVED1:** MBZ
22:16	RW		**DEVCDV_DISPLAY_A_FIFO_WATERMARK1:** Number in 64Bs of space in FIFO above which the Display A Stream will generate request with status 2
15:14	RO		**RESERVED2:** MBZ

Bit	Access	Default Value	Description
13:8	RW		**DEVCDV_CURSOR_B_FIFO_WATERMARK1:**
7:6	RO		**RESERVED3:** MBZ
5:0	RW		**DEVCDV_CURSORFIFO_SELF_REFRESH_WATERMARK 1:** Value should be as recommended in the high priority bandwidth analysis spreadsheet .

1.11.175 DISPLAY_CONTROLLER.FW6

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70078h
MMIO: Base/Offset: MMADR/70078h
IO: Base/Offset:

These control values only apply to high resolution non VGA modes of operation. The hardware depends on these registers being set properly since it is possible to set the watermarks to states causing starvation of the sync FIFO. These values control the second watermark level.

Bit	Access	Default Value	Description
31:9	RO		**RESERVED0:** MBZ
8:0	RW		**DEVCDV_DISPLAY_FIFO_SELF_REFRESH_WATERMAR K1:** Value should be as recommended in the high priority bandwidth analysis spreadsheet .

1.11.176 DISPLAY_CONTROLLER.GAMC0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721F4h
MMIO: Base/Offset: MMADR/721F4h
IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the display C pixel data pre blending. Additional gamma correction can be done in the display pipe gamma if desired. The pixels input to the gamma correction are 8 bit per channel pixels and the output of the gamma correction is 10 bit per channel pixels. The gamma curve is represented by specifying a set of points along the curve. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The 8 bit values in the register are extended to 10 bit values in hardware by concatenating two zeroes onto the LSBs. The two end points 0 and 1023 have fixed values 0 and 1023 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise screen artifacts may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to Y Blue to Cb also called U

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.177 DISPLAY_CONTROLLER.GAMC1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721F0h
MMIO: Base/Offset: MMADR/721F0h
IO: Base/Offset:

Same as previous register.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.178 DISPLAY_CONTROLLER.GAMC2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721ECh
MMIO: Base/Offset: MMADR/721ECh
IO: Base/Offset:

Same as previous register.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.179 DISPLAY_CONTROLLER.GAMC3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721E8h
MMIO: Base/Offset: MMADR/721E8h
IO: Base/Offset:

Same as previous register.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.180 DISPLAY_CONTROLLER.GAMC4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721E4h
MMIO: Base/Offset: MMADR/721E4h
IO: Base/Offset:

Same as previous register.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.181 DISPLAY_CONTROLLER.GAMC5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//721E0h
MMIO: Base/Offset: MMADR/721E0h
IO: Base/Offset:

Same as previous register.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.182 DISPLAY_CONTROLLER.GMBUS0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05100h
MMIO: Base/Offset: MMADR/05100h
IO: Base/Offset:

Description GMBUS clock and port select gmbus_register.v reg_gmbus0 The GMBUS0 register will set the clock rate of the serial bus and the device the controller is connected to. The clock rate options are 50KHz 100KHz 400KHz and 1MHz. This register should be set before the first data valid bit is set because it will be read only at the very first data valid bit and not read during the period of the transmission until stop is issued and next first data valid bit is set.

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15	RW		**HOLD_TIME_EXTENSION:** This bit selects the hold time on the data line driven from the GMCH. 0 Hold time of 0ns 1 Hold time of 300 ns
14:12	RO		**RESERVED1:**
11	RO		**DEVBW_DEVCL_RESERVED2:** DevBLC DevCTG DevIntel Atom Processor D2000 series and N2000 Series AKSV buffer select This bit selects whether the data to be written over GMBUS comes from the AKSV buffer for HDCP authentication or from the GMBUS data buffer. Please note that when writing data from the AKSV buffer all GMBUS protocol must be followed including indicating the number of bytes to be transferred during the DATA phase of a GMBUS cycle. 0 Default Use the GMBUS data buffer GMBUS3 for data transmission 1 Use the AKSV data buffer GMBUS6 and GMBUS7 for data transmission.
10:8	RW		**GMBUS_RATE_SELECT:** These two bits select the rate that the GMBUS will run at. It also defines the AC timing parameters used. It should only be changed when between transfers when the GMBUS is idle.

Bit	Access	Default Value	Description
7:3	RO		**RESERVED3:**
2:0	RW		**PIN_PAIR_SELECT:** This field selects an GMBUS pin pair for use in the GMBUS communication. Use the table above to determine which pin pairs are available for a particular device and the intended function of that pin pair. Note that it is not a straight forward mapping of port numbers to pair select numbers. 000 None disabled 001 Dedicated Control GMBUS Pins DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series LCTRCLKA LCTRLCLKB SSC Clock Device 010 Dedicated Analog Monitor DDC Pins DDC1DATA DDC1CLK 011 DevCL and DevCTG Integrated Digital Panel DDC Pins LVDS or DP D 100 DP HDMI port C Use DevCTG 101 sDVO HDMI Use 110 Reserved 111 D connector control signals

1.11.183 DISPLAY_CONTROLLER.GMBUS1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05104h
MMIO: Base/Offset: MMADR/05104h
IO: Base/Offset:

Description GMbus command and status gmbus_register.v reg_gmbus1 This register lets the software indicate to the GMBUS controller the slave device address register index and indicate when the data write is complete. When the SW_CLR_INT bit is asserted all writes to the GMBUS2 GMBUS3 and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally regardless of the state of the SW_CLR_INT bit.

Bit	Access	Default Value	Description
31	RO		**SOFTWARE_CLEAR_INTERRUPT_SW_CLR_INT:** This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller. This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK. 0 If this bit is written as a zero when its current state is a one will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers Write Protect Off . This bit is cleared to zero when an event causes the HW_RDY bit transition to occur. 1 Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared. Setting 1 this bit also asserts the HW_RDY bit until this bit is written with a 0 . When this bit is set no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
30	RW		**SOFTWARE_READY_SW_RDY:** Data handshake bit used in conjunction with HW_RDY bit. 0 De asserted via the assertion event for HW_RDY bit 1 When asserted by software results in de assertion of HW_RDY bit
29	RW		**ENABLE_TIMEOUT_ENT:** Enables timeout for slave

Bit	Access	Default Value	Description
			response. When this bit is enabled and the slave device response has exceeded the timeout period the GMBUS Slave Stall Timeout Error interrupt bit is set. 0 disable timeout counter 1 enable timeout counter
28	RO		**RESERVED0:**
27:25	RW		**BUS_CYCLE_SELECT:** 000 No GMBUS cycle is generated. 001 GMBUS cycle is generated without an INDEX with no STOP and ends with a WAIT 010 Reserved 011 GMBUS cycle is generated with an INDEX with no STOP and ends with a WAIT 100 Generates a STOP if currently in a WAIT or after the completion of the current byte if active. 101 GMBUS cycle is generated without an INDEX and with a STOP 110 Reserved 111 GMBUS cycle is generated with an INDEX and with a STOP GMBUS cycle will always consist of a START followed by Slave Address followed by an optional read or write data phase. A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase. The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle. This can only cause a STOP to be generated if a GMBUS cycle is generated the GMBUS is currently in a data phase or it is in a WAIT phase Note that the three bits can be decoded as follows 27 STOP generated 26 INDEX used 25 cycle ends in a WAIT
24:16	RW		**TOTAL_BYTE_COUNT:**
15:8	RW		**BIT_GMBUS_SLAVE_REGISTER_INDEX_INDEX:** This field specifies the 8 bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE READ pair. It only has an effect if the enable Index bit is set. Do not change this field during a GMBUS transaction.
7:1	RW		**BIT_GMBUS_SLAVE_ADDRESS_SADDR:** When a GMBUS cycle is to be generated using the Bus Cycle Select field this field specifies the value of the slave address that is to be sent out. For use with 10 bit slave address devices set this value to 11110XXb where the last two bits xx are the two MSBs of the 10 bit address and the slave direction bit to a write. This is followed by the first data byte being the 8 LSBs of the 10 bit slave address. Special Slave Addresses 0000 000R General Call Address 0000 000W Start byte 0000 001x CBUS Address 0000 010x Reserved 0000 011x Reserved 0000 1xxx Reserved 1111 1xxx Reserved 1111 0xxx 10 Bit addressing
0	RW		**SLAVE_DIRECTION_BIT:** When a GMBUS cycle is to be generated based on the Bus Cycle Select this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re start and a read. 1 Indicates that a Read from the slave device

Bit	Access	Default Value	Description
			operation is to be performed. 0 Indicates that a Write to slave device operation is to be performed.

1.11.184 DISPLAY_CONTROLLER.GMBUS2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05108h
MMIO: Base/Offset: MMADR/05108h
IO: Base/Offset:

Description GMbus status gmbus_register.v reg_gmbus2

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15	RW		**INUSE:** 0 read operation that contains a zero in this bit position indicates that the GMBUS engine is now acquired and the subsequent reads of this register will now have this bit set. Writing a 0 to this bit has no effect. 1 read operation that contains a one for this bit indicates that the GMBUS is currently allocated to someone else and In use . Once set a write of a 1 to this bit indicates that the software has relinquished the GMBUS resource and will reset the value of this bit to a 0. Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware and is only used as semaphore among various independent software threads that don t know how to synchronize their use of this resource that may need to use the GMBUS logic. Writing a one to this bit is software s indication that the software use of this resource is now terminated and it is available for other clients.
14	RO		**HARDWARE_WAIT_PHASE_HW_WAIT_PHASE:** 0 The GMBUS engine is not in a wait phase. 1 Set when GMBUS engine is in wait phase. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP. Once in a WAIT_PHASE the software can now choose to generate a STOP cycle or a repeated start RESTART cycle followed by another GMBUS transaction on the GMBUS.
13	RO		**SLAVE_STALL_TIMEOUT_ERROR:** 0 No slave timeout has occurred. 1 A slave acknowledge timeout has occurred
12	RO		**GMBUS_INTERRUPT_STATUS:** 0 The conditions that could cause a GMBUS interrupt have not occurred or this bit has been cleared by software assertion of the SW_CLR_INT bit. 1 GMBUS interrupt event occurred. This interrupt must have been one of the types enabled in the GMBUS4 register. DevIntel Atom Processor D2000 series and N2000 Series DevCTG Reserved
11	RO		**HARDWARE_READY_HW_RDY:** 0 Condition required for assertion has not occurred or when this bit was a one

Bit	Access	Default Value	Description
			and 0 SW_RDY bit has been asserted. 1 During a GMBUS read transaction after the each read of the data register. 2 During a GMBUS write transaction after each write of the data register. 3 SW_CLR_INT bit has been cleared. 1 This bit is asserted under the following conditions a After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit. b When an active GMBUS cycle has terminated with a STOP. c When during a GMBUS write transaction the data register needs and can accept another four bytes of data. d During a GMBUS read transaction this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data. This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.
10	RO		**NAK_INDICATOR:** 0 No bus error has been detected or SW_CLR_INT has been written as a zero since the last bus error. 1 Set by hardware if any expected device acknowledge is not received from the slave within the timeout.
9	RO		**GMBUS_ACTIVE_GA:** 0 The GMBUS controller is currently IDLE. 1 This indicates that the bus is in START ADDRESS INDEX DATA WAIT or STOP Phase. Set when GMBUS hardware is not IDLE.
8:0	RO		**CURRENT_BYTE_COUNT:**

1.11.185 DISPLAY_CONTROLLER.GMBUS3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//0510Ch
MMIO: Base/Offset: MMADR/0510Ch
IO: Base/Offset:

Description GMbus data buffer gmbus_register.v reg_gmbus3 This is data read write register. This register is double buffered. Bit 0 is the first bit sent or read bit 7 is the 8thbit sent or read all the way through bit 31 being the 32ndbit sent or read. For GMBUS write operations with a non zero byte count this register be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. For GMBUS read operations software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.

Bit	Access	Default Value	Description
31:24	RW		**DATA_BYTE_3:**
23:16	RW		**DATA_BYTE_2:**
15:8	RW		**DATA_BYTE_1:**
7:0	RW		**DATA_BYTE_0:**

1.11.186 DISPLAY_CONTROLLER.GMBUS4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05110h
MMIO: Base/Offset: MMADR/05110h
IO: Base/Offset:

Description GMbus interrupt mask gmbus_register.v reg_gmbus4

Bit	Access	Default Value	Description
31:5	RO		**RESERVED0:**
4:0	RW		**INTERRUPT_MASK:** This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in second level interrupt status register PIPEASTAT. Bit 4 GMBUS Slave stall timeout Bit 3 GMBUS NAK Bit 2 GMBUS Idle Bit 1 Hardware wait GMBUS cycle without a stop has completed Bit 0 Hardware ready Data has been transferred 0 Disable this type of GMBUS interrupt 1 Enable this type of GMBUS interrupt

1.11.187 DISPLAY_CONTROLLER.GMBUS5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05120h
MMIO: Base/Offset: MMADR/05120h
IO: Base/Offset:

Description GMBUS index gmbus_register.v reg_gmbus5 This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.

Bit	Access	Default Value	Description
31	RW		**BYTE_INDEX_ENABLE:** When this bit is asserted 1 then bits 15 00 are used as the index. Bits 15 8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1 lt 15 8 gt are ignored. Bits 7 0 are used in the second byte which is the least significant index bits.
30:16	RO		**RESERVED0:**
15:0	RW		**BYTE_SLAVE_INDEX:** This is the 2 byte index used in all GMBUS accesses when bit 31 is asserted 1 .

1.11.188 DISPLAY_CONTROLLER.GMBUS6

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05130h
MMIO: Base/Offset: MMADR/05130h
IO: Base/Offset:

Description GMbus data buffer gmbus_register.v reg_gmbus6 This is the AKSV write register written by system BIOS on boot. Bit 0 is the first bit sent bit 7 is the 8thbit sent through bit 31 being the 32ndbit sent.

Bit	Access	Default Value	Description
31:24	WO		**DATA_BYTE_3:**
23:16	WO		**DATA_BYTE_2:**
15:8	WO		**DATA_BYTE_1:**
7:0	WO		**DATA_BYTE_0:**

1.11.189 DISPLAY_CONTROLLER.GMBUS7

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05134h
MMIO: Base/Offset: MMADR/05134h
IO: Base/Offset:

Description GMbus data buffer gmbus_register.v reg_gmbus7 This is the AKSV write register written by system BIOS on boot. Bit 0 is the first bit sent through bit 7 being the 8th bit sent.

Bit	Access	Default Value	Description
31:9	RO		**RESERVED0:** MBZ
8	WO		**AKSV_SELECTION_BIT_DEVELK_DEVCDV:** 0 The register value of the AKSV is used. 1 The fuse value of the AKSV is used. DevBLC DevCTG Reserved
7:0	WO		**DATA_BYTE_5:**

1.11.190 DISPLAY_CONTROLLER.GPIOCTL_0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05010h
MMIO: Base/Offset: MMADR/05010h
IO: Base/Offset:

Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:**
12	RO		**GPIO_DATA_IN:** RO This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
11	RW		**GPIO_DATA_VALUE:** R W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
10	WO		**GPIO_DATA_MASK:** WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT write GPIO Data Value bit default . 1 Write GPIO Data Value bit.
9	RW		**GPIO_DATA_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 Pin is configured as an input default 1 Pin is configured as an output.
8	WO		**GPIO_DATA_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Data Direction Value bit default . 1 Write GPIO Data Direction Value bit.
7:5	RO		**RESERVED_MUST_BE_WRITTEN_WITH_ZEROS1:**
4	RO		**GPIO_CLOCK_DATA_IN:** RO This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
3	RW		**GPIO_CLOCK_DATA_VALUE:** R W This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
2	WO		**GPIO_CLOCK_DATA_MASK:** WO This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should

Bit	Access	Default Value	Description
			be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Clock Data Value bit default . 1 Write GPIO Clock Data Value bit.
1	RW		**GPIO_CLOCK_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 Pin is configured as an input and the output driver is set to tri state default 1 Pin is configured as an output.
0	WO		**GPIO_CLOCK_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT update the GPIO Clock Direction Value bit on a write default . 1 Update the GPIO Clock Direction Value bit. on a write operation to this register.

1.11.191 DISPLAY_CONTROLLER.GPIOCTL_1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05014h
MMIO: Base/Offset: MMADR/05014h
IO: Base/Offset:

Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:**
12	RO		**GPIO_DATA_IN:** RO This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
11	RW		**GPIO_DATA_VALUE:** R W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also

Bit	Access	Default Value	Description
			asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
10	WO		**GPIO_DATA_MASK:** WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT write GPIO Data Value bit default . 1 Write GPIO Data Value bit.
9	RW		**GPIO_DATA_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 Pin is configured as an input default 1 Pin is configured as an output.
8	WO		**GPIO_DATA_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Data Direction Value bit default . 1 Write GPIO Data Direction Value bit.
7:5	RO		**RESERVED_MUST_BE_WRITTEN_WITH_ZEROS1:**
4	RO		**GPIO_CLOCK_DATA_IN:** RO This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
3	RW		**GPIO_CLOCK_DATA_VALUE:** R W This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
2	WO		**GPIO_CLOCK_DATA_MASK:** WO This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Clock Data Value bit default . 1 Write GPIO Clock Data Value bit.
1	RW		**GPIO_CLOCK_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 Pin is configured as an

Bit	Access	Default Value	Description
			input and the output driver is set to tri state default 1 Pin is configured as an output.
0	WO		**GPIO_CLOCK_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT update the GPIO Clock Direction Value bit on a write default . 1 Update the GPIO Clock Direction Value bit. on a write operation to this register.

1.11.192 DISPLAY_CONTROLLER.GPIOCTL_2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//05018h
MMIO: Base/Offset: MMADR/05018h
IO: Base/Offset:

Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:**
12	RO		**GPIO_DATA_IN:** RO This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
11	RW		**GPIO_DATA_VALUE:** R W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
10	WO		**GPIO_DATA_MASK:** WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into

Bit	Access	Default Value	Description
			the register. This value is not stored and when read returns 0. 0 Do NOT write GPIO Data Value bit default . 1 Write GPIO Data Value bit.
9	RW		**GPIO_DATA_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 Pin is configured as an input default 1 Pin is configured as an output.
8	WO		**GPIO_DATA_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Data Direction Value bit default . 1 Write GPIO Data Direction Value bit.
7:5	RO		**RESERVED_MUST_BE_WRITTEN_WITH_ZEROS1:**
4	RO		**GPIO_CLOCK_DATA_IN:** RO This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
3	RW		**GPIO_CLOCK_DATA_VALUE:** R W This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
2	WO		**GPIO_CLOCK_DATA_MASK:** WO This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Clock Data Value bit default . 1 Write GPIO Clock Data Value bit.
1	RW		**GPIO_CLOCK_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 Pin is configured as an input and the output driver is set to tri state default 1 Pin is configured as an output.
0	WO		**GPIO_CLOCK_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT update the GPIO Clock Direction Value bit on a write default . 1 Update the GPIO Clock Direction Value bit. on a write

Bit	Access	Default Value	Description
			operation to this register.

1.11.193 DISPLAY_CONTROLLER.GPIOCTL_3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//0501Ch
MMIO: Base/Offset: MMADR/0501Ch
IO: Base/Offset:

Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:**
12	RO		**GPIO_DATA_IN:** RO This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
11	RW		**GPIO_DATA_VALUE:** R W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
10	WO		**GPIO_DATA_MASK:** WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT write GPIO Data Value bit default . 1 Write GPIO Data Value bit.
9	RW		**GPIO_DATA_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted.

Bit	Access	Default Value	Description
			The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 Pin is configured as an input default 1 Pin is configured as an output.
8	WO		**GPIO_DATA_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Data Direction Value bit default . 1 Write GPIO Data Direction Value bit.
7:5	RO		**RESERVED_MUST_BE_WRITTEN_WITH_ZEROS1:**
4	RO		**GPIO_CLOCK_DATA_IN:** RO This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
3	RW		**GPIO_CLOCK_DATA_VALUE:** R W This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
2	WO		**GPIO_CLOCK_DATA_MASK:** WO This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Clock Data Value bit default . 1 Write GPIO Clock Data Value bit.
1	RW		**GPIO_CLOCK_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 Pin is configured as an input and the output driver is set to tri state default 1 Pin is configured as an output.
0	WO		**GPIO_CLOCK_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT update the GPIO Clock Direction Value bit on a write default . 1 Update the GPIO Clock Direction Value bit. on a write operation to this register.

1.11.194 DISPLAY_CONTROLLER.GPIOCTL_4

PCI: B/D/F/Reg:

SBI: Port/Reg/Mem: 06h//05020h
MMIO: Base/Offset: MMADR/05020h
IO: Base/Offset:

Description GPIO I2C register gmbus_register.v reg_gpio0 reg_gpio1 reg_gpio2. reg_gpio3 reg_gpio4 These registers define the control of the sets of the so called general purpose I O pins. Each register controls a pair of pins that while can be used for general purpose control most are designated for specific functions according to the requirements of the device and the system that the device finds itself in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine for each product which pins registers are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. GMBUS port 5 is reserved for LT visual status indication and is controlled by hardware only. It is not accessible or programmable through its associated GPIO register which should be considered reserved. For devices with a PCI Express bus and in the case of the pins that are multiplexed with PCI Express signals the registers that control those pins should only be utilized if the Digital Port B detected bit in the SDVO HDMIB control register is set to 1.

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:**
12	RO		**GPIO_DATA_IN:** RO This is the value that is sampled on the GPIO_Data pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
11	RW		**GPIO_DATA_VALUE:** R W This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
10	WO		**GPIO_DATA_MASK:** WO This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT write GPIO Data Value bit default . 1 Write GPIO Data Value bit.
9	RW		**GPIO_DATA_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit. 0 Pin is configured as an input default 1 Pin is configured as an output.
8	WO		**GPIO_DATA_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO DIRECTION VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Data Direction Value bit default . 1 Write GPIO Data Direction Value bit.

Bit	Access	Default Value	Description
7:5	RO		**RESERVED_MUST_BE_WRITTEN_WITH_ZEROS1:**
4	RO		**GPIO_CLOCK_DATA_IN:** RO This is the value that is sampled on the GPIO Clock pin as an input. This input is synchronized to the Core Clock domain. Because the default setting is this buffer is an input this bit is undefined at reset.
3	RW		**GPIO_CLOCK_DATA_VALUE:** R W This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. Default 1. The GPIO default clock data value is programmed to 1 in hardware. The hardware drives a default of 1 since the I2C interface defaults to a 1 . this mimics the I2C external pull ups on the bus
2	WO		**GPIO_CLOCK_DATA_MASK:** WO This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. This value is not stored and when read always returns 0. 0 Do NOT write GPIO Clock Data Value bit default . 1 Write GPIO Clock Data Value bit.
1	RW		**GPIO_CLOCK_DIRECTION_VALUE:** R W This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. 0 Pin is configured as an input and the output driver is set to tri state default 1 Pin is configured as an output.
0	WO		**GPIO_CLOCK_DIRECTION_MASK:** WO This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. This value is not stored and when read returns 0. 0 Do NOT update the GPIO Clock Direction Value bit on a write default . 1 Update the GPIO Clock Direction Value bit. on a write operation to this register.

1.11.195 DISPLAY_CONTROLLER.HBLANK_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60004h
MMIO: Base/Offset: MMADR/60004h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Read Only.
28:16	RW		**PIPE_A_HORIZONTAL_BLANK_END:** This 13 bit field specifies the position of Horizontal Blank End expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK End pixel position where the first active pixel is considered position 0 the second active pixel is considered position 1 etc. Horizontal blank ending at the same point as the horizontal total indicates that there is no left hand border area. HBLANK size has a minimum value of 32 clocks.
15:13	RO		**RESERVED1:** Read Only.
12:0	RW		**PIPE_A_HORIZONTAL_BLANK_START:** This 13 bit field specifies the Horizontal Blank Start position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HBLANK Start pixel position where the first active pixel is considered position 0 the second active pixel is considered position 1 etc.

1.11.196 DISPLAY_CONTROLLER.HBLANK_BPIPE_B_HORIZONTAL_BLANK_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61004h
MMIO: Base/Offset: MMADR/61004h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:**
28:16	RW		**PIPE_B_HORIZONTAL_BLANK_END:** See pipe A description
15:13	RO		**RESERVED1:** Write as zero.
12:0	RW		**PIPE_B_HORIZONTAL_BLANK_START:** See pipe A description.

1.11.197 DISPLAY_CONTROLLER.HDCP_AKEY_HI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61424h
MMIO: Base/Offset: MMADR/61424h

IO: Base/Offset:

This register holds part of the Akey value.

Bit	Access	Default Value	Description
31:20	RO		**RESERVED0:**
19:0	RW		**AKEY_HIGH:** This is the most significant 20 bits of the 84 bit encrypted Akey value decryption mode or 84 bit Initialization Vector encryption mode . The Akey registers should be written in sequence from low to high. Writing to this register during key decryption mode triggers the cipher to process the register values. The value of this register must be zero during key encryption mode after the initialization vector has been processed. Write this register to zero after writing the IV. During key encryption mode the read value of this register contains the encrypted key value once the status register s key encrypt decrypt ready value is asserted. The read back is zero during key encryption data processing.

1.11.198 DISPLAY_CONTROLLER.HDCP_AKEY_LO

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6141Ch
MMIO: Base/Offset: MMADR/6141Ch
IO: Base/Offset:

This register holds part of the Akey value.

Bit	Access	Default Value	Description
31:0	RW		**AKEY_LOW:** This is the least significant 32 bits of the 84 bit encrypted Akey value 84 bit encryption initialization vector IV or 56 bit Akey value to encrypt. The Akey registers should be written in order from low to high. During key encryption mode the read value of this register contains the encrypted key value once the status register s key encrypt decrypt ready value is asserted. The read back is zero during key encryption data processing.

1.11.199 DISPLAY_CONTROLLER.HDCP_AKEY_MED

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61420h
MMIO: Base/Offset: MMADR/61420h
IO: Base/Offset:

This register holds part of the Akey value.

Bit	Access	Default Value	Description
31:0	RW		**AKEY_MIDDLE:** This is the middle 32 bits 63 32 of the 84 bit encrypted Akey value or 84 bit encryption Initialization Vector or the most significant 24 bits of the 56 bit plain text Akey value to encrypt. The Akey registers should be

Bit	Access	Default Value	Description
			written in order from low to high. Writing to this register during key encryption mode triggers the cipher to process the register values. During key encryption mode the read value of this register contains the encrypted key value once the status register s key encrypt decrypt ready value is asserted. The read back is zero during key encryption data processing.

1.11.200 DISPLAY_CONTROLLER.HDCP_AKSV_HI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61450h
MMIO: Base/Offset: MMADR/61450h
IO: Base/Offset:

This is a clear on read register.

Bit	Access	Default Value	Description
31:8	RO		**RESERVED0:**
7:0	RO		**HDCP_AKSV_HI:** hdcp_AKSV 39 32 HDCP A key selection vector as written in the Fuses after decryption.

1.11.201 DISPLAY_CONTROLLER.HDCP_AKSV_LO

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61454h
MMIO: Base/Offset: MMADR/61454h
IO: Base/Offset:

This is a clear on read register

Bit	Access	Default Value	Description
31:0	RO		**HDCP_AKSV_LOW:** hdcp_AKSV 31 0 HDCP A key selection vector as written in the Fuses after decryption.

1.11.202 DISPLAY_CONTROLLER.HDCP_AN_HI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61414h
MMIO: Base/Offset: MMADR/61414h
IO: Base/Offset:

This register holds part of the An value. Writeable with debug fuse enabled

Bit	Access	Default Value	Description
31:0	RO		**AN_HIGH:** This is the most significant 32 bits of the 64 bit An value

1.11.203 DISPLAY_CONTROLLER.HDCP_AN_LO

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61410h
MMIO: Base/Offset: MMADR/61410h
IO: Base/Offset:

This register holds part of the An value. Writeable with debug fuse enabled

Bit	Access	Default Value	Description
31:0	RO		**AN_LOW:** This is the least significant 32 bits of the 64 bit An value

1.11.204 DISPLAY_CONTROLLER.HDCP_BKSV_HI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6140Ch
MMIO: Base/Offset: MMADR/6140Ch
IO: Base/Offset:

This register holds part of the Bksv value.

Bit	Access	Default Value	Description
31:8	RO		**RESERVED0:**
7:0	WO		**BKSV_HIGH:** This is the most significant 8 bits of the 40 bit Bksv value

1.11.205 DISPLAY_CONTROLLER.HDCP_BKSV_LO

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61408h
MMIO: Base/Offset: MMADR/61408h
IO: Base/Offset:

This register holds part of the Bksv value.

Bit	Access	Default Value	Description
31:0	WO		**BKSV_LOW:** This is the least significant 32 bits of the 40 bit Bksv value

1.11.206 DISPLAY_CONTROLLER.HDCP_CONFIG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61400h
MMIO: Base/Offset: MMADR/61400h
IO: Base/Offset:

This register configures the HDCP mode.

Bit	Access	Default Value	Description
31:6	RO		**RESERVED0:**
5	RW		**AKEY_SOURCE_DEVELK:** 1 Akeys loaded from onboard fuses 0 Akeys loaded from registers DevCL DevBLC DevCTG Reserved
4:3	RO		**RESERVED1:**
2:0	RW		**HDCP_CONFIGURATION:** This field is used by software to control the flow of HDCP modes. 000 HDCP off 001 Capture An 010 Decrypt keys 011 Authenticate and encrypt includes summing keys over Bksv DevBLC and DevCTG 100 Reserved DevCL DevBLC DevCTG Program Fuses DevELK 101 Unique MCH ID 110 Encrypt Keys 111 Cipher Check Mode

1.11.207 DISPLAY_CONTROLLER.HDCP_DBG_STAT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6144Ch
MMIO: Base/Offset: MMADR/6144Ch
IO: Base/Offset:

This register reports HDCP status information for debugging. Debug fuse removes all access

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:24	RO		**SEQUENCE_STATUS:** State of cipher operation
23:16	RO		**CIPHER_STATE:** Internal cipher status and state
15:8	RO		**RESERVED1:**
7:0	RO		**ROUND_COUNT:**

1.11.208 DISPLAY_CONTROLLER.HDCP_INIT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61404h
MMIO: Base/Offset: MMADR/61404h
IO: Base/Offset:

This register is used to inject entropy into the An calculation. Hardware holds 64 bits of initialization vector. The hardware destination for writes to this register alternates between the high 32 bits and the low 32 bits. When generating An hardware will use the two most recent values written to this register as a 64 bit source of entropy.

Bit	Access	Default Value	Description
31:0	WO		**INITIALIZATION_VECTOR:** Software should write a random value to this field. It should be written at least twice.

1.11.209 DISPLAY_CONTROLLER.HDCP_REP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61444h
MMIO: Base/Offset: MMADR/61444h
IO: Base/Offset:

This register describes information needed for HDCP repeater support.

Bit	Access	Default Value	Description
31:20	RO		**RESERVED0:**
19:16	RO		**REPEATER_STATUS:** This field provides information about the current status of the repeater processing 0000 Idle 0001 Busy 0010 Ready for next data 0100 Complete no match 1100 Complete match All others Reserved
15:4	RO		**RESERVED1:**
3:1	RW		**REPEATER_CONTROL:** This field is used to control the processing of the repeater information When selecting 100 101 or 110 the desired text must be aligned to the least significant byte of the HDCP SHA 1 In register. Hardware will automatically append the 0x80 after the Mo if the Mo is not 32 bit aligned.
0	RW		**REPEATER_PRESENT:** This bit indicates that the receiver is a repeater.

1.11.210 DISPLAY_CONTROLLER.HDCP_RI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61418h
MMIO: Base/Offset: MMADR/61418h
IO: Base/Offset:

This register holds the receiver s Ri value.

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15:0	RW		**RI:** This is the receiver s Ri value. Write with all 0s when turning off HDCP.

1.11.211 DISPLAY_CONTROLLER.HDCP_SHA1_IN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61440h
MMIO: Base/Offset: MMADR/61440h
IO: Base/Offset:

This register provides the input for the SHA1 hash.

Bit	Access	Default Value	Description
31:0	RW		**SHA_1_DATA_STREAM:** This is the data stream input to the SHA 1 hash. The hardware performs the hash on this

			value. Input data in big endian format.

1.11.212 DISPLAY_CONTROLLER.HDCP_STATUS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61448h
MMIO: Base/Offset: MMADR/61448h
IO: Base/Offset:

This register describes the HDCP status.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27	RO		**HDCP_FUSE_LOCK_DISABLE:** 0 HDCP memory RF dft interface is disabled by fuse. 1 HDCP memory RF dft interface is enabled by fuse.
26	RO		**HDCP_FUSE_DISABLE:** 0 HDCP is enabled by fuse. 1 HDCP is disabled by fuse.
25	RO		**HDCP_DTEP_FUSE_PROGRAMMING_SUCCESS_DEVELK:** 0 Fuse programming not successful. 1 The fuse programming was successful with MAC value matching. This bit must be checked after Bit 24 has been set to check if the fuse transfer was successful. Writing a 1 to this bit clears it. DevCL DevBLC DevCTG Reserved
24	RO		**HDCP_DTEP_FUSE_PROGRAMMING_COMPLETE_DEVELK:** 0 Fuse transfer not complete 1 Fuse transfer has completed. Writing a 1 to this bit clears it. DevCL DevBLC DevCTG Reserved
23	RO		**CIPHER_STATUS_MAC_STATUS:** 0 Key load not verified 1 Key decryption mode data load test OK
22	RO		**CIPHER_STATUS_MCH_ID_READY:** 0 UMCH ID not ready 1 UMCH ID ready
21	RO		**CIPHER_STATUS_KEY_ENCRYPTION_DECRYPTION_READY:** 0 Cipher not ready 1 Cipher ready for next Akey
20	RO		**CIPHER_STATUS_ENCRYPTING_STATUS:** 0 Hardware is not currently encrypting 1 Hardware is encrypting
19	RO		**CIPHER_STATUS_RI_MATCHES:** 0 Ri does not match 1 Ri matches
18	RO		**CIPHER_STATUS_RI_READY:** This field indicates whether Ri is ready for Ro during initial authorization 0 Ri not ready 1 Ri ready
17	RO		**CIPHER_STATUS_AN:** 0 An not ready 1 An ready
16	RO		**CIPHER_STATUS:** HDCP status 0 HDCP off 1 HDCP on
15:8	RO		**FRAME_COUNT:** Internal frame counter for cipher R update
7:0	RO		**AINFO:** This field provides the Ainfo value. If HDCP 1.1 features are not enabled this value will be 0.

1.11.213 DISPLAY_CONTROLLER.HDCP_V_0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6142Ch
MMIO: Base/Offset: MMADR/6142Ch
IO: Base/Offset:

These registers hold the V hash result from the receiver used for repeaters.

Bit	Access	Default Value	Description
31:0	RW		**V_HASH_RESULT:** This holds part of the hash result from the receiver used for repeaters.

1.11.214 DISPLAY_CONTROLLER.HDCP_V_1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61430h
MMIO: Base/Offset: MMADR/61430h
IO: Base/Offset:

These registers hold the V hash result from the receiver used for repeaters.

Bit	Access	Default Value	Description
31:0	RW		**V_HASH_RESULT:** This holds part of the hash result from the receiver used for repeaters.

1.11.215 DISPLAY_CONTROLLER.HDCP_V_2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61434h
MMIO: Base/Offset: MMADR/61434h
IO: Base/Offset:

These registers hold the V hash result from the receiver used for repeaters.

Bit	Access	Default Value	Description
31:0	RW		**V_HASH_RESULT:** This holds part of the hash result from the receiver used for repeaters.

1.11.216 DISPLAY_CONTROLLER.HDCP_V_3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61438h
MMIO: Base/Offset: MMADR/61438h
IO: Base/Offset:

These registers hold the V hash result from the receiver used for repeaters.

Bit	Access	Default Value	Description
31:0	RW		**V_HASH_RESULT:** This holds part of the hash result from the receiver used for repeaters.

1.11.217 DISPLAY_CONTROLLER.HDCP_V_4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6143Ch
MMIO: Base/Offset: MMADR/6143Ch
IO: Base/Offset:

These registers hold the V hash result from the receiver used for repeaters.

Bit	Access	Default Value	Description
31:0	RW		**V_HASH_RESULT:** This holds part of the hash result from the receiver used for repeaters.

1.11.218 DISPLAY_CONTROLLER.HISTOGRAM_THRESHOLD_GUARDBAND_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61268h
MMIO: Base/Offset: MMADR/61268h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**HISTOGRAM_INTERRUPT_ENABLE:** 0 Disabled 1 Enabled. This generates a histogram interrupt once a Histogram event occurs.
30	RO		**HISTOGRAM_EVENT_STATUS:** When a Histogram event has occurred this will get set by the hardware. For any more Histogram events to occur the software needs to clear this bit by writing a 1 . The default state for this bit is 0 . 0 Histogram event has not occurred. 1 Histogram event has occurred.
29:22	RW		**GUARDBAND_INTERRUPT_DELAY:** An interrupt is generated after this many consecutive frames of the guardband threshold being surpassed. This value is double buffered on start of vblank. A value of 0 is invalid.

Bit	Access	Default Value	Description
21:0	RW		**THRESHOLD_GUARDBAND:** This value is used to determine the guardband for the threshold interrupt generation. This single value is used for all the segments. This value is double buffered on start of vblank

1.11.219 DISPLAY_CONTROLLER.HORZ_PH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30124h
MMIO: Base/Offset: MMADR/30124h
IO: Base/Offset:

This register value is mirrored from DDR in address 24h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:20	RO		**UV_HORIZONTAL_PHASE:** Sets the initial horizontal phase for the U and V data. Only used in YUV modes.
19:16	RO		**RESERVED0:** MBZ
15:4	RO		**Y_RGB_HORIZONTAL_PHASE:** Sets the initial horizontal phase for both buffers fields. Unlike the vertical initial phases this does not change buffer to buffer or field to field. YUV modes use a separate initial phase for Y and UV data. This value will either be the actual initial phase or the initial phase minus one.
3:0	RO		**RESERVED1:** MBZ

1.11.220 DISPLAY_CONTROLLER.HSYNC_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60008h
MMIO: Base/Offset: MMADR/60008h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_A_HORIZONTAL_SYNC_END:** This 13 bit field specifies the horizontal Sync End position expressed in terms of the absolute pixel number relative to the horizontal active display start. The value programmed should be the HSYNC End pixel position where the first active pixel is considered position 0 the second active pixel is considered position 1 etc.
15:13	RO		**RESERVED1:** Read Only.
12:0	RW		**PIPE_A_HORIZONTAL_SYNC_START:** This 13 bit field specifies the horizontal Sync Start position expressed in terms of the absolute pixel number relative to the

Bit	Access	Default Value	Description
			horizontal active display start. The value programmed should be the HSYNC Start pixel position where the first active pixel is considered position 0 the second active pixel is considered position 1 etc. Note that when HSYNC Start is programmed equal to HBLANK Start both HSYNC and HBLANK will be asserted on the same pixel clock. It should never be programmed to less than HBLANK start.

1.11.221 DISPLAY_CONTROLLER.HSYNC_BPIPE _B_HORIZONTAL_SYNC_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61008h
MMIO: Base/Offset: MMADR/61008h

IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_B_HORIZONTAL_SYNC_END:** See pipe A description.
15:13	RO		**RESERVED1:** Write as zero.
12:0	RW		**PIPE_B_HORIZONTAL_SYNC_START:** See pipe A description

1.11.222 DISPLAY_CONTROLLER.HTOTAL_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60000h
MMIO: Base/Offset: MMADR/60000h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_A_HORIZONTAL_TOTAL_DISPLAY_CLOCKS:** This 13 bit field provides Horizontal Total up to 8192 pixels encompassing the Horizontal Active Display period front back border and retrace period. Any pending event HSYNC ACTIVE HBLANK is reset at HTOTAL and the programmed sequence begins again. This field is programmed to the number of clocks desired minus one.
15:12	RO		**RESERVED1:** Write as zero.
11:0	RW		**PIPE_A_HORIZONTAL_ACTIVE_DISPLAY_END_PIXELS:** This 12 bit field provides Horizontal Active Display resolutions up to 4096 pixels. Note that the first horizontal active display pixel is considered pixel number 0. The value programmed

Bit	Access	Default Value	Description
			should be the active pixels line 1 .

1.11.223 DISPLAY_CONTROLLER.HTOTAL_BPIPE _B_HORIZONTAL_TOTAL_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61000h
MMIO: Base/Offset: MMADR/61000h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_B_HORIZONTAL_TOTAL_DISPLAY:** See pipe A description.
15:12	RO		**RESERVED1:** Write as zero.
11:0	RW		**PIPE_B_HORIZONTAL_ACTIVE_DISPLAY:** See pipe A description

1.11.224 DISPLAY_CONTROLLER.IMAGE_ENHANCEMENT _BIN_DATA_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61264h
MMIO: Base/Offset: MMADR/61264h
IO: Base/Offset:

Writes to this address are steered to the correct register by programming the Bin Register Function Select and the Bin Register Index. Function 0 usage Threshold Count this Function is Read Only

Bit	Access	Default Value	Description
31	RW		**BUSY_BIT:** If set the engine is busy the rest of the register is undefined. If clear the register contains valid data.
30:22	RO		**RESERVED0:**
21:0	RW		**BIN_COUNT:** The total number of pixels in this bin value is updated at the start of each vblank.

1.11.225 DISPLAY_CONTROLLER.INIT_PHS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30128h
MMIO: Base/Offset: MMADR/30128h
IO: Base/Offset:

This register value is mirrored from DDR in address 28h R W . This register provides a method to create a negative initial phase or one with a positive integer offset. If the corresponding bits are set to all ones the initial phase is the fractional phase register value minus one. These bits should only be set in cases where the buffer pointer is pointing to the first pixel of the line or column because it will effectively cause the first pixel to be duplicated. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:20	RO		**Y0_VPP_INITIAL_PHASE_FOR_VERTICAL_PANNING:** 0000 0 Positive fractional phase 0001 fractional phase plus one 0010 fractional phase plus two 0011 1110 Reserved 1111 fractional phase minus one 1
19:16	RO		**Y1_VPP_INITIAL_PHASE_FOR_VERTICAL_PANNING:**
15:12	RO		**Y_HPP_INITIAL_PHASE_FOR_HORIZONTAL_PANNING:**
11:8	RO		**UV0_VPP_INITIAL_PHASE_FOR_VERTICAL_PANNING:**
7:4	RO		**UV1_VPP_INITIAL_PHASE_FOR_VERTICAL_PANNING:**
3:0	RO		**UV_HPP_INITIAL_PHASE_FOR_HORIZONTAL_PANNING:**

1.11.226 DISPLAY_CONTROLLER.LVDS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61180h
MMIO: Base/Offset: MMADR/61180h
IO: Base/Offset:

Description Video control dplreg.v lvds_port_cntl Write Protect by Panel Power Sequencer on

Bit	Access	Default Value	Description
31	RW		**LVDS_PORT_ENABLE:** When disabled the LVDS port is inactive and in it s low power state. Enabling the LVDS port changes the way that the PLL for this pipe is programmed. This bit must be set before the display PLL is enabled and the port is power sequenced on using the panel power sequencing logic. 0 The port is disabled and all LVDS pairs are powered down. 1 The port is enabled port must be enabled before powering up a connected panel
30	RW		**LVDS_PORT_PIPE_ASSIGN:** 0 The port gets data from pipe A 1 The port gets data from pipe B default
29:26	RO		**RESERVED0:**
25	RW		**DITHER_ENABLE:** This bit enables or disables bypassing 8 6 bit color dithering function. The usage of this bit would be on for 18 bpp panels and off for 24 bpp panels. 0 disabled 1 enabled
24	RW		**DATA_FORMAT_SELECT:** Combined with the other control bits it selects the LVDS data format. Other control

Bit	Access	Default Value	Description
			bits in this register determine if two channel is enabled and 18 or 24 bit color is enabled. 0 1x18.0 2x18.0 1x24.0 or 2x24.0 1 1x24.1 or 2x24.1
23	RO		**LE_CONTROL_ENABLE:** This bit is used when the second channel control signal field indicates that we are using the LE instead of HS and the two channel mode is enabled. In single channel mode this bit has no effect. DevCTG 0 Send 0 on second channel HS B2 lt 2 gt 1 Send 1 on second channel HS DevIntel Atom Processor D2000 series and N2000 Series Reserved
22	RO		**LF_CONTROL_ENABLE:** This bit is used when the second channel control signal field indicates that we are using the LF instead of VS and two channel mode is enabled. In single channel mode this bit has no effect. DevCTG 0 Send 0 on second channel VS B2 lt 3 gt 1 Send 1 on second channel VS DevIntel Atom Processor D2000 series and N2000 Series Reserved
21	RW		**VSYNC_POLARITY:** This controls the polarity of the VSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity. 0 No inversion 1 active 1 Invert the sense 0 active
20	RW		**HSYNC_POLARITY_LP_INVERT:** This controls the polarity of the HSYNC indicator that is sent over the LVDS connection. Panels may require one or the other polarity or work with either polarity. 0 No inversion 1 active 1 Invert the sense 0 active
19	RW		**DE_INVERT:** This controls the polarity of the DE indicator that is sent over the LVDS connection. 0 No inversion of DE 1 active 1 Invert the sense of DE 0 active
18:17	RO		**SECOND_CHANNEL_CONTROL_SIGNALS:** This bit only applies to the two channel modes of operation it has no effect in single channel modes. DevCTG 00 Send DE HS VS on second channel if enabled 01 Reserved 10 Do not send DE HS VS on second channel use zero instead 11 Use DE 0 HS LE VS LF on second channel DevIntel Atom Processor D2000 series and N2000 Series Reserved
16	RO		**CHANNEL_RESERVED_BITS_DEVCTG_DEVCDV1:** 0 Send 0 for the channel reserved bits 1 Send duplicate data bit for reserved bits
15	RW		**LVDS_BORDER_ENABLE:** This selects whether the border data should be included in the active display data sent to the panel. Border should be used when in VGA centered un scaled mode or when scaling a 4 3 source image to a wide screen panel typical 16 9 . 0 Border to the LVDS transmitter is disabled. DE Display Enable is used. 1 Border to the LVDS transmitter is enabled. Blank is used as DE for the panel.
14:11	RO		**RESERVED2:**
10	RW		**BUFFER_POWER_DOWN_STATE:** This bit selects the state of the LVDS buffers during a powered down state

Bit	Access	Default Value	Description
			caused by the power sequence logic power down. This selection will be made based on the connected panel requirements. 0 Zero Volts Driven on both lines of the pairs 1 Tri State High impedance state
9:8	RW		**CLKA_A0_A1_A2_CONTROL:** This field controls the A0 A2 data pairs and CLKA. It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state. 00 Power Down all A channel signals including A3 0V 01 Power up A0 A1 A2 Data bits forced to 0 Timing active Clock Active 10 Reserved 11 Power up Data lines and clock active
7:6	RW		**EIGHT_BIT_COLOR_CHANNEL_A3_CONTROL:** This field can control both the A3 and B3 data pairs. Enabling those pairs indicates the selection of 8 bit per color channel mode. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The A3 pair will only be powered up if both this field and the A0 A1 A2 CLKA field indicates that the pair should be powered up and will only be active if both indicate that it should be active. The B3 pair will only be powered up if both this field and the B0 B1 B2 B3 field indicates that the pair should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control. When the power sequencer is in the power down mode all signals are in the power down state. 00 Power Down all signals A3 B3 common mode 01 Power up A3 B3 Data pixel data not control lines forced to 0 output 10 Reserved 11 Power up A3 B3 Data lines active
5:4	RO		**TWO_CHANNEL_MODE_CLKB_CONTROL:** When in two channel mode this field controls the CLKB pair. It sets the highest level of activity that is allowed on these lines when the panel is powered on. The CLKB pair should only be powered up if the B0 B1 B2 B3 field indicates that the second channel should be powered up and will only be active if both indicate that it should be active. Power sequencing for LVDS connected panels overrides the control. DevCTG 00 Power Down CLKB common mode 01 Power up CLKB Forced to 0 10 Reserved 11 Power up Clock B active DevIntel Atom Processor D2000 series and N2000 Series Reserved
3:2	RO		**TWO_CHANNEL_MODE_B0_B1_B2_CONTROL:** This field controls both the set B0 B2 data pairs. It sets the highest level of activity that is allowed on these lines when the panel is powered on. Power sequencing for LVDS connected panels overrides the control. During single channel operation 1x18.0 these bits need to be both zero. Two channel operation is selected by setting them to ones. Note that the second clock can be optionally enabled or disabled by the two channel mode ClkB control field. DevCTG 00 Power Down all signals including B3 and CLKB 01 Power up B0 B1 B2 Data lines forced to 0 timing is active 10 Reserved 11 Power up Data lines active color and timing DevIntel Atom Processor D2000 series and N2000

Bit	Access	Default Value	Description
			Series Reserved
1:0	RO		**RESERVED3:**

1.11.227 DISPLAY_CONTROLLER.LVDSCKT1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61184h
MMIO: Base/Offset: MMADR/61184h
IO: Base/Offset:

Description PHY LVDSIO TX Control dplrreg.v dsp_lvd_tx_cnt This register contains the control bit to get optimal performance out of LVDS Transmitter circuit

Bit	Access	Default Value	Description
31:30	RW		**ST1_TIME_DEVCDV:** Programmable bits to control TX stage1 flop timing
29:28	RW		**ST2_TIME_DEVCDV:** Programmable bits to control TX stage2 flop timing
27:26	RW		**ST3_TIME_DEVCDV:** Programmable bits to control TX stage3 flop timing
25:16	RW		**RES_DEVCDV:** Reserved for future use
15:10	RW		**RES_TX0_DEVCDV:** Reserved for future use in tx
9:6	RW		**SLEW_RATE_DEVCDV:** Slew rate control bits for driver
5:2	RW		**RES_TX1_DEVCDV:** Reserved for future use in tx
1:0	RW		**TX_SWING_DEVCDV:** Changes LVDS transmitter output swing by changing Iload Iref multiplier mirror ratio

1.11.228 DISPLAY_CONTROLLER.LVDSCKT2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61188h
MMIO: Base/Offset: MMADR/61188h
IO: Base/Offset:

Description PHY LVDSIO Analog Control dplrreg.v dsp_lvd_ana_cnt This register contains circuit control bits to optimize analog reference circuit performance of lvdsphy

Bit	Access	Default Value	Description
31	RW		**BG_DIS_DEVCDV:** Disable bandgap chopper clock chopper is enabled by default
30	RW		**BG_SEL_DEVCDV:** Select external clock for bandgap chopper default is internal clock
29:16	RW		**RES_ANA0_DEVCDV:** Reserved for future use

Bit	Access	Default Value	Description
15	RW		**RES_ANA1_DEVCDV:** Reserved for future use
14:13	RW		**VOL_SEL_DEVCDV:** For selecting constant voltage from resistor divider
12:5	RW		**BIAS_DEVCDV:** Driver keeper bias programmability
4:0	RW		**CONTROLS_ANALOG_VOLTAGE_AND_CURRENT_REFERENCES_TO_CHANNEL_A_AMP_B_DEVCDV:** 1 0 Reference voltage selection from BG or Resistor divider or external reference

1.11.229 DISPLAY_CONTROLLER.LVDSCKT3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6118ch
MMIO: Base/Offset: MMADR/6118ch
IO: Base/Offset:

Description PHY LVDSIO LoopBack Control dplrreg.v dsp_lvd_lb_cnt This register contains circuit control bits to optimize analog reference circuit performance of lvdsphy

Bit	Access	Default Value	Description
31:30	RW		**LB_TIM1_DEVCDV:** Controls loop back external timing data going to core in loop back circuit flop stage1
29:28	RW		**LB_TIM2_DEVCDV:** Controls loop back internal timing in loop back circuit flop stage 2
27:24	RW		**RES_0_DEVCDV:** Reserved for future use
23:18	RW		**RES_LB0_DEVCDV:** Reserved for future use in lbc
17:16	RW		**LB_TIM_GLOBAL0_DEVCDV:** Controls internal timing in loop back circuit
15:10	RW		**RES_1_DEVCDV:** Reserved for future use
9:4	RW		**RES_LB1_DEVCDV:** Reserved for future use in lbc
3:0	RW		**LB_TIM_GLOBAL1_DEVCDV:** Controls internal timing in loop back circuit

1.11.230 DISPLAY_CONTROLLER.LVDSCKT4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61190h
MMIO: Base/Offset: MMADR/61190h
IO: Base/Offset:

Description PHY LVDSIO Future used dplrreg.v lvd_dsp_phy_spare

Bit	Access	Default Value	Description
31:18	RW		**RES_0_DEVCDV:** Reserved for future use

17:16	RW		**BON_ANA_DEVCDV:** Bonus writable register bits for LVDSPHY Analog circuit
15:10	RW		**RES_1_DEVCDV:** Reserved for future use
9:0	RW		**BON_TX_DEVCDV:** Bonus writable register bits for LVDSPHY TX

1.11.231 DISPLAY_CONTROLLER.LVDSTCR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61194h
MMIO: Base/Offset: MMADR/61194h
IO: Base/Offset:

Description PHY LVDSIO Future used dplrreg.v lvd_dsp_phy_spare

Bit	Access	Default Value	Description
31	RW		**LVDS_DFT_ENABLE:** Gates all other bits in LVDS test control register except for bit 30
30	RW		**LVDS_TRANSMITTER_ENABLE:** Used to enable LVDS transmitters which require 2ms warm up time before data can be accurately transmitted.
29:15	RW		**RES_0:** Reserved for future use
14:11	RW		**BIT_ERROR_TEST_PAIR_SELECT:**
10:8	RW		**LVDS_TEST_MODE_SELECT:**
7	RW		**LVDS_TRANSMITTER_AND_RECEIVER_BYPASSING_FOR_DFT:**
6	RW		**BER_PULSE_STRETCHING_OPTION:**
5	RW		**LVDS_RECEIVER_DISABLE:** Used to disable LVDS receiver loopback
4:0	RW		**RES_1:** Reserved for future use

1.11.232 DISPLAY_CONTROLLER.OBUF_0U

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30108h 3010B
MMIO: Base/Offset: MMADR/30108h 3010B
IO: Base/Offset:

This register value is mirrored from DDR in address 08h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_BUFFER_0_U_LINEAR_OFFSET:** This is the offset for the U planar data. This value is added to the

			surface address to get the graphics address of the first pixel to be displayed. This offset is the difference between the address of the upper left pixel to be displayed and the overlay surface address. When mirroring horizontally X backward this field points to first byte of the last pixel of the line.

1.11.233 DISPLAY_CONTROLLER.OBUF_0V

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3010Ch
MMIO: Base/Offset: MMADR/3010Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 0Ch R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_BUFFER_0_V_LINEAR_OFFSET:** This is the offset for the V planar data. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset is the difference between the address of the upper left pixel to be displayed and the overlay surface address. When mirroring horizontally X backward this field points to first byte of the last pixel of the line.

1.11.234 DISPLAY_CONTROLLER.OBUF_0Y

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30100h
MMIO: Base/Offset: MMADR/30100h
IO: Base/Offset:

This register value is mirrored from DDR in address 00h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_BUFFER_0_Y_LINEAR_OFFSET:** This is the offset for the Y planar or YUV packed color data. This value is added to the surface address to get the graphics address of the first pixel to be displayed. It must be pixel aligned e.g. low order bit is zero for 16 bpp packed formats . This offset is the difference between the address of the upper left pixel to be displayed and the overlay surface address. When mirroring horizontally X backward this field points to

Bit	Access	Default Value	Description
			first byte of the last pixel of the line.

1.11.235 DISPLAY_CONTROLLER.OBUF_1U

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30110h 30113
MMIO: Base/Offset: MMADR/30110h 30113
IO: Base/Offset:

This register value is mirrored from DDR in address 10h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_BUFFER_1_U_LINEAR_OFFSET:** This is the offset for the U planar data. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset is the difference between the address of the upper left pixel to be displayed and the overlay surface address. When mirroring horizontally X backward this field points to first byte of the last pixel of the line.

1.11.236 DISPLAY_CONTROLLER.OBUF_1V

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30114h
MMIO: Base/Offset: MMADR/30114h
IO: Base/Offset:

This register value is mirrored from DDR in address 14h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_BUFFER_1_V_LINEAR_OFFSET:** This is the offset for the V planar data. This value is added to the surface address to get the graphics address of the first pixel to be displayed. This offset is the difference between the address of the upper left pixel to be displayed and the overlay surface address. When mirroring horizontally X backward this field points to first byte of the last pixel of the line.

1.11.237 DISPLAY_CONTROLLER.OBUF_1Y

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30104h 30107
MMIO: Base/Offset: MMADR/30104h 30107
IO: Base/Offset:

This register value is mirrored from DDR in address 04h R W . This value specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory this field contains the byte offset of the plane data in graphics memory. When the surface is tiled the value in this register is ignored. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_BUFFER_1_Y_LINEAR_OFFSET:** This is the offset for the Y planar or YUV packed color data. This value is added to the surface address to get the graphics address of the first pixel to be displayed. It must be pixel aligned e.g. low order bit is zero for 16 bpp packed formats . This offset is the difference between the address of the upper left pixel to be displayed and the overlay surface address. When mirroring horizontally X backward this field points to first byte of the last pixel of the line.

1.11.238 DISPLAY_CONTROLLER.OCLRC0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30148h
MMIO: Base/Offset: MMADR/30148h
IO: Base/Offset:

This register value is mirrored from DDR in address 48h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:** MBZ
26:18	RO		**CONTRAST:** Contrast adjustment applies to YUV data. The Y channel is multiplied by the value contained in the register field. This signed fixed point number is in 3i.6f format with the first 3 MSBs as the integer value and the last 6 LSBs as the fraction value. The allowed contrast value ranges from 0 to 7.53125 decimal. Bypassing Contrast for YUV modes and for source data in RGB format is accomplished by programming this field to a field value that represents 1.0 decimal or 001.000000 binary.
17:8	RO		**RESERVED1:** MBZ
7:0	RO		**BRIGHTNESS:** This field provides the brightness adjustment with a 8 bit 2 s compliment value ranging 128 127 . This value is added to the Y value after contrast multiply and before YUV to RGB conversion. A value of zero disables this adjustment affect. This 8 bit signed value provides half of the achievable brightness adjustment dynamic range. A full range brightness value would have a programmable range of 255 255 . Bypassing Brightness for

Bit	Access	Default Value	Description
			YUV formats and for source data in RGB format is accomplished by programming this field to 0.

1.11.239 DISPLAY_CONTROLLER.OCLRC1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3014Ch
MMIO: Base/Offset: MMADR/3014Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 4Ch R W . The sum of the absolute value of SH_SIN and SH_COS must be limited to less than 8. ABS SH_SIN ABS SH_COS lt 8The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:** MBZ
26:16	RO		**SATURATION_AND_HUE_SIN:** This field can be used in two modes Similar to the contrast field there is no limit for saturation reduction saturation 0 means all pixels become the same value. However increasing contrast can only be increased by a factor less than 8. For example the largest contrast with value of 0x7.7F can bring input range 0 32 to a full display color range of 0 255 . Bypassing Hue even for source data in RGB format is accomplished by programming this field to 0.0. Format This 11 bit signed fixed point number is in 2 s compliment s3i.7f format with the MSB as the sign next 3 MSBs as the integer value and the last 7 LSBs as the fraction value
15:10	RO		**RESERVED1:** MBZ
9:0	RO		**SATURATION_AND_HUE_COS:** This field can be used in two modes Similar to the contrast field there is no limit for saturation reduction saturation 0 means all pixels become the same value. However increasing contrast can only be increased by a factor less than 8. For example the largest contrast with value of 0x7.7F can bring input range 0 32 to a full display color range of 0 255 . Bypassing Saturation even for source data in RGB format is accomplished by programming this field to 1.0. Format This unsigned fixed point number is in 3i.7f format with the first 3 MSBs be the integer value and the last 7 LSBs be the fraction value.

1.11.240 DISPLAY_CONTROLLER.OCOMD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30168h
MMIO: Base/Offset: MMADR/30168h
IO: Base/Offset:

This register value is mirrored from DDR in address 68h R W . This register and the Overlay Configuration register provide the basic programming options that the overlay engine needs to begin its work. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:20	RO		**RESERVED0:** MBZ
19	RO		**TILED_SURFACE:** This bit indicates that the overlay surface data is in tiled memory. The tile pitch is specified in bytes in the OSTRIDE register. Only X tiling is supported for overlay surfaces. When this bit is set it affects the hardware interpretation of the OBUF and OSTART registers. 0 Overlay surfaces use linear memory 1 Overlay surfaces use X tiled memory
18:17	RO		**MIRRORING:** Mirroring cause either a horizontal or vertical reversal in the displayed image. Note that when both horizontal and vertical mirroring is enabled it is a 180 degree rotation. Mirroring affects the buffer address values used. See buffer address description for details. 00 Normal orientation 01 Horizontal Mirroring 10 Vertical Mirroring 11 Both Horizontal and Vertical Mirroring 180 degree rotate
16	RO		**RESERVED1:** MBZ
15:14	RO		**PACKED_YUV_4:** 2 2 Byte Order ORDER422 Affects the byte order for Packed YUV 4 2 2 data. This allows for the support of multiple YUV 4 2 2 formats. It must be set to zero for other data formats. 00 Normal in YUYV order with FOURCC code YUY2 01 UV Swap in YVYU order 10 Y Swap in UYVY order with FOURCC code UYVY 11 Y and UV swap in VYUY order
13:10	RO		**FORMAT:** Source Format. 0XXX Reserved 0111 NV12 1000 Packed YUV 4 2 2 Field ORDER422 in this register determines the byte order of this format 1001 Reserved 1011 NV12 1100 Planar YUV 4 2 0 MPEG 1 or 2 based on UV initial phase 1101 Planar YUV 4 2 2 e.g. for DCT domain downsampled MPEG2 video 1110 Planar YUV 4 1 0 or YUV 4 1 1 planar 1111 Reserved In all YUV formats UV source values are in excess 128 format in which value 128 stands for intensity of 0 for the color components.
9	RO		**RESERVED2:** was TV Field Synchronized Flip Field Parity Setting TVSYNCFLIP_PARITY
8	RO		**RESERVED3:** MBZ Enabling AUTOFLIP
7	RO		**FIELD_SYNCHRONIZED_FLIP_ENABLE:** This bit enables the overlay flip that is synchronized with the display field. 0 Normal Overlay Flip standard . The TVSYNCFLIP_PARITY bit is ignored. 1 Field Synchronized Overlay Flip

Bit	Access	Default Value	Description
6	RO		**RESERVED4:** MBZ
5	RO		**BUFFER_DISPLAY_FLIP_TYPE:** This bit affects the buffer addressing used for buffer display and the use of the initial vertical phase. Frame mode starts addressing at the value contained in the buffer address register and increments Decrements by stride as it advances from line to line. Initial phase selection is based on the buffer and the vertical Initial phase select bit. Field mode uses the Active Field bit 1 of this register and the reverse Y bit to determine if the start address should be the value in the start address register or the start address register plus minus stride. Field mode will increment decrement the address by two times the stride as it increments from line to line. Initial phase selection is based on the field and the vertical Initial phase select. 0 Frame Mode or called Non Interleaved Buffer Mode 1 Field Mode or called Interleaved Buffer Mode
4	RO		**TEST_MODE:**
3:2	RW		**ACTIVE_BUFFER_POINTER:** Selects which overlay buffer for display. This determines which buffer will be displayed when the overlay is enabled and the Ignore Buffer Field bit 4 of this register is cleared to 0 . It will otherwise be ignored and the internal buffer value with the previously loaded value will be used. The internal buffer value is readable through the status register OC_BUF . 00 Buffer 0 01 Buffer 1 10 Reserved 11 Reserved
1	RW		**ACTIVE_FIELD_SELECT:** Selects which field in an interleaved overlay buffer for display. This determines which field will be displayed when the overlay is enabled and the Ignore Buffer Field bit 4 was cleared to 0 . It will otherwise be ignored and the internal field value with the previously loaded value will be used. The internal buffer value is readable through the status register OC_FIELD . This bit is ignored if Buffer Display Flip Type is in Frame Mode non Interleaved Buffer mode . 0 Field 0 1 Field 1
0	RO		**OVERLAY_ENABLE:** Changing this bit from a Zero to a One will cause the overlay to begin display after the next qualified flip event. This can only be done in conjunction with a flip packet that enables the reconfiguration of the cache using the flush flags. A disable from 1 to 0 will cause the overlay to stop displaying on this current display overlay VBLANK. When Overlay is flipped from one display pipe to another it will be automatically temporarily disabled to allow for the switch. When disabled it will cause the overlay to enter a low power state. Overlay when enabled automatically prevents the special C3 display fetch mode from being activated. There is an override for the enable of this plane in the Pipe Configuration register. Overlay can also be disabled from the pipe control register of the pipe that overlay is assigned to. Full on off changes to the overlay require the shared render cache to be re configured. This must be done through the command stream according to the packet definition. You can leave the cache intact while disabling the overlay command

Bit	Access	Default Value	Description
			register . You cannot enable the overlay without having previously configured the cache. Alviso Grantsdale G Erratum GRG04 This bit must be manually disabled by clearing to 0 when toggling the Overlay Pipe Select bit if BOTH display pipes are enabled. This erratum will be fixed on future products. There are two cases 1 Overlay is disabled prior to enabling and switching to other pipe a Issue Overlay Flip ON request with Overlay Enable bit cleared to 0 and Overlay Pipe Select bit toggled b Issue Overlay Flip CONTINUE request with Overlay Enable bit set to 1 2 Overlay is enabled prior to switching to other pipe a Issue Overlay Flip CONTINUE request with Overlay Enable bit cleared to 0 and Overlay Pipe Select bit toggled b Issue Overlay Flip CONTINUE request with Overlay Enable bit set to 1 Note A wait on flip event is always required between back to back overlay flip requests. 0 Overlay Plane Disable No display or memory fetches default 1 Overlay Plane Enable Requires cache to be configured first

1.11.241 DISPLAY_CONTROLLER.OCONFIG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30164h
MMIO: Base/Offset: MMADR/30164h
IO: Base/Offset:

This register value is mirrored from DDR in address 64h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:** MBZ
26:19	RO		**RESERVED_FOR_SLOT_TIME1:** Programmed for UMA to allow for improved CPU performance.
18	RO		**OVERLAY_PIPE_SELECT:** Changing this bit causes the display to take VBLANK events from both pipes in the proper order to complete the change. An untrusted overlay can be enabled on a trusted pipe the Z order will place all trusted planes above the overlay in Z order. Alviso Grantsdale G Errata GRG04 This bit may not be toggled when BOTH pipes are enabled unless the Overlay Enable bit in the Overlay Command Register is cleared to 0 . See further description under Overlay Enable bit. 0 Overlay is assigned to display pipe A 1 Overlay is assigned to display pipe B
17	RO		**RESERVED2:** MBZ
16	RO		**OVERLAY_SECONDARY_GAMMA_ENABLE:** The secondary gamma refers to the gamma RAM in the graphics pipe that overlay is associated with. This field provides independent control of the secondary gamma logic for overlay pixels. When this bit is in use software MUST make sure that its correspondence compatibility bit 26 of register PIPEACONF at 70008h is set to zero all the time. 0 Overlay pixel data bypasses secondary gamma correction

Bit	Access	Default Value	Description
			logic default . 1 Overlay pixel data is gamma corrected by the secondary correction logic.
15:6	RO		**RESERVED3:** MBZ
5	RO		**YUV2RGB_CONVERSION_MODE:** This bit sets the color space conversion mode for the overlay plane. When bit 4 CSC_BYPASS is set this bit is ignored in the CSC logic since it is in bypass mode.
4	RO		**YUV2RGB_CONVERSION_BYPASS:** This bit sets the overlay data path to bypass the YUV to RGB conversion logic. This bit should only be set when the overlay data is output to compliant external TV encoders in overlay native YUV444 format. The color adjustment controls programmed through brightness contrast and saturation registers are still active. In CSC_BYPASS mode software should also program the overlay gamma to a linear ramp which is the gamma default values. The output YUV data from Overlay contains 10 bit unsigned Y value possibly in the full 0 255 range and 10 bit UV data in excess 512 format. The exact values depend on the mode of the Overlay Color Control Output. Converting to YCrCb range readjustment for 656 TV out is handled separately by the TV Out control logic. 0 Enable the YUV to RGB Color Space Conversion Logic default 1 Bypass Disable the YUV to RGB Color Space Conversion Logic
3	RO		**RESERVED_COLOR_CONTROL_OUTPUT_MODE4:** Sets the output pixel resolution of the Color Control Unit including the piecewise linear gamma correction logic to be either 10 bit or 8 bit. Proper rounding is applied to the pixels. CC_OUT should be set to 1 to enable correct rounding to 8 bit if the backend including the blending unit operates in 8 bit mode. This mode takes affect whether gamma correction is enabled or not. 0 10 bit output. default 1 8 bit output.
2	RO		**SINGLE_REQUEST_MODE:** 0 Single Request disabled 1 Single Request enabled
1	RO		**RESERVED5:** MBZ reserved for future overlay line buffer configuration
0	RO		**LINE_BUFFER_CONFIGURATION:** Sets the overlay line buffer configuration. Using the 2 line mode reduces the peak bandwidth demands of the overlay when down scaling. Configuring the cache for the 2 line mode increases the source line size that will fit in the line buffers. See the appendix for details of the cache configurations and the source size limits based on format and configuration. Other limits are based on available bandwidth. 0 Two line buffers 1 Three line buffers

1.11.242 DISPLAY_CONTROLLER.OGAMC0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30024h
MMIO: Base/Offset: MMADR/30024h

IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to YBlue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.243 DISPLAY_CONTROLLER.OGAMC1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30020h
MMIO: Base/Offset: MMADR/30020h
IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to YBlue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.244 DISPLAY_CONTROLLER.OGAMC2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3001Ch
MMIO: Base/Offset: MMADR/3001Ch
IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to YBlue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.245 DISPLAY_CONTROLLER.OGAMC3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30018h
MMIO: Base/Offset: MMADR/30018h
IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are

the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to YBlue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.246 DISPLAY_CONTROLLER.OGAMC4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30014h
MMIO: Base/Offset: MMADR/30014h
IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to YBlue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**RED:**

15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.247 DISPLAY_CONTROLLER.OGAMC5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30010h
MMIO: Base/Offset: MMADR/30010h
IO: Base/Offset:

These registers are used to determine the characteristics of the gamma correction for the overlay data. The gamma correction receives 8 bit per channel pixels input and sends out 10 bit per channel pixels to the display blender. Each register has 32 bits which are written to and read from together when accessed by the software. They are the six individual breakpoints on a logarithmically spaced color intensity space as shown in the following figure. The two end points 0 and 255 have fixed values 0 and 255 respectively. The appropriate Gamma breakpoint pairs adjacent are selected for each color component Red Green and Blue and the output is interpolated between these two breakpoint values. The difference between any two points should never exceed 7E hex and sequential points must be greater than or equal to the previous point. The Gamma Correction registers GAMC0 to GAMC5 are not double buffered. They should be updated when the overlay is off. Otherwise video anomaly may show. When the output from overlay is set in YUV format by programming CSC bypass normally software should also bypass this gamma unit. However since this gamma unit can also be viewed as a nonlinear transformation it can be used for whatever reason in YUV output mode. In this case the mapping of the three sets of piecewise linear map are as the following Red to Cr also called V Green to YBlue to Cb also called U Errata Overlay fails when gamma point 5 is set to 0x80.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**RED:**
15:8	RW		**GREEN:**
7:0	RW		**BLUE:**

1.11.248 DISPLAY_CONTROLLER.OSTART_0U

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30178h
MMIO: Base/Offset: MMADR/30178h
IO: Base/Offset:

This register value is mirrored from DDR in address 78h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_SURFACE_U_0_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the OBUF_0Y register. When the surface is in linear memory panning is specified using a linear offset in the OBUF_0Y

			register. This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL These registers do not have a readback path through On chip Reg.

1.11.249 DISPLAY_CONTROLLER.OSTART_0V

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3017Ch
MMIO: Base/Offset: MMADR/3017Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 7Ch R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_SURFACE_V_0_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the OBUF_0Y register. When the surface is in linear memory panning is specified using a linear offset in the OBUF_0Y register. This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL These registers do not have a readback path through On chip Reg.

1.11.250 DISPLAY_CONTROLLER.OSTART_0Y

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30170h
MMIO: Base/Offset: MMADR/30170h
IO: Base/Offset:

This register value is mirrored from DDR in address 70h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_SURFACE_Y_0_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the OBUF_0Y register. When the surface is in linear memory panning is specified using a linear offset in the OBUF_0Y register. This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL These registers do not have a readback path through On chip Reg.

1.11.251 DISPLAY_CONTROLLER.OSTART_1U

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30180h

MMIO: Base/Offset: MMADR/30180h
IO: Base/Offset:

This register value is mirrored from DDR in address 80h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_SURFACE_U_1_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the OBUF_0Y register. When the surface is in linear memory panning is specified using a linear offset in the OBUF_0Y register. This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL These registers do not have a readback path through On chip Reg.

1.11.252 DISPLAY_CONTROLLER.OSTART_1V

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30184h
MMIO: Base/Offset: MMADR/30184h
IO: Base/Offset:

This register value is mirrored from DDR in address 84h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_SURFACE_V_1_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the OBUF_0Y register. When the surface is in linear memory panning is specified using a linear offset in the OBUF_0Y register. This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL These registers do not have a readback path through On chip Reg.

1.11.253 DISPLAY_CONTROLLER.OSTART_1Y

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30174h
MMIO: Base/Offset: MMADR/30174h
IO: Base/Offset:

This register value is mirrored from DDR in address 74h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_SURFACE_Y_1_BASE_ADDRESS:** This address specifies the surface base address. When the surface is tiled panning is specified using x y offsets in the

			OBUF_0Y register. When the surface is in linear memory panning is specified using a linear offset in the OBUF_0Y register. This address must be 4K aligned. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT. DevBW and DevCL These registers do not have a readback path through On chip Reg.

1.11.254 DISPLAY_CONTROLLER.OSTRIDE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30118h 3011B
MMIO: Base/Offset: MMADR/30118h 3011B
IO: Base/Offset:

This register value is mirrored from DDR in address 18h R W . These values represent the stride of the overlay video data buffers. A stride value determines the line to line increment of the buffer which is independent of the actual width of the overlay video data that gets displayed. . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:16	RO		**OVERLAY_UV_PLANAR_BUFFER_STRIDE:** Only used for YUV Planar formats and gives the U or V buffer stride in bytes. This is a two s complement number and will be negative when Y mirroring is used with linear memory. Hardware ignores the least significant 6 bits. When using tiled memory the stride must be positive 512 byte aligned and cannot exceed 2kb.
15:0	RO		**OVERLAY_Y_PLANAR_OR_YUV422_PACKED_BUFFER_STRIDE:**

1.11.255 DISPLAY_CONTROLLER.OTEST

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30004h
MMIO: Base/Offset: MMADR/30004h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:3	RO		**RESERVED0:** MBZ
2	RW		**FEATURE_ENABLE:** allow the line buffers in LC to be filled up during vblank before overlay to start sending pixels down the pixel pipeline.
1:0	RW		**UNKNOWN:**

1.11.256 DISPLAY_CONTROLLER.OTILEOFF_0U

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30190h
MMIO: Base/Offset: MMADR/30190h
IO: Base/Offset:

This register value is mirrored from DDR in address 90h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:16	RO		**SOURCE_START_Y_POSITION:**
15:12	RO		**RESERVED1:**
11:0	RO		**SOURCE_START_X_POSITION:**

1.11.257 DISPLAY_CONTROLLER.OTILEOFF_0V

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30194h
MMIO: Base/Offset: MMADR/30194h
IO: Base/Offset:

This register value is mirrored from DDR in address 94h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:16	RO		**SOURCE_START_Y_POSITION:**
15:12	RO		**RESERVED1:**
11:0	RO		**SOURCE_START_X_POSITION:**

1.11.258 DISPLAY_CONTROLLER.OTILEOFF_0Y

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30188h
MMIO: Base/Offset: MMADR/30188h
IO: Base/Offset:

This register value is mirrored from DDR in address 88h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:16	RO		**SOURCE_START_Y_POSITION:**
15:12	RO		**RESERVED1:**
11:0	RO		**SOURCE_START_X_POSITION:**

1.11.259 DISPLAY_CONTROLLER.OTILEOFF_1U

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30198h
MMIO: Base/Offset: MMADR/30198h
IO: Base/Offset:

This register value is mirrored from DDR in address 98h R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:16	RO		**SOURCE_START_Y_POSITION:**
15:12	RO		**RESERVED1:**
11:0	RO		**SOURCE_START_X_POSITION:**

1.11.260 DISPLAY_CONTROLLER.OTILEOFF_1V

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3019Ch
MMIO: Base/Offset: MMADR/3019Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 9Ch R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:16	RO		**SOURCE_START_Y_POSITION:**
15:12	RO		**RESERVED1:**
11:0	RO		**SOURCE_START_X_POSITION:**

1.11.261 DISPLAY_CONTROLLER.OTILEOFF_1Y

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3018Ch
MMIO: Base/Offset: MMADR/3018Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 8Ch R W . This register specifies the panning for the overlay surface. Bit 19 of OCOMD specifies whether the overlay surfaces are in linear or tiled memory. When the surface is in linear memory the contents of this register are ignored. When the surface is tiled the start position is specified in this register as an x y offset from the beginning of the surface. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:**
27:16	RO		**SOURCE_START_Y_POSITION:**
15:12	RO		**RESERVED1:**
11:0	RO		**SOURCE_START_X_POSITION:**

1.11.262 DISPLAY_CONTROLLER.OVADD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30000h
MMIO: Base/Offset: MMADR/30000h
IO: Base/Offset:

This register provides a graphics memory address that will be used on the next Overlay register update. This graphics memory address points to an array of Overlay registers. This register cannot be used to flip the overlay if the cache has not been configured through a command pipe flip packet.

Bit	Access	Default Value	Description
31:16	RW		**REGISTER_UPDATE_ADDRESS:** Graphics memory address that will be used on the next Overlay register update. For forward compatibility purpose software must ensure that the graphics memory address is at least 64K aligned i.e. the lower 16 bits are assumed to be zero and do not exceed the proper values .
15:1	RO		**RESERVED0:** MBZ
0	RW		**COEFFICIENT_FLAG:** This bit determines if the coefficients will be loaded in addition to the other overlay registers during an overlay flip. 0 Load registers only do not load coefficients 1 Load registers and coefficients

1.11.263 DISPLAY_CONTROLLER.OVRSYNCPH0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30058h
MMIO: Base/Offset: MMADR/30058h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**DATA_VALID:** This bit informs software that the phase information in the register is valid. It is set when a flip event occurs on the overlay capture or software and is cleared when the register is read.
30	RO		**OVERRUN:** This bit indicates that the register was updated before software had read the register and cleared the valid bit. 0 No overrun has occurred 1 Overrun
29:24	RO		**FRAME:** This field contains the value in the frame counter a free running counter which counts display VBLANK events when the flip occurred. When the frame counter reaches its maximum value it just wraps around to zero.
23:12	RO		**RESERVED0:** MBZ
11:0	RO		**PHASE:** This field indicates the phase in lines between the display VBLANK event and the overlay flip event.

1.11.264 DISPLAY_CONTROLLER.OVRSYNCPH1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3005Ch
MMIO: Base/Offset: MMADR/3005Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**DATA_VALID:** This bit informs software that the phase information in the register is valid. It is set when a flip event occurs on the overlay capture or software and is

Bit	Access	Default Value	Description
			cleared when the register is read.
30	RO		**OVERRUN:** This bit indicates that the register was updated before software had read the register and cleared the valid bit. 0 No overrun has occurred 1 Overrun
29:24	RO		**FRAME:** This field contains the value in the frame counter a free running counter which counts display VBLANK events when the flip occurred. When the frame counter reaches its maximum value it just wraps around to zero.
23:12	RO		**RESERVED0:** MBZ
11:0	RO		**PHASE:** This field indicates the phase in lines between the display VBLANK event and the overlay flip event.

1.11.265 DISPLAY_CONTROLLER.OVRSYNCPH2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30060h
MMIO: Base/Offset: MMADR/30060h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**DATA_VALID:** This bit informs software that the phase information in the register is valid. It is set when a flip event occurs on the overlay capture or software and is cleared when the register is read.
30	RO		**OVERRUN:** This bit indicates that the register was updated before software had read the register and cleared the valid bit. 0 No overrun has occurred 1 Overrun
29:24	RO		**FRAME:** This field contains the value in the frame counter a free running counter which counts display VBLANK events when the flip occurred. When the frame counter reaches its maximum value it just wraps around to zero.
23:12	RO		**RESERVED0:** MBZ
11:0	RO		**PHASE:** This field indicates the phase in lines between the display VBLANK event and the overlay flip event.

1.11.266 DISPLAY_CONTROLLER.OVRSYNCPH3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30064h
MMIO: Base/Offset: MMADR/30064h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**DATA_VALID:** This bit informs software that the phase information in the register is valid. It is set when a flip event occurs on the overlay capture or software and is cleared when the register is read.

Bit	Access	Default Value	Description
30	RO		**OVERRUN:** This bit indicates that the register was updated before software had read the register and cleared the valid bit. 0 No overrun has occurred 1 Overrun
29:24	RO		**FRAME:** This field contains the value in the frame counter a free running counter which counts display VBLANK events when the flip occurred. When the frame counter reaches its maximum value it just wraps around to zero.
23:12	RO		**RESERVED0:** MBZ
11:0	RO		**PHASE:** This field indicates the phase in lines between the display VBLANK event and the overlay flip event.

1.11.267 DISPLAY_CONTROLLER.PFIT_CONTROL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61230h
MMIO: Base/Offset: MMADR/61230h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**PANEL_FITTING_ENABLED:** Disables the panel fitting function by forcing pixels to bypass. Panel fitting must be disabled when running VGA native modes or interlaced modes on the same pipe. Panel fitting should be enabled or disabled before the pipe is enabled. 0 Bypass the panel fitting 1 1 ratio 1 Enable panel fitting Ratios include 1 1
30:29	RW		**PIPE_SELECT:** Indicates the pipe attached to the panel fitter 00 Panel fitter is attached to Display Pipe A. 01 Panel fitter is attached to Display Pipe B. This is the default after reset. 10 Reserved for pipe C 11 Reserved for pipe D
28:26	RW		**SCALING_MODE:** 000 Auto scale source and destination should have the same aspect ratios 001 Programmed scaling Values in register 61234h will be used for horizontal and vertical scaling factors 010 Pillarbox example 4 3 to 16 9 auto conversion use only when destination has wider aspect ratio than source 011 Letterbox example 16 9 to 4 3 auto conversion use only when destination has taller aspect ratio than source 1xx Reserved
25:24	RW		**FILTER_COEFFICIENT_SELECT:** Selects the set of predefined filter coefficients to use for panel fitting 00 Fuzzy filtering 01 Crisp edge enhancing filtering 10 Median between fuzzy and crisp filtering 11 Reserved
23	RW		**DEBUG_FORCE_TWO_LINE_MODE:**
22	RW		**DEBUG_FORCE_THREE_PIXEL_MODE_WHEN_IN_TWO_LINE_MODE:**
21:19	RW		**DEBUG_CREATE_EXTRA_STALLS_IN_VGA_MODE:** 000 No stall 001 33 stall 010 50 stall 011 66 stall 100 75 stall 101 80 stall 110 90 stall 111 Reserved
18:5	RO		**RESERVED0:**

Bit	Access	Default Value	Description
4	RO		**RESERVED1:**
3	RO		**RESERVED2:**
2:0	RO		**RESERVED3:**

1.11.268 DISPLAY_CONTROLLER.PFIT_PGM_RATIOS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61234h
MMIO: Base/Offset: MMADR/61234h
IO: Base/Offset:

When programmed scaling mode Panel Fitting Controls 28 26 001 is selected this determines the vertical and horizontal ratios used for panel fitting scaling. The values should be based on the source sizes and active sizes programmed into the pipe timing registers. The values written into the register should be rounded to the proper number of bits for the best precision. The value programmed should be source size register value 1 active size register value 1 When programmed scaling mode is not selected read back of this register gives the auto generated vertical and horizontal scaling ratios used for panel fitting scaling. Register writes will be ignored. The ratios are calculated each VBLANK. When in HiRes modes the values are based on the source sizes and active sizes programmed into the pipe timing registers. When in VGA modes it is determined by the VGA source sizes calculated by the VGA and active sizes from the pipe timing registers. VGA source sizes may have invalid values due to mode change transitions. These will eventually be correct when the mode change is complete. The value read is internally generated source size register value 1 active size register value 1 For each register field the MSB is the 1 bit integer value and the lower 12 bits are the fractional value. A value of 1.0 will indicate 1 1 scaling. A value greater than 1.0 will indicate downscaling. A value less than 1.0 will indicate upscaling. The vertical and horizontal ratios are usually identical except for when source and active aspect ratios differ.

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:**
28:16	RW		**PANEL_FITTING_VERTICAL_RATIO:** Vertical scaling ratio for panel fitting.
15:13	RO		**RESERVED1:**
12:0	RW		**PANEL_FITTING_HORIZONTAL_RATIO:** Horizontal scaling ratio for panel fitting.

1.11.269 DISPLAY_CONTROLLER.PIPEACONF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70008h
MMIO: Base/Offset: MMADR/70008h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**PIPE_A_ENABLE:** Setting this bit to the value of one turns on pipe A. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at it s lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should contain valid values before this bit is enabled. 1 Enable
30	RW		**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off this bit indicates the true current state of the pipe. 1 Enabled
29	RO		**RESERVED0:**
28:27	RW		**FRAME_START_DELAY:** TEST MODE Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. Care must be taken to insure that there are enough lines during VBLANK to support this setting. 00 Frame Start occurs on the first HBLANK after the start of VBLANK 01 Frame Start occurs on the second HBLANK after the start of VBLANK 10 Frame Start occurs on the third HBLANK after the start of VBLANK 11 Frame Start occurs on the forth HBLANK after the start of VBLANK
26	RO		**RESERVED1:**
25	RW		**FORCE_BORDER:** TEST MODE 0 Normal Operation 1 Color information is ignored and border color is substituted during active region
24	RW		**PIPE_A_GAMMA_UNIT_MODE:** This bit selects which mode the pipe gamma correction logic works in. In the palette mode it behaves as a 3X256x8 RAM lookup. VGA and indexed mode operation should use the palette in 8 bit mode. In the 10 bit gamma mode it will act as a piecewise linear interpolation. Other gamma units such as in the overlay or sprite are unaffected by this bit.
23:21	RW		**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off or in the vertical blank after programming if pipe is enabled. 0xx Progressive 100 Interlaced embedded panel using programmable vertical sync shift. 101 Interlaced using vertical sync shift. Backup option to 110 setting.110 Interlaced with VSYNC HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 Interlaced with Field 0 Only using legacy vertical sync shift. Not used Note VGA display modes sDVO line stall and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output

Bit	Access	Default Value	Description
			to match the specifications of panels that support interlaced mode.
20	RO		**RESERVED2:**
19	RW		**DISPLAY_OVERLAY_PLANES_OFF:** This bit when set will cause all enabled Display and overlay planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit at the next VBLANK. Timing signals continue as they were but the screen becomes blank. Setting the bit back to a zero will then allow the display and overlay planes to resume on the following VBLANK. 0 Normal Operation 1 Planes assigned to this pipe are disabled.
18	RW		**CURSOR_PLANES_OFF:** This bit when set will cause all enabled cursor planes that are assigned to this pipe to be disabled by overriding the current setting of the plane enable bit at the next VBLANK. Timing signals continue as they were but the cursor s no longer appear on the screen. Setting the bit back to a zero will then allow the cursor planes to resume on the following VBLANK. 0 Normal Operation 1 Planes assigned to this pipe are disabled.
17:16	RW		**REFRESH_RATE_CXSR_MODE_ASSOCIATION:**
15:10	RO		**RESERVED3:** Write as zero
9:8	RW		**SCRAMBLING_ENABLE_DEVCTG:** This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 Scrambling disabled Default 01 Scrambling enabled no SR after initialization at loop 2 of training 10 RESERVED 11 Scrambling and SR enabled. Scrambling is reset every 512 BS symbols. DevIntel Atom Processor D2000 series and N2000 Series Reserved
7:5	RW		**BITS_PER_COLOR_DEVCTG:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change in DisplayPort. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 8 bits per color Default 001 10 bits per color 010 6 bits per color 011 RESERVED 1xx RESERVED
4	RW		**DITHERING_ENABLE_DEVCTG_DEVCDV:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled Default 1 Dithering enabled
3:2	RW		**DITHERING_TYPE_DEVCTG_DEVCDV:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 Spatial only default 01 Spatio Temporal 1 10 Spatio Temporal 2 testmode 11 Temporal only testmode
1	RW		**DDA_RESET_DEVCTG_DEVCDV:** 0 Do not reset DDA 1 Reset DDA every 8th display frame

Bit	Access	Default Value	Description
0	RO		**RESERVED4:** Write as zero

1.11.270 DISPLAY_CONTROLLER.PIPEADPLINKM

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70060h
MMIO: Base/Offset: MMADR/70060h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:0	RW		**PIPE_A_LINK_M_VALUE:** Link m n pixel clk ls_clk Please note that in the DisplayPort specification pixel clk is referred to as strm_clk This formula is equivalent to LinkM LinkN stream_clk dot clock Referring to dot clock as in the Intel Atom Processor D2000 series and N2000 Series Display Controller HAS

1.11.271 DISPLAY_CONTROLLER.PIPEADPLINKN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70064h
MMIO: Base/Offset: MMADR/70064h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:0	RW		**PIPE_A_DATA_N_VALUE:** Link m n pixel clk ls_clk Please note that in the DisplayPort specification pixel clk is referred to as strm_clk This formula is equivalent to LinkM LinkN stream_clk dot clock Referring to dot clock as in the Intel Atom Processor D2000 series and N2000 Series Display Controller HAS

1.11.272 DISPLAY_CONTROLLER.PIPEAFRAMEHIGH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70040h
MMIO: Base/Offset: MMADR/70040h
IO: Base/Offset:

Requires that this pipe s PLL is running

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15:0	RO		**PIPE_A_FRAME_COUNT_HIGH:** The counter is reset to zero when the device is reset or when the pipe transitions from off to on. It is incremented when the low frame

Bit	Access	Default Value	Description
			counter rolls over to zero. This counter wraps when the maximum count is reached the next count value will be zero. When combined with the least significant bits of the frame counter forms a 24 bit value that indicates the number of frames since the pipe was enabled. This register should only be read if the display PLL for this display pipe is running. The hardware does not attempt to synchronize this value with the read of the least significant bits. Software must take the appropriate actions when it is desired to form a full frame count value by combining the two portions of the frame counter. The following example is a possible method Read the Frame count high High1 Read the Frame count low Low 1 Pixel1 Read the Frame count high High2 Read the Frame count low 2 Pixel2 Read the Frame count high High3 If Both versions of the frame count high are equal High1 High2 then Frame High1 Low1 Line int Pixel1 Htotal Pixel Pixel1 Line Htotal ElseIf High2 High3 then Frame High2 Low2 Line int Pixel2 Htotal Pixel Pixel2 Line Htotal Else Error Unable to acquire frame number Indicates that the above register read sequence takes more than 256 display frames. EndIf

1.11.273 DISPLAY_CONTROLLER.PIPEAFRAMEPIXEL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70044h
MMIO: Base/Offset: MMADR/70044h
IO: Base/Offset:

Requires that this pipe s PLL be running

Bit	Access	Default Value	Description
31:24	RO		**PIPE_A_FRAME_COUNT_LOW:**
23:0	RO		**PIPE_A_PIXEL_COUNT:** The pixel count and the frame count low operate together if a display frame has for example 64 000 clocks and we are on frame 5 this register value would read Frame 5 Pixel 63 999 on the last pixel of frame five one display clock later it would read Frame 6 Pixel 0. Pixel Count tracks pixels at the output. Even in the most basic cases the actual fetch of the source data for that pixel may occur a significant amount of time before the pixel makes it to the output. In addition there are cases where there is a difference between pixels in the source data and the output. These cases include This field is only to be used for display modes with 16M or less clocks per frame. This is not to be used in VGA display operation.

1.11.274 DISPLAY_CONTROLLER.PIPEAGCMAXBLUE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70018h
MMIO: Base/Offset: MMADR/70018h

IO: Base/Offset:

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16:0	RW		**MAX_BLUE_GAMMA_CORRECTION_POINT:** 129th reference point for blue channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format 11.6 Default 0x10000

1.11.275 DISPLAY_CONTROLLER.PIPEAGCMAXGREEN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70014h
MMIO: Base/Offset: MMADR/70014h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16:0	RW		**MAX_GREEN_GAMMA_CORRECTION_POINT:** 129th reference point for green channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format 11.6 Default 0x10000

1.11.276 DISPLAY_CONTROLLER.PIPEAGCMAXRED

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70010h
MMIO: Base/Offset: MMADR/70010h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16:0	RW		**MAX_RED_GAMMA_CORRECTION_POINT:** 129th reference point for red channel of the pipe piecewise linear gamma correction. The value should always be programmed to be less than or equal to 1024.0. Format 11.6 Default 0x10000

1.11.277 DISPLAY_CONTROLLER.PIPEAGMCHDATAM

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70050h
MMIO: Base/Offset: MMADR/70050h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**RESERVED0:**

30:25	RW		**TU_SIZE:** Default value to program 111111 TU size of 64
24	RO		**RESERVED1:**
23:0	RW		**PIPE_A_DATA_M_VALUE:** Data m n dot clock bytes per pixel ls_clk of lanes Please note that in the DisplayPort specification dot clock is referred to as strm_clk This formula is equivalent to M N stream_clk dot clock symbol_per_pixel of lanes Where symbol_per_pixel 3 bpc 8 Referring to dot clock as in the Intel Atom Processor D2000 series and N2000 Series Display Controller HAS

1.11.278 DISPLAY_CONTROLLER.PIPEAGMCHDATAN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70054h
MMIO: Base/Offset: MMADR/70054h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:0	RW		**PIPE_A_DATA_N_VALUE:** Data m n dot clock bytes per pixel ls_clk of lanes Please note that in the DisplayPort specification dot clock is referred to as strm_clk This formula is equivalent to M N stream_clk dot clock symbol_per_pixel of lanes Where symbol_per_pixel 3 bpc 8 Referring to dot clock as in the Intel Atom Processor D2000 series and N2000 Series Display Controller HAS

1.11.279 DISPLAY_CONTROLLER.PIPEASTAT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70024h
MMIO: Base/Offset: MMADR/70024h
IO: Base/Offset:

This register is the second level of a two level interrupt and status scheme. A single bit in the first line interrupt status register represents the state of this register which is equal to the AND of a status bits with their corresponding enable bits OR ed together. First line interrupt status bits can cause interrupts or writes of the status register to cacheable memory. Bits in this register indicate the status of the display pipe A and can cause interrupt status bit changes in the first level interrupt and status register. Status bits in this register as sticky and once they are set will be cleared by writing a one to that bit. A write of a zero will not have an effect on the corresponding Interrupt status bit. The corresponding enable bits will determine if the interrupt status bit should be used in the first line interrupt status register. When an interrupt occurs the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt. Programming 1. Prior to clearing a Display Pipe sourced interrupt e.g. Display Pipe A VBLANK in the IIR the corresponding interrupt source status in the PIPEASTAT or PIPEBSTAT register e.g. Pipe A VBLANK Interrupt Status bit of PIPEASTAT must first be cleared. Note that clearing these status bits requires writing a 1 to the appropriate bit position.

Bit	Access	Default Value	Description
31	RW		**FIFO_A_UNDER_RUN_STATUS:** Set when a pipe A FIFO under run occurs cleared by a write of a 1. An underrun has occurred on an attempt to pop an empty FIFO. This does not feed into the first line interrupt status register. This will occur naturally during mode changes to be useful it should be cleared after a mode change has occurred. This bit is only valid after Pipe A has been completely configured. 1 FIFO A Underflow occurred 0 FIFO A Underflow did not occur
30	RO		**RESERVED0:**
29	RW		**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt status logic. 0 CRC Error Detect Disabled 1 CRC Error Detect Enabled
28	RW		**CRC_DONE_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt status logic. 0 CRC Done Detect Disabled 1 CRC Done Detect Enabled
27	RW		**GMBUS_EVENT_ENABLE:** This will enable the use of the GMBUS interrupt status bit in the first line interrupt status logic. 0 No GMBUS event enabled 1 GMBUS event enabled
26	RO		**RESERVED1:** Write as zero
25	RW		**VERTICAL_SYNC_INTERRUPT_ENABLE:** This will enable the consideration of the vertical sync interrupt status bit in the first line interrupt logic. 0 Vertical Sync Interrupt Status Disabled 1 Vertical Sync Interrupt Status Enabled
24	RW		**DISPLAY_LINE_COMPARE_ENABLE:** This will enable the consideration of the line compare interrupt status bit in the first line interrupt status logic. 0 Display Line Compare Interrupt Status Disabled 1 Display Line Compare Interrupt Status Enabled
23	RW		**DPST_EVENT_ENABLE:** DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series This interrupt is generated by the DPST logic. 0 No DPST event enabled 1 DPST event enabled
22	RW		**LEGACY_BLC_EVENT_ENABLE:** DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series This will enable writes to the PCI Backlight Control Register to cause and the display A event status to be set and an Interrupt if Display A Event interrupt is enabled. 0 No BLC Event enabled 1 BLC Event enabled
21	RW		**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 Odd Field Event disable 1 Odd Field Event enable
20	RW		**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** This bit should only be used when this pipe is in an interlaced display timing. 0 Even field Event disable 1 Even field Event enable

Bit	Access	Default Value	Description
19	RO		**RESERVED2:** Write as zero.
18	RW		**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt status logic. 0 Start of Vertical Blank Interrupt Status Disabled 1 Start of Vertical Blank Interrupt Status Enabled
17	RW		**VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt status logic. 0 Vertical Blank Interrupt Status Disabled 1 Vertical Blank Interrupt Status Enabled
16	RW		**OVERLAY_REGISTERS_UPDATED_ENABLE:** DevBW and DevCL 0 Overlay Registers have been updated during Vertical Blank Status Disabled 1 Overlay Registers have been updated during Vertical Blank Status Enabled Reserved DevBLC DevCTG DevIntel Atom Processor D2000 series and N2000 Series Write as zero.
15	RO		**RESERVED3:** MBZ
14	RO		**RESERVED4:**
13	RW		**CRC_ERROR_INTERRUPT_STATUS:** This sticky status bit is set when a Pipe A CRC error is detected. It is cleared by a write of a one. For this bit to be meaningful the pipe and pixel clock should be enabled and running. 0 No CRC error has occurred 1 CRC Error Detected
12	RW		**CRC_DONE_INTERRUPT_STATUS:** This sticky status bit is set when Pipe A CRC calculation and compare are complete. It is cleared by a write of a one. For this bit to be meaningful the pipe and pixel clock should be enabled and running. 0 CRC Not Done 1 CRC Done
11	RW		**GMBUS_INTERRUPT_STATUS:** This status bit will be set on a GMBUS event. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 GMBUS event has not occurred 1 GMBUS event has occurred
10	RO		**RESERVED5:**
9	RW		**VERTICAL_SYNC_INTERRUPT_STATUS:** This bit provides a sticky status that is set when a pipe A vertical sync occurs cleared by a write of a 1. For interlaced timing modes this occurs once per field when in progressive it occurs once per frame. For this bit to be meaningful the pipe and pixel clock should be enabled and running. 0 Vertical Sync has not occurred 1 Vertical Sync has occurred
8	RW		**DISPLAY_LINE_COMPARE_INTERRUPT_STATUS:** Set when a pipe A compare match occurs cleared by a write of a 1. 0 Display Line Compare has not been satisfied 1 Display Line Compare has been satisfied
7	RW		**DPST_EVENT_STATUS:** DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the

Bit	Access	Default Value	Description
			value of the bit. Multiple DPST events Histogram or Phase In can cause this bit to be asserted determination of which event occurred is done in the DPST registers. 0 DPST Interrupt has not occurred on pipe A 1 DPST Interrupt has occurred on pipe A
6	RW		**LEGACY_BLC_EVENT_STATUS:** DevCL DevCTG DevIntel Atom Processor D2000 series and N2000 Series This status bit indicates that a write to the PCI Backlight Control Register LBPC has occurred. Software must clear this bit in order to detect subsequent writes for example while servicing the Event Interrupt. This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 No BLC write detected 1 A BLC write was detected
5	RW		**ODD_FIELD_INTERRUPT_STATUS:** This status bit will be set on a Odd field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 Odd Field Vertical Blank has not occurred 1 Odd Field Vertical Blank has occurred
4	RW		**EVEN_FIELD_INTERRUPT_STATUS:** This status bit will be set on a even field VBLANK event. This bit should only be used when this pipe is in an interlaced display timing. For synchronization with register updates the actual event will occur one line after the start of VBLANK. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. Note This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 Even Field Vertical Blank has not occurred 1 Even Field Vertical Blank has occurred
3	RO		**RESERVED6:**
2	RW		**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point the double buffered display registers flip taking their new values. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 Start of Vertical Blank has not occurred 1 Start of Vertical Blank has occurred
1	RW		**VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event when the frame start occurs. The display registers are updated at the start of vertical blank but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs which is the event that triggers this bit. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 Vertical Blank has not occurred 1 Vertical Blank has occurred

Bit	Access	Default Value	Description
0	RW		**OVERLAY_REGISTERS_UPDATED_INTERRUPT_STATUS:** DevBW DevCL DevIntel Atom Processor D2000 series and N2000 Series This is not a pipe A event. It exists in this register for compatibility reasons only. The bit is set when an overlay register update completes cleared by a write of a 1. 0 Overlay Registers update has not occurred 1 Overlay Registers update has occurred. Reserved DevBLC and DevCTG Write as zero.

1.11.280 DISPLAY_CONTROLLER.PIPEA_DSL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70000h
MMIO: Base/Offset: MMADR/70000h
IO: Base/Offset:

This register enables the read back of the display pipe vertical line counter . The display line value is from the display pipe A timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation scan line zero is the first active line of the display. When in VGA centering mode the scan line 0 is the 1stactive scan line of the pseudo border not the centered active VGA image. In interlaced display timings the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Programming Note In order to cause the scan line logic to report the correct Line Counter value the corresponding Display Pipeline timing registers must be programmed to valid non zero e.g. 640x480 60Hz values before enabling the Pipe or programming VGA timing and enabling native VGA.

Bit	Access	Default Value	Description
31	RO		**DEVBLC_DEVCTG_DEVCDV_CURRENT_FIELD:** Provides read back of the current field being displayed on display pipe A. Non TV mode 0 first field odd field 1 second field even field TV mode 1 first field odd field 0 second field even field DevBW and DevCL Reserved Read only.
30:13	RO		**RESERVED0:** Read only.
12:0	RO		**LINE_COUNTER_FOR_DISPLAY_12:** 0 Provides read back of the display pipe A vertical line counter. This is an indication of the current display scan line to be used by software to synchronize with the display.

1.11.281 DISPLAY_CONTROLLER.PIPEA_SLC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//70004h
MMIO: Base/Offset: MMADR/70004h
IO: Base/Offset:

This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands or through

MMIO for DevBLC and DevCTG . They can safely be accessed at any time. The Top and Bottom Line Count Compare registers are compared with the display line values from display A timing generator. The Top compare register operator is a less than or equal while the Bottom compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts status and command stream flow control wait for within range and wait for not within range . For range check the value programmed should be the desired value 1 so for line 0 the value programmed is VTOTAL and for line 1 the value programmed is 0.

Bit	Access	Default Value	Description
31	RW		**INCLUSIVE_EXCLUSIVE:** 1 Inclusive within the range. 0 Exclusive outside of the range.
30:29	RO		**RESERVED0:** Read only.
28:16	RW		**DEVBLC_DEVCTG_DEVCDV_START_SCAN_LINE_NUMBER:** This field specifies the starting scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 . DevBW DevCL End Scan Line Number This field specifies the ending scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 .
15:13	RO		**RESERVED1:** Read only.
12:0	RW		**DEVBLC_DEVCTG_DEVCDV_END_SCAN_LINE_NUMBER:** This field specifies the ending scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 . DevBW and DevCL Start Scan Line Number This field specifies the starting scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 .

1.11.282 DISPLAY_CONTROLLER.PIPEBCONF

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71008h
MMIO: Base/Offset: MMADR/71008h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RW		**PIPE_B_ENABLE:** Setting this bit to the value of one turns on pipe B. This must be done before any planes are enabled on this pipe. Changing it to a zero should only be done when all planes that are assigned to this pipe have been disabled. Turning the pipe enable bit off disables the timing generator in this pipe. Plane disable occurs after the next VBLANK event after the plane is disabled. Synchronization pulses to the display are not maintained if the timing generator is disabled. Power consumption will be at its lowest state when disabled. A separate bit controls the DPLL enable for this pipe. Pipe timing registers should

Bit	Access	Default Value	Description
			contain valid values before this bit is enabled.
30	RW		**PIPE_STATE:** This bit indicates the actual state of the pipe. Since there can be some delay between disabling the pipe and the pipe actually shutting off this bit indicates the true current state of the pipe. 1 Enabled
29	RO		**RESERVED0:** Write as zero.
28:27	RW		**FRAME_START_DELAY:** Used to delay the frame start signal that is sent to the display planes. Normal operation uses the default 00 value and test modes can use the delayed frame start to shorten the test time. This would be set to 00 for normal operation. 00 Frame Start occurs on the first HBLANK after the start of VBLANK 01 Frame Start occurs on the second HBLANK after the start of VBLANK 10 Frame Start occurs on the third HBLANK after the start of VBLANK 11 Frame Start occurs on the forth HBLANK after the start of VBLANK
26	RO		**RESERVED1:** Write as zero.
25	RW		**FORCE_BORDER:** TEST MODE 0 Normal Operation 1 Color information is ignored and border color is substituted during active region
24	RW		**PIPE_B_GAMMA_UNIT_MODE:**
23:21	RW		**INTERLACED_MODE:** These bits are used for software control of interlaced behavior. They are updated immediately if the pipe is off or in the vertical blank after programming if pipe is enabled. 0xx Progressive 100 Interlaced embedded panel using programmable vertical sync shift 101 Interlaced using vertical sync shift. Backup option to setting 110. 110 Interlaced with VSYNC HSYNC Field Indication using legacy vertical sync shift. Used for SDVO. 111 Interlaced with Field 0 Only using legacy vertical sync shift. Not used. Note VGA display modes sDVO line stall and Panel fitting do not work while in interlaced modes Setting the Interlaced embedded panel mode causes hardware to automatically modify the output to match the specifications of panels that support interlaced mode.
20	RO		**RESERVED2:** Write as zero
19	RW		**DISPLAY_OVERLAY_PLANES_OFF:** 0 Normal Operation 1 Planes assigned to this pipe are disabled.
18	RW		**CURSOR_PLANES_OFF:** 0 Normal Operation 1 Planes assigned to this pipe are disabled.
17:16	RW		**REFRESH_RATE_CXSR_MODE_ASSOCIATION:** 11 Reserved
15:10	RO		**RESERVED3:** Write as zero
9:8	RW		**SCRAMBLING_ENABLE_DEVCTG:** This bit enables scrambling for DisplayPort. Software must set this bit appropriately when enabling a DisplayPort output. 00 Scrambling disabled Default 01 Scrambling enabled no SR after initialization at loop 2 of training 10 RESERVED 11

Bit	Access	Default Value	Description
			Scrambling and SR enabled. Scrambling is reset every 512 BS symbols. DevIntel Atom Processor D2000 series and N2000 Series Reserved
7:5	RW		**BITS_PER_COLORDEVCTG_DEVCDV:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change can be done independent of a pixel clock change. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 8 bits per color Default 001 10 bits per color 010 6 bits per color 011 RESERVED 1xx RESERVED
4	RW		**DITHERING_ENABLE_DEVCTG_DEVCDV:** This bit enables dithering for DisplayPort 6bpc or 8bpc modes 0 Dithering disabled Default 1 Dithering enabled
3:2	RW		**DITHERING_TYPE_DEVCTG_DEVCDV:** This bit selects dithering type for DisplayPort 6bpc or 8bpc modes 00 Spatial only default 01 Spatio Temporal 1 10 Spatio Temporal 2 testmode 11 Temporal only testmode
1	RW		**DDA_RESET_DEVCTG_DEVCDV:** 0 Do not reset DDA 1 Reset DDA every 8th display frame
0	RO		**RESERVED4:** Write as zero

1.11.283 DISPLAY_CONTROLLER.PIPEBDPLINKM

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71060h
MMIO: Base/Offset: MMADR/71060h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:0	RW		**PIPE_B_LINK_M_VALUE:** Link m n pixel clk ls_clk Please note that in the DisplayPort specification pixel clk is referred to as strm_clk

1.11.284 DISPLAY_CONTROLLER.PIPEBDPLINKN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71064h
MMIO: Base/Offset: MMADR/71064h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:0	RW		**PIPE_B_DATA_N_VALUE:** Link m n pixel clk ls_clk Please note that in the DisplayPort specification pixel clk is referred to as strm_clk

1.11.285 DISPLAY_CONTROLLER.PIPEBFRAMEHIGH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71040h
MMIO: Base/Offset: MMADR/71040h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:16	RO		**RESERVED0:**
15:0	RO		**PIPE_B_FRAME_COUNT_HIGH:** See PipeAFrameHigh description.

1.11.286 DISPLAY_CONTROLLER.PIPEBFRAMEPIXEL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71044h
MMIO: Base/Offset: MMADR/71044h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**FRAME_COUNT_LOW:**
23:0	RO		**PIXEL_COUNT:**

1.11.287 DISPLAY_CONTROLLER.PIPEBGCMAXBLUE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71018h
MMIO: Base/Offset: MMADR/71018h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16:0	RW		**MAX_BLUE_GAMMA_CORRECTION_POINT:** Format 11.6 Default 0x10000

1.11.288 DISPLAY_CONTROLLER.PIPEBGCMAXGREEN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71014h
MMIO: Base/Offset: MMADR/71014h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16:0	RW		**MAX_GREEN_GAMMA_CORRECTION_POINT:** Format 11.6 Default 0x10000

1.11.289 DISPLAY_CONTROLLER.PIPEBGCMAXRED

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71010h
MMIO: Base/Offset: MMADR/71010h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:17	RO		**RESERVED0:**
16:0	RW		**MAX_RED_GAMMA_CORRECTION_POINT:** Format 11.6 Default 0x10000

1.11.290 DISPLAY_CONTROLLER.PIPEBGMCHDATAM

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71050h
MMIO: Base/Offset: MMADR/71050h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**RESERVED0:**
30:25	RW		**TU_SIZE:** Default value to program 111111 TU size of 64
24	RO		**RESERVED1:**
23:0	RW		**PIPE_B_DATA_M_VALUE:** Data m n dot clock bytes per pixel ls_clk of lanes Please note that in the DisplayPort specification dot clock is referred to as strm_clk

1.11.291 DISPLAY_CONTROLLER.PIPEBGMCHDATAN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71054h
MMIO: Base/Offset: MMADR/71054h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:**
23:0	RW		**PIPE_B_DATA_N_VALUE:** Data m n dot clock bytes per pixel ls_clk of lanes Please note that in the DisplayPort specification dot clock is referred to as strm_clk

1.11.292 DISPLAY_CONTROLLER.PIPEBSRC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6101Ch
MMIO: Base/Offset: MMADR/6101Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**PIPE_B_HORIZONTAL_SOURCE_IMAGE_SIZE:** See pipe A description.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**PIPE_B_VERTICAL_SOURCE_IMAGE_SIZE:** See pipe A description.

1.11.293 DISPLAY_CONTROLLER.PIPEBSTAT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71024h
MMIO: Base/Offset: MMADR/71024h

IO: Base/Offset:

Programming Prior to clearing a Display Pipe sourced interrupt e.g. Display Pipe A VBLANK in the IIR the corresponding interrupt source status in the PIPEASTAT or PIPEBSTAT register e.g. Pipe A VBLANK Interrupt Status bit of PIPEASTAT must first be cleared. Note that clearing these status bits requires writing a 1 to the appropriate bit position.

Bit	Access	Default Value	Description
31	RW		**PIPE_B_UNDERFLOW_STATUS:** This bit is set when an underflow occurs at the display pipe B. It is cleared by writing a one to this bit. This event will occur naturally during mode changes to be effective it should be cleared after a mode change. This bit is only valid after Pipe B has been completely configured. 1 FIFO B Underflow occurred 0 FIFO B Underflow did not occur
30	RO		**RESERVED0:** Write as zero.
29	RW		**CRC_ERROR_ENABLE:** This will enable the consideration of the CRC error status bit in the first line interrupt status logic. 0 CRC Error Detect Disabled 1 CRC Error Detect Enabled
28	RW		**CRC_DONE_ENABLE:** This will enable the consideration of the CRC done status bit in the first line interrupt status logic. 0 CRC Done Detect Disabled 1 CRC Done Detect Enabled
27:26	RO		**RESERVED1:** Write as zero.
25	RW		**VERTICAL_SYNC_INTERRUPT_ENABLE:** 0 Vertical Sync Interrupt Status Disabled 1 Vertical Sync Interrupt Status Enabled
24	RW		**DISPLAY_LINE_COMPARE_ENABLE:** 0 Pipe B Display Line Compare Status Report Disabled 1 Pipe B Display Line Compare Status report Enabled
23	RW		**BLM_EVENT_ENABLE_DEVCL_DEVCTG_DEVCDV:** This interrupt is generated by the image brightness segment comparators. Which segment cause an interrupt are controlled by the BLM Histogram control register. 0 No BLM event enabled 1 BLM event enabled
22	RW		**LEGACY_BLC_EVENT_ENABLE_DEVCL_DEVCTG_DEVCDV :** This will enable writes to the PCI Backlight Control Register to cause an the display B event status to be set and an Interrupt if Display B Event interrupt is enabled. 0 No BLC Event enabled 1 BLC Event enabled
21	RW		**ODD_FIELD_INTERRUPT_EVENT_ENABLE:** 0 Odd Field Event disable 1 Odd Field Event enable
20	RW		**EVEN_FIELD_INTERRUPT_EVENT_ENABLE:** 0 Even field Event disable 1 Even field Event enable
19	RO		**RESERVED2:** Read only as zero
18	RW		**START_OF_VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the start of vertical blank interrupt status bit in the first line interrupt status logic. 0 Start of Vertical Blank Interrupt Status Disabled 1 Start of Vertical Blank Interrupt Status Enabled

Bit	Access	Default Value	Description
17	RW		**VERTICAL_BLANK_INTERRUPT_ENABLE:** This will enable the consideration of the vertical blank interrupt status bit in the first line interrupt status logic. 0 Vertical Blank Interrupt Status Disabled 1 Vertical Blank Interrupt Status Enabled
16	RO		**RESERVED3:** Write as zero.
15:14	RO		**RESERVED4:** Read only.
13	RW		**CRC_ERROR_STATUS:** This bit is set when a Pipe B CRC error is detected. It is cleared by a write of a one. 0 No CRC Error 1 CRC Error detected
12	RW		**CRC_DONE_INTERRUPT_STATUS:** This bit is set when Pipe B CRC calculation and compare are complete. It is cleared by a write of a one. 0 CRC Not Done 1 CRC Done
11:10	RO		**RESERVED5:**
9	RW		**PIPE_B_VERTICAL_SYNC_STATUS:** 0 Vertical Sync not asserted 1 Vertical Sync asserted
8	RW		**PIPE_B_DISPLAY_LINE_COMPARE_STATUS:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 Display Line Compare Status not asserted 1 Display Line Compare Status asserted
7	RW		**BLM_IMAGE_BRIGHTNESS_STATUS_DEVCL_DEVCTG_DEVCDV:** This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 DPST Interrupt has not occurred on pipe B 1 DPST Interrupt has occurred on pipe B
6	RW		**LEGACY_BLC_EVENT_STATUS_DEVCL_DEVCTG_DEVCDV:** This status bit indicates that a write to the PCI Backlight Control Register LBPC has occurred. Software must clear this bit in order to detect subsequent writes for example while servicing the Event Interrupt. This bit is cleared when a write to this register occurs with this bit as a one. Writes with this bit as a zero has no effect on the value of the bit. 0 No BLC write detected 1 A BLC write was detected
5	RW		**ODD_FIELD_INTERRUPT_STATUS:** Note This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 Odd Field Vertical Blank has not occurred 1 Odd Field Vertical Blank has occurred
4	RW		**EVEN_FIELD_INTERRUPT_STATUS:** Note This bit will not be set when pipe is in Interlaced with Field 0 Only using legacy vertical sync shift mode. 0 Even Field Vertical Blank has not occurred 1 Even Field Vertical Blank has occurred
3	RO		**RESERVED6:** Read only write as zero
2	RW		**START_OF_VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set at the beginning of a VBLANK event. At this point the double buffered display registers flip taking their new values. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 Start of Vertical Blank has not occurred 1 Start of Vertical Blank has occurred

Bit	Access	Default Value	Description
1	RW		**VERTICAL_BLANK_INTERRUPT_STATUS:** This status bit will be set on a VBLANK event when the frame start occurs. The display registers are updated at the start of vertical blank but the new register data is not utilized by the display pipeline until the point in the vertical blank period when the frame start occurs which is the event that triggers this bit. To use this bit in a polling manner clear the bit by writing a one to it followed by the polling loop waiting for it to become set. 0 Vertical Blank has not occurred 1 Vertical Blank has occurred
0	RO		**RESERVED7:** Read only write as zero

1.11.294 DISPLAY_CONTROLLER.PIPEB_DSLDISPLAY_SCAN_LINE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71000h
MMIO: Base/Offset: MMADR/71000h
IO: Base/Offset:

This register enables the read back of the display pipe vertical line counter . The display line value is from the display pipe B timing generator and is reset to zero at the beginning of a scan. The value increments at the leading edge of HSYNC and can be safely read any time. For normal operation scan line zero is the first active line of the display. When in VGA centering mode the scan line 0 is the 1stactive scan line of the pseudo border not the centered active VGA image display area. In interlaced display timings the scan line counter provides the current line in the field. One field will have a total number of lines that is one greater than the other field. Programming Note In order to cause the scan line logic to report the correct Line Counter value the corresponding Display Pipeline timing registers must be programmed to valid non zero e.g. 640x480 60Hz values before enabling the Pipe or programming VGA timing and enabling native VGA.

Bit	Access	Default Value	Description
31	RO		**DEVBLC_DEVCTG_DEVCDV_CURRENT_FIELD:** Provides read back of the current field being displayed on display pipe B. Non TV mode 0 first field odd field 1 second field even field TV mode 1 first field odd field 0 second field even field DevBW and DevCL Reserved Read only.
30:13	RO		**RESERVED0:** Read only.
12:0	RO		**PIPE_B_DISPLAY_LINE_COUNTER:** This register enables the read back of the display vertical line counter . The display line values are from the pipe B timing generator. They change at the leading edge of HSYNC and can be safely read at any time.

1.11.295 DISPLAY_CONTROLLER.PIPEB_SLC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71004h
MMIO: Base/Offset: MMADR/71004h
IO: Base/Offset:

The Start and End Line Count Compare registers are compared with the display line values from the timing generator. They change at the leading edge of HSYNC. They can safely be accessed at any time. The End compare register operator is a less than or equal while the Start compare register operator is a greater than or equal. The results of these 2 comparisons are communicated to the command stream controller for generating interrupts status and command stream flow control wait for within range and wait for not within range . For range check the value programmed should be the desired value 1. So for line 0 the value programmed is VTOTAL and for line 1 the value programmed is 0. This register can be written via the command stream processor using the MI_LOAD_SCAN_LINES_INCL or MI_LOAD_SCAN_LINES_EXCL commands or through MMIO for DevBLC and DevCTG.

Bit	Access	Default Value	Description
31	RW		**INCLUSIVE_EXCLUSIVE:** 0 Exclusive Out of Range
30:29	RO		**RESERVED0:** Read only.
28:16	RW		**DEVBLC_DEVCTG_DEVCDV_START_SCAN_LINE_NUMBER:** This field specifies the starting scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 . DevBW and DevCL End Scan Line Number This field specifies the ending scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 .
15:13	RO		**RESERVED1:** Read only.
12:0	RW		**DEVBLC_DEVCTG_DEVCDV_END_SCAN_LINE_NUMBER:** This field specifies the ending scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 . DevBW and DevCL Start Scan Line Number This field specifies the starting scan line number of the Scan Line Window. Format U16 in scan lines where scan line 0 is the first line of the display frame. Range 0 Display Buffer height in lines 1 .

1.11.296 DISPLAY_CONTROLLER.PIPESRCA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6001Ch
MMIO: Base/Offset: MMADR/6001Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:28	RO		**RESERVED0:** Write as zero
27:16	RW		**PIPE_A_HORIZONTAL_SOURCE_IMAGE_SIZE:** This 12 bit field specifies Horizontal source image size up to 4096. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one. The actual source size must be two times the programmed value in the pixel multiply mode.
15:12	RO		**RESERVED1:** Write as zero
11:0	RW		**PIPE_A_VERTICAL_SOURCE_IMAGE_SIZE:** This 12 bit field specifies the vertical source image size up to 4096 lines. This determines the size of the image created by the display planes sent to the blender. The value programmed should be the source image size minus one.

1.11.297 DISPLAY_CONTROLLER.PORT_HOTPLUG_EN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61110h
MMIO: Base/Offset: MMADR/61110h
IO: Base/Offset:

Description DPD enable control dprrega.v ql_hotplugen_Q NOTE For correct operation of display port hot plug detection the device 2 configuration register GMBUSFREQ at offset 0xCC 0xCD must be programmed correctly.

Bit	Access	Default Value	Description
31:30	RO		**RESERVED0:** mbz
29	RW		**DEVCDV_DEVCTG_DEVELK_DISPLAYPORT_HDMI_B_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort B in the Port Hotplug Status register offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt it must not be cleared and reset as part of interrupt processing. 0 DisplayPort or HDMIB Hot Plug Detect Disabled Default 1 DisplayPort or HDMIB Hot Plug Detect Enabled
28	RW		**DEVCDV_DEVCTG_DEVELK_DISPLAYPORT_HDMI_C_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort C in the Port Hotplug Status register offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state.

Bit	Access	Default Value	Description
			Since setting this bit may generate an interrupt it must not be cleared and reset as part of interrupt processing. 0 DisplayPort or HDMIC Hot Plug Detect Disabled Default 1 DisplayPort or HDMIC Hot Plug Detect Enabled
27	RW		**DEVCTG_DISPLAYPORT_HDMI_D_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit for DisplayPort D in the Port Hotplug Status register offset 61114h. Please note that software must set this bit at boot in order to detect the HPD input buffer live state. Since setting this bit may generate an interrupt it must not be cleared and reset as part of interrupt processing. 0 DisplayPort or HDMID Hot Plug Detect Disabled Default 1 DisplayPort or HDMID Hot Plug Detect Enabled
26	RW		**DEVCTG_SDVOB_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register offset 61114h. This bit enables detection on the SDVOB interrupt input pin pair. 0 SDVOB Hot Plug Detect Disabled Default 1 SDVOB Hot Plug Detect Enabled
25	RW		**DEVCTG_SDVOC_HOT_PLUG_INTERRUPT_DETECT_ENABLE:** This will enable the consideration of the hot plug interrupt status bit in the Port Hotplug Status register offset 61114h. This bit enables detection on the SDVOC interrupt input pin pair. 0 SDVOC Hot Plug Detect Disabled Default 1 SDVOC Hot Plug Detect Enabled
24	RW		**DEVCDV_DEVCL_DEVCTG_AUDIO_INTERRUPT_DETECT_ENABLE:** This bit enables consideration of the audio interrupt status bit in the Port Hotplug Status Register offset 61114h. It relates to the HDMI port that has audio enabled and can only be used in combination with TMDS encoding. This bit is only to be used for integrated HDMI. 0 Audio interrupt detect disabled Default 1 Audio interrupt detect enabled
23:19	RO		**RESERVED1:** mbz
18	RW		**DEVCL_DEVCTG_TV_HOT_PLUG_DETECT_INTERRUPT_ENABLE:** 0 TV Hot Plug Detect Disabled bit 10 of the port hotplug status register no longer detects interrupts Default 1 TV Hot Plug Detect Enabled
17:16	RW		**DEVCDV_DEVCTG_DEVELK_DP_HOTPLUG_SHORT_PULSE_DURATION:** These bits define the duration of the pulse defined as a short pulse for DisplayPort ports. 00 2mS Default 01 4.5mS 10 6mS 11 100mS
15:10	RO		**RESERVED2:** mbz
9	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_CRT_HOT_PLUG_INTERRUPT_ENABLE:** Hotplug detection is used to cause an interrupt or status bit based on the connection or disconnection of a CRT to the analog video connection. 0 No hot plug interrupt is enabled Default 1 Hot plug detection is enabled
8	RW		**DEVCDV_DEVCTG_CRT_HOT_PLUG_CIRCUIT_ACTIV**

Bit	Access	Default Value	Description
			ATION_PERIOD: This bit sets the activation period for the CRT hot plug circuit detection. Setting this bit to 1 is required for the correct operation of CRT DAC detection. 0 32 cdclk periods Default 1 64 cdclk periods
7	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_CRT_DAC_ON_TIME_VALUE:** Powerup time for 0 CRT DAC requires 2M cdclks for warmup Default 1 CRT DAC requires 4M cdclks for warmup
6:5	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_CRT_HOT_PLUG_VOLTAGE_COMPARE_VALUE:** Compare value for CRT hotplug detect Vref to determine whether the analog port is connected to a CRT. The voltage is forced at the beginning of the active region of the screen every 2 seconds. 00 A0 01 B0 Default 10 C0 11 D0
4	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_CRT_HOT_PLUG_DETECT_DELAY:** This bit determines the length of time between polling periods when the DAC pipe are disabled 0 1G cdclks default 1 2G cdclks
3	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_FORCE_CRT_DETECT_TRIGGER:** Triggers a CRT hotplug unplug detection cycle independent of the interrupt enable bit. Bits 5 8 of this register must be correctly programmed when forcing a trigger. This bit is automatically cleared after the detection is completed. The result of this trigger is reflected in bits 9 8 of the port hotplug interrupt status register. The CRT interrupt status bit 11 in the hot plug status register 61114 will get set the first time Force CRC detect trigger is used after reset. Software must reset status after a force CRT detect trigger. 0 No trigger Default 1 Trigger
2	RW		**DEVCTG_B_CRT_DAC_HOT_PLUG_DETECTION_REFERENCE_VOLTAGE_SELECTION:** 0 325mv bits 6 5 should be set to 01 Default 1 475mv bits 6 5 should be set to 11
1:0	RO		**RESERVED3:** mbz

1.11.298 DISPLAY_CONTROLLER.PORT_HOTPLUG_STAT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61114h
MMIO: Base/Offset: MMADR/61114h
IO: Base/Offset:

Description CRT port control dprrega.v porthotst_aR This register is the second level of a two level interrupt and status scheme. Status bits in this register are sticky once set they can be cleared by writing a one to that bit. A write of a zero does not affect the corresponding Interrupt status bit. The corresponding enable bits determine if the interrupt status bit should be propagated to the first line interrupt status register. When an interrupt occurs the first line interrupt register indicates the second line source of the interrupt. Reading the second line register will determine the precise source for the interrupt. Before clearing a Port sourced interrupt e.g. CRT hotplug in the IIR the corresponding interrupt source status in the PORT_HOTPLUG_STAT must

be cleared by writing a 1 to the appropriate bit. In the case where fields are larger than 1 bit wide all bits in the field must be cleared by writing a 1 to them.

Bit	Access	Default Value	Description
31:30	RO		**RESERVED0:** mbz
29	RW		**DEVCDV_DEVCTG_DEVELK_DISPLAYPORT_HDMIB_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** This bit is read only. It reflects the real time state of the of the hot plug input HPD pin on DisplayPort or HDMI B when bit 29 of the hotplug enable register offset 61110h is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 HPD detected active 0 HPD detected inactive
28	RW		**DEVCDV_DEVCTG_DEVELK_DISPLAYPORT_HDMIC_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** This bit is read only. It reflects the real time state of the of the hot plug input HPD pin on DisplayPortC when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. This bit should be read to confirm cable connection prior to attempting EDID read. 1 HPD detected high 0 HPD detected low
27	RW		**DEVCTG_DISPLAYPORTD_HOT_PLUG_INPUT_BUFFER_LIVE_STATE:** This bit is read only. It reflects the real time state of the of the hot plug input HPD pin on DisplayPortD when bit of this register is set. This pin signal is active high. This does not feed into the first line interrupt status register. Please note that port D is intended for LFP use and therefore HPD may not be present. Bit 2 of the DPD control register must therefore be read to determine whether DPD is used in the system. 1 HPD detected high 0 HPD detected low
26:23	RO		**RESERVED1:** mbz
22:21	RW		**DEVCTG_DISPLAYPORT_D_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on DisplayPort D. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 27 of the hotplug enable status register is set. 00 DisplayPort D Hot Plug event not detected 1x DisplayPort D long pulse Hot Plug event detected X1 DisplayPort D short pulse Hot Plug event detected
20:19	RW		**DEVCDV_DEVCTG_DEVELK_DISPLAYPORT_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on DisplayPort or HDMI C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 28 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 28 the hot plug input buffer live state when determining further action if bit 28 0 the bits should be cleared and the port must be disabled. 00 DisplayPort HDMI C Hot Plug event not detected 1x DisplayPort HDMI C long pulse Hot Plug event detected X1 DisplayPort C short pulse Hot Plug event detected
18:17	RW		**DEVCDV_DEVCTG_DEVELK_DISPLAYPORT_B_HOT_PLUG**

Bit	Access	Default Value	Description
			_INTERRUPT_DETECT_STATUS: This reflects hot plug interrupt status on DisplayPort B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of a sink event. This bit feeds into the first line interrupt status register when bit 29 of the hotplug enable status register is set. Please note that these bits should be considered in conjunction with bit 29 the hot plug input buffer live state when determining further action if bit 29 0 the bits should be cleared and the port must be disabled. 00 DisplayPort HDMI B Hot Plug event not detected 1x DisplayPort HDMI B long pulse Hot Plug event detected X1 DisplayPort B short pulse Hot Plug event detected
16	RW		**DEVCDV_DEVCTG_DEVCL_AUDIO_INTERRUPT_LIVE_STATE:** This read only bit is used only in ports that use TMDS encoding. It reflects the state of the audio interrupt request for HDCP when bit 1 of this register is set. This pin signal is active high. It does not feed into the first line interrupt status register. 1 HDCP invocation requested from audio 0 HDCP disable requested from audio
15	RW		**DEVCDV_DEVCTG_DEVCL_DIGITAL_PORT_B_AUDIO_REQUEST_LIVE_STATE:** This read only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 17 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 HDCP invocation requested from audio 0 HDCP disable requested from audio
14	RW		**DEVCDV_DEVCTG_DEVCL_DIGITAL_PORT_C_AUDIO_REQUEST_LIVE_STATE:** This read only bit is only used on ports using audio. It reflects the state of audio HDCP request when bit 19 of this register is set if audio is enabled on this port. This pin signal is active high. This does not feed into the first line interrupt status register. 1 HDCP invocation requested from audio 0 HDCP disable requested from audio
13:12	RO		**RESERVED2:** mbz
11	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_CRT_HOT_PLUG_INTERRUPT_STATUS:** This bit is set when a CRT hot plug or unplug event has been detected. A hot plug or unplug event is defined as the change in connection state of the CRT as determined by the hardware CRT detect sequence which is enabled through bit 9 CRT hot plug interrupt enable or bit 3 Force CRT detect trigger in the Port_HotPlug_En register 0x61110. After reset the CRT is considered unconnected even if physically connected until the first detect sequence occurs. Physically plugging or unplugging the CRT device will also be detected as a change of connection state. Writing a 1 to this bit clears it. 0 CRT Interrupt has not occurred 1 CRT Interrupt has occurred
10	RW		**DEVCTG_DEVBW_DEVCL_DEVBLC_TV_HOT_PLUG_INTERRUPT_STATUS:** This bit is set when a TV hot plug or unplug event has been detected. Reflects the state of bit 31 of the TV DAC state register offset 68004 68007h. Software must write a one to these bits to clear the status. 0 TV Interrupt has not occurred 1 TV Interrupt has occurred

Bit	Access	Default Value	Description
9:8	RO		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_CRT_HOT_PLUG_DETECTION_STATUS:** These bits are set when a CRT hot plug or unplug event has been detected. 00 No channels attached default 01 Blue channel only is attached 10 Green channel only is attached 11 Both blue and green channel attached
7	RO		**RESERVED3:** mbz
6	RW		**DEVCTG_DISPLAYPORT_D_AUX_INTERRUPT_STATUS:** This bit is set when a transaction on AUX channel D has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel D control register is set. Writing a 1 to this bit clears it. 0 AUX channel D Interrupt has not occurred 1 AUX channel D Interrupt has occurred
5:4	RW		**DEVBW_DEVCL_DEVBLC_SDVO_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on SDVO port C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 25 of the hotplug enable status register is set. 00 SDVO C Hot Plug event not detected x1 SDVO C long pulse gt 50mS Hot Plug event detected 1x SDVO C short pulse lt 50mS Hot Plug event detected
5	RW		**DEVCTG_DEVCDV_DISPLAYPORT_C_AUX_INTERRUPT_STATUS:** This bit is set when a transaction on AUX channel C has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel C control register is set. Writing a 1 to this bit clears it. 0 AUX channel C Interrupt has not occurred 1 AUX channel C Interrupt has occurred
4	RW		**DEVCTG_DEVCDV_DISPLAYPORT_B_AUX_INTERRUPT_STATUS:** This bit is set when a transaction on AUX channel B has completed or timed out. This bit feeds into the first line interrupt status register when bit 29 of the AUX channel B control register is set. Writing a 1 to this bit clears it. 0 AUX channel B Interrupt has not occurred 1 AUX channel B Interrupt has occurred
3:2	RW		**DEVBW_DEVCL_DEVBLC_SDVO_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on SDVO port B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 26 of the hotplug enable status register is set. 00 SDVO B Hot Plug event not detected x1 SDVO B long pulse gt 50mS Hot Plug event detected 1x SDVO B short pulse 50mS Hot Plug event detected
3	RW		**DEVCTG_DEVCDV_SDVO_C_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on SDVO port C. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of an HDCP state change request from the audio

Bit	Access	Default Value	Description
			driver over SDVO only. This bit feeds into the first line interrupt status register when bit 25 of the hotplug enable status register is set. 0 SDVO Hot Plug event not detected 1 SDVO Hot Plug event detected
2	RW		**DEVCTG_DEVCDV_SDVO_B_HOT_PLUG_INTERRUPT_DETECT_STATUS:** This reflects hot plug interrupt status on SDVO port B. Graphics software must write a one to these bits to clear the status. This bit is used for either monitor hotplug unplug or for notification of an HDCP state change request from the audio driver over SDVO only. This bit feeds into the first line interrupt status register when bit 26 of the hotplug enable status register is set. 0 SDVO Hot Plug event not detected 1 SDVO Hot Plug event detected
1	RW		**DEVCTG_DEVCDV_DEVCL_AUDIO_INTERRUPT_DETECT_STATUS:** This reflects a request for integrated HDCP state change set by audio driver and propagated through the audio hardware. The graphics software must write a one to this bit to clear the status. Upon clearing this bit the audio ready bit is cleared in the audio registers. The graphics software then must reset audio ready bit 14 in the audio control register offset 620B4h to 1 when the HDCP interrupt has been serviced. This bit feeds into the first line interrupt status register when bit 24 of the hotplug enable status register is set 0 Audio interrupt event not detected 1 Audio interrupt event detected
0	RO		**RESERVED4:** mbz

1.11.299 DISPLAY_CONTROLLER.PP_CONTROL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61204h
MMIO: Base/Offset: MMADR/61204h
IO: Base/Offset:

Description PP Control dplrreg.v pnl_pwr_cntl

Bit	Access	Default Value	Description
31:16	RW		**WRITE_PROTECT_KEY:** ABCD Write protect off When this field is programmed to anything except the write protect off setting and the panel is either powered up or in the process of a power up sequence a set of registers involved in generation of panel timing or control become write protected. Any write cycles to those write protected registers while they will complete as normal will not change the value of the register when write protected. When this register field contains the write protect off key value write protect will be unconditionally disabled. In situations where the embedded panel port is unused the port should remain powered down and the write protect will be inactive. This field in normal operation should be left to all zeros and never programmed with the key value. It exists only to allow testing and workarounds. List of Write protected registers LVDS and Panel sequencing Registers LVDS Digital Display Port Control Address

Bit	Access	Default Value	Description
			61180h 61183h Panel power on sequencing delays Address 61208 6120Bh Panel power off sequencing delays Address 6120Ch 6120Fh Panel power cycle delay and Reference Divisor Address 61210h 61213 DPLL registers DPLL Control Registers FPA0 DPLL Divisor Register FPA1 DPLL Divisor Register 1 FPB0 DPLL Divisor Register FPB1 DPLL Divisor Register 1 Display Pipe timing registers except source size HTOTAL Horizontal Total Register HBLANK Horizontal Blank Register HSYNC_ Horizontal Sync Register VTOTAL_ Vertical Total Register VBLANK_ Vertical Blank Register VSYNC_ Vertical Sync Register
15:4	RO		**RESERVED0:**
3	RW		**EDP_PANEL_VDD_ENABLE_DEVCDV:** Enabling this bit enables the panel vdd if the embedded panel is DisplayPort as indicated in bits 31 30 of the panel power on sequencing. Software must enable this bit for eDP link training. After eDP link training is done software must disable it and let the normal panel power sequencing to take control. 0 eDP panel Vdd disabled 1 eDP panel Vdd enabled DevCLN Reserved
2	RW		**BACKLIGHT_ENABLE_DEVCTG_DEVCDV:** Enabling this bit enables the panel backlight if the embedded panel is DisplayPort as indicated in bits 31 30 of the panel power on sequencing. Software must enable this bit after training the link and disable it when disabling the panel power state target. 0 Backlight disabled 1 Backlight enabled DevCL Reserved
1	RW		**POWER_DOWN_ON_RESET:** Enabling this bit causes the panel to power down when a reset warning comes to the GMCH from the ICH. When system reset is initiated the embedded panel port automatically begins the panel power down sequence. If the panel is not on during a reset event this bit is ignored. 0 Do not run panel power down sequence when reset is detected 1 Run panel power down sequence when system is reset
0	RW		**POWER_STATE_TARGET:** Writing this bit can occur any time it will only be used at the completion of any current power cycle. 0 The panel power state target is off if the panel is either on or in a power on sequence a power off sequence is started as soon as the panel reaches the power on state. This may include a power cycle delay. If the panel is currently off there is no change of the power state or sequencing done. 1 The panel power state target is on if the panel is in either the off state or a power off sequence if all pre conditions are met a power on sequence is started as soon as the panel reaches the power off state. This may include a power cycle delay. If the panel is currently off there is no change of the power state or sequencing done. While the panel is on or in a power on sequence the register write lock will be enabled.

1.11.300 DISPLAY_CONTROLLER.PP_DIVISOR

PCI: B/D/F/Reg:

SBI: Port/Reg/Mem: 06h//61210h
MMIO: Base/Offset: MMADR/61210h
IO: Base/Offset:

Description PP Divisor dplrreg.v DPLRrefdiv_pp_cd Write Protect by Panel Power Sequencer on Mobile Products. This register selects the reference divisor and controls how long the panel must remain in a power off condition once powered down. This has a default value that allows a timer to initiate directly after device reset. If the panel limits how fast we may sequence from up to down to up again. Typically this is .5 1.5 sec. But limited to 400ms in the SPWG specification. This register forces the panel to stay off for a programmed duration. Special care is needed around reset and D3 cold situations to conform to power cycle delay specifications.

Bit	Access	Default Value	Description
31:8	RW		**REFERENCE_DIVIDER:** This field provides the value of the divider used for the creation of the panel timer reference clock. The output of the divider is used as the fastest of the three time bases 100us for all other timers. The other time bases are divided from this frequency. The value of zero should not be used. When it is desired to divide by N the actual value to be programmed is N 2 1. The value should be 100 RefinMHz 2 1. The default value assumes the default value for the display core clock that is for DevCL and DevCTG a 200MHz reference value. The following are examples for other memory speeds. Display Core Frequency Value of Field 233MHz 2D81h 200MHz 270Fh 133MHz 19F9h
7:5	RO		**RESERVED0:**
4:0	RW		**POWER_CYCLE_DELAY:** Programmable value of time panel must remain in a powered down state after powering down. For devices coming out of reset the default values will define how much time must pass before a power on sequence can be started. This field uses the .1 S time base unit from the divider. If the panel power on sequence is attempted during this delay the power on sequence will commence once the power cycle delay is complete. Writing a value of 0 selects no delay or is used to abort the delay if it is active. During the initial power up reset a D3 cold power cycle or a user instigated system reset the timer will be set to the default value and the countdown will begin after the de assertion of reset. Writing this field to a zero while the count is active will abort this portion of the sequence. This corresponds to the T4 of the SPWG specification. Note Even if the panel is not enabled the T4 count happens after reset. This register needs to be programmed to a 1 value. For instance for meeting the SPWG specification of 400mS program 5 to achieve at least 400 mS delay prior to power-up.

1.11.301 DISPLAY_CONTROLLER.PP_OFF_DELAYS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6120Ch
MMIO: Base/Offset: MMADR/6120Ch
IO: Base/Offset:

Description PP Delay Off values dplrreg.v DPLRppoff_sd Write Protect by Panel Power Sequencer on Mobile products

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:**
28:16	RW		**POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power up. This provides the time delay for the T3 T5 for DisplayPort time sequence. The time unit used is the 100us timer.
15:13	RO		**RESERVED1:**
12:0	RW		**POWER_BACKLIGHT_OFF_TO_POWER_DOWN_DELAY:** Programmable value of panel power sequencing delay during power down. This provides the time delay for the Tx T4 for DisplayPort time sequence. The time unit used is the 100us timer.

1.11.302 DISPLAY_CONTROLLER.PP_ON_DELAYS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61208h
MMIO: Base/Offset: MMADR/61208h
IO: Base/Offset:

Description PP On Delay values dplrreg.v DPLRppon_sd Write Protect by Panel Power Sequencer on

Bit	Access	Default Value	Description
31:30	RW		**PANEL_CONTROL_PORT_SELECT:** These bits define to which port the embedded panel is connected. This is used for automatic control of the panel power. If the selected port is disabled or if the port is not on pipe B then the power sequence will not allow a panel power up. 00 Panel is connected to the LVDS display port 01 Panel is connected to the embedded DisplayPort 10 Reserved 11 Reserved The selection of nonexistent ports are not allowed. This programming will disable panel power sequencing logic.
29	RO		**RESERVED0:**
28:16	RW		**POWER_UP_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T1 T2 time sequence. The time unit used is the 100us timer.
15:13	RO		**RESERVED1:**
12:0	RW		**POWER_ON_TO_BACKLIGHT_ENABLE_DELAY:** Programmable value of panel power sequencing delay during panel power up. This provides the time delay for the T5 T3 for DisplayPort time sequence. The time unit used is the 100us timer.

1.11.303 DISPLAY_CONTROLLER.PP_STATUS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61200h
MMIO: Base/Offset: MMADR/61200h
IO: Base/Offset:

Bit	Access	Default Value	Description
31	RO		**PANEL_POWER_ON_STATUS:** 0 Indicates that the panel power down sequencing has completed. A power cycle delay may be currently active. It is safe and allowed to program pipe timing and DPLL registers. If this bit is not a zero it activates the register write protect and writes to those registers will be ignored unless the write protect key value is set in the panel sequencing control register. 1 In conjunction with bits Power Sequence Progress field and Power Cycle Delay Active this bit set to a one indicates that the panel is currently powered up or is currently in the power down sequence and it is unsafe to change the pipe timing and DPLL registers for the pipe that is assigned to the embedded panel output. If the embedded panel port is selected as the target for the panel control Software is responsible for enabling the LCD display by writing a 1 to the port enable bit only after all pipe timing DPLL registers are properly programmed and the PLL has locked to the reference signal. This bit is cleared set to 0 only after the panel power down sequencing is completed.
30	RO		**REQUIRE_ASSET_STATUS:** This bit indicates the status of programming of the display PLL and the selected display port. This a power on cycle will not be allowed unless this status indicates that the required assets are programmed and ready for use. 0 All required assets are not properly programmed. 1 All required assets are ready for the driving of a panel. The following conditions determine that the assets are ready 1 Display Pipe PLL Enabled and frequency locked bit 31 of DPLL Control Register for the pipe attached to the embedded panel port . 2 Display Pipe Enabled bit 31 of PIPECONF Pipe Configuration Register. For the pipe attached to the embedded panel port 3 Embedded Panel Port is Programmed Enabled
29:28	RO		**POWER_SEQUENCE_PROGRESS:** 00 Indicates that the panel is not in a power sequence 01 Indicates that the panel is in a power up sequence may include power cycle delay 10 Indicates that the panel is in a power down sequence 11 Reserved
27	RO		**POWER_CYCLE_DELAY_ACTIVE:** Power cycle delays occur after a panel power down sequence or after a hardware reset. On reset a power cycle delay will occur using the default value for the timing. 0 A power cycle delay is not currently active 1 A power cycle delay T4 is currently active
26:4	RO		**RESERVED0:**
3:0	RO		**INTERNAL_SEQUENCE_STATE:** 0000 Power Off Idle S0.0 0001 Power Off Wait for cycle delay S0.1 0010 Power Off S0.2 0011 Power Off S0.3 0100 Reserved 0101 Reserved 0110 Reserved 0111 Reserved 1000 Power On

Bit	Access	Default Value	Description
			Idle S1.0 1001 Power On S1.1 1010 Power On S1.2 1011 Power On Wait for cycle delay S1.3 1100 Reserved 1101 Reserved 1110 Reserved 1111 Reset

1.11.304 DISPLAY_CONTROLLER.RAMCLK_GATE_D

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//06210h
MMIO: Base/Offset: MMADR/06210h
IO: Base/Offset:

Description memory clock gating cpdmmreg.v gfxramcg2

Bit	Access	Default Value	Description
31	RW		**TVOUT_RAM_CLOCK_GATING_DISABLE:** 1 Disable RAM bank clock gating function
30	RW		**PANEL_FITTER_RAM_CLOCK_GATING_DISABLE:** 1 Disable RAM bank clock gating function
29	RW		**CURSOR_DATA_BUFFER_RAM_CLOCK_GATING_DISABLE:** 1 Disable RAM bank clock gating function
28	RW		**DEVCTG_DEVCDV_AUDM_UNIT_RAM_CLOCK_GATING_DISABLE:** DeBLC Reserved. DevCL WIZ Z coeff readback return FIFO Clock Gating Disable 1 Disable RAM bank clock gating function
27	RW		**DEVCTG_DPFC_UNIT_RAM_CLOCK_GATING_DISABLE:** DevBLC Reserved. DevCL Display Data Buffer2 Overlay Gating Disable 1 Disable RAM bank clock gating function
26	RW		**DISPLAY_DATA_BUFFER1_RAM_CLOCK_GATING_DISABLE:** 1 Disable RAM bank clock gating function
25	RW		**DEVBLC_DEVCTG_DEVCDV_HDCP_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL ME RAM Clock Gating Disable 1 Disable RAM bank clock gating function
24	RW		**DEVCTG_DEVCDV_DPIOM_UNIT_RAM_CLOCK_GATING_DISABLE:** DevBLC Reserved. DevCL WIZ polygon FIFO RAM Clock Gating Disable 1 Disable RAM bank clock gating function
23	RO		**DEVBLC_AND_DEVCTG_RESERVED0:** DevCL VF RAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
22	RO		**DEVBLC_AND_DEVCTG_RESERVED1:** DevCL SF RAMClock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
21	RO		**DEVBLC_AND_DEVCTG_RESERVED2:** DevCL WMIZ Latency FIFO Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
20	RO		**DEVBLC_AND_DEVCTG_RESERVED3:** DevCL TC FIFO Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.

Bit	Access	Default Value	Description
19	RO		**DEVBLC_DEVCTG_DEVCDV_RESERVED4:** DevCL SV FIFO Clock Gating Disable 1 Disable RAM bank clock gating function
18	RW		**DEVBLC_AND_DEVCTG_BD_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Latency FIFO Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
17	RW		**DEVBLC_AND_DEVCTG_BF_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL URB Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
16	RW		**DEVBLC_AND_DEVCTG_CS_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL L2 Instruction Tag RAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
15	RW		**DEVCTG_FH_UNIT_RAM_CLOCK_GATING_DISABLE:** DevBLC DevIntel Atom Processor D2000 series and N2000 Series Reserved. DevCL Data RAM Clock Gating Disable 1 Disable RAM bank clock gating function
14	RO		**DEVBLC_AND_DEVCTG_RESERVED5:** DevCL TAG RAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved
13	RO		**DEVBLC_AND_DEVCTG_RESERVED6:** DevCL L2 Instruction Cache Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
12	RO		**DEVBLC_AND_DEVCTG_RESERVED7:** DevCL MRFRAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
11	RW		**DEVBLC_AND_DEVCTG_VFM_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL GRF RAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel Atom Processor D2000 series and N2000 Series Reserved.
10	RW		**DEVBLC_AND_DEVCTG_SFM_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Data Cache CAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
9	RW		**DEVBLC_AND_DEVCTG_WIZM_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Data Cache Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
8	RW		**DEVBLC_AND_DEVCTG_URB_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Render Cache Latency FIFO Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
7	RW		**DEVBLC_AND_DEVCTG_IC_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Render PA Tag RAM Z Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
6	RW		**DEVBLC_AND_DEVCTG_ISC_UNIT_RAM_CLOCK_GATING_**

Bit	Access	Default Value	Description
			DISABLE: DevCL Render PA Tag RAM Color Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
5	RW		**DEVBLC_AND_DEVCTG_GA_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Render Cache Write Back FIFO Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
4	RW		**DEVBLC_AND_DEVCTG_MS_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Render Cache Z Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
3	RW		**DEVBLC_AND_DEVCTG_RCBP_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL Render Cache color Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
2	RW		**DEVBLC_AND_DEVCTG_RCC_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL L2 Mapping Cache CAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
1	RW		**DEVBLC_AND_DEVCTG_RCZ_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL L2 Mapping Tag RAM Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.
0	RW		**DEVBLC_AND_DEVCTG_MT_UNIT_RAM_CLOCK_GATING_DISABLE:** DevCL L2 Mapping Cache Clock Gating Disable 1 Disable RAM bank clock gating function DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved.

1.11.305 DISPLAY_CONTROLLER.RESERVED

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//301A0h
MMIO: Base/Offset: MMADR/301A0h
IO: Base/Offset:

This register value is mirrored from DDR in address 0h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:21	RO		**RESERVED0:** MBZ
20:16	RO		**RESERVED1:** The fast scale factors must be set so that the output of the fast scalar has a luminance to chrominance ratio of either 2 1 or 1 1. The original source format and the two fast scale factors determine that ratio. 0000 No fast horizontal scaling only precision NNNN Down scale by 2 N N 1 5 for 3 line Vertical filter N 1 6 for 2 line Vertical filter
15:5	RO		**RESERVED2:** MBZ

Bit	Access	Default Value	Description
4:0	RO		**RESERVED3:** 0000 No fast horizontal scaling only precision NNNN Down scale by 2 N N 1 5 for 3 line Vertical filter N 1 6 for 2 line Vertical filter

1.11.306 DISPLAY_CONTROLLER.RESERVED_USED_TO_BE_AUTO_SCALING_RATIOS_READBACK

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61238h
MMIO: Base/Offset: MMADR/61238h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO		**RESERVED0:**

1.11.307 DISPLAY_CONTROLLER.RESERVED_USED_TO_BE_SCALING_INITIAL_PHASE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6123Ch
MMIO: Base/Offset: MMADR/6123Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO		**RESERVED0:**

1.11.308 DISPLAY_CONTROLLER.SCHRKEN

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30160h
MMIO: Base/Offset: MMADR/30160h
IO: Base/Offset:

This register value is mirrored from DDR in address 60h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:** MBZ
26:24	RW		**SOURCE_CHROMA_KEY_ENABLE:** Each bit enables one channel of source chroma key range comparison. If the bit is a one the comparison result is used otherwise it is ignored. Bit 26 Enables Y Green Comparison 23 16 Bit 25 Enables U Blue Comparison 15 8 Bit 24 Enables V Red Comparison 7 0
23:8	RO		**RESERVED1:** MBZ
7:0	RO		**OVERLAY_CONSTANT_ALPHA_VALUE:** This field provides the alpha value when constant alpha is enabled.

Bit	Access	Default Value	Description
			A value of FF means fully opaque and a value of zero means fully transparent. Values in between those values allow for a blending of overlay with other surfaces.

1.11.309 DISPLAY_CONTROLLER.SCHRKVH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30158h
MMIO: Base/Offset: MMADR/30158h
IO: Base/Offset:

This register value is mirrored from DDR in address 58h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**Y_GREEN_SOURCE_KEY_HIGH:** This 8 bit field specifies the high end Y Green value less than or equal to for the overlay source exclusion pixel data. When the corresponding Y Green Source Key Mask Enables bit in SCLRKM register is set an overlay value greater than this field fails the comparison and the overlay pixel passes. Otherwise the overlay pixel becomes transparent. YUV format Y value in 0 255 range. RGB format Green value in 0 255 range.
15:8	RW		**U_BLUE_SOURCE_KEY_HIGH:** This field specifies the high end U Blue value less than or equal to for the overlay source exclusion pixel data. When the corresponding U Blue Source Key Mask Enables bit in SCLRKM register is set an overlay value greater than this field fails the comparison and the overlay pixel passes. Otherwise the overlay pixel becomes transparent. YUV format U value in excess 128 format. RGB format Blue value in 0 255 range.
7:0	RW		**V_RED_SOURCE_KEY_HIGH:** This field specifies the high end V Red value less than or equal to for the overlay source exclusion pixel data. When the corresponding V Red Source Key Mask Enables bit in SCLRKM register is set an overlay value greater than this field fails the comparison and the overlay pixel passes. Otherwise the overlay pixel becomes transparent. YUV format V value in excess 128 format. RGB format Red value in 0 255 range.

1.11.310 DISPLAY_CONTROLLER.SCHRKVL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3015Ch
MMIO: Base/Offset: MMADR/3015Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 5Ch R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:16	RW		**Y_GREEN_SOURCE_KEY_LOW:** This field specifies the low end Y Green value greater than or equal to for the overlay source exclusion pixel data. When the corresponding Y Green Source Key Mask Enables bit in SCLRKM register is set an overlay value less than this field fails the comparison and the overlay pixel passes. Otherwise the overlay pixel becomes transparent. YUV format Y value in 0 255 range. RGB format Green value in 0 255 range.
15:8	RW		**U_BLUE_SOURCE_KEY_LOW:** This field specifies the low end U Blue value greater than or equal to for the overlay source exclusion pixel data. When the corresponding U Blue Source Key Mask Enables bit in SCLRKM register is set an overlay value less than this field fails the comparison and the overlay pixel passes. Otherwise the overlay pixel becomes transparent. YUV format U value in excess 128 format. RGB format Blue value in 0 255 range.
7:0	RW		**V_RED_SOURCE_KEY_LOW:** This field specifies the low end V Red value greater than or equal to for the overlay source exclusion pixel data. When the corresponding V Red Source Key Mask Enables bit in SCLRKM register is set an overlay value less than this field fails the comparison and the overlay pixel passes. Otherwise the overlay pixel becomes transparent. YUV format V value in excess 128 format. RGB format Red value in 0 255 range.

1.11.311 DISPLAY_CONTROLLER.SDVO_DP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61150h
MMIO: Base/Offset: MMADR/61150h
IO: Base/Offset:

Description DFT DPIO and AUX control dprrega.v sdvo_dftQ

Bit	Access	Default Value	Description
31	RW		**SDVO_DPB_TEST_MODE_ENABLE:** Enables Test mode for sDVO DPB logic in the PCI Express AFE. Enables mode for the sDVO DPB port only. 1 Test mode Enabled. 0 Test mode Disabled. Default
30	RW		**DEVCTG_SDVO_DPB_TEST_MODE_CHECK_ENABLE:** 1 Enable checking of Test mode data 0 Disable Check DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
29	RW		**SDVO_DPB_PATTERN_SELECT:** 1 1010101010 0 0101010101
28	RW		**SDVO_DPC_TEST_MODE_ENABLE:** Enables Test mode for sDVO DP logic in the PCI Express AFE. Enables mode for sDVO DPC only. 1 Test mode Enabled. 0 Test mode Disabled. Default
27	RW		**DEVCTG_SDVO_DPC_TEST_MODE_CHECK_ENABLE:** 1

Bit	Access	Default Value	Description
			Enable checking of Test mode data 0 Disable Check DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
26	RW		**SDVO_DPC_PATTERN_SELECT:** 1 1010101010 0 0101010101
25	RW		**DEVCDV_DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DP_DC_BALANCE_SET:** 1 DC Balance circuitry will be reset on every frame with Vsynch 0 DC Balance circuitry does not get reset on every frame.
24	RW		**DEVCDV_DEVCTG_DPB_AUX_FULL_TEST_ENABLE:** Enables test for the DPB AUX core logic transmit and receive functions through the DPB AUX and DPC AUX buffers. DPB AUX and DPC AUX are interconnected through I O buffer loopbacks. DPB AUX is programmed as source to output a 20 byte test pattern. DPC AUX is programmed as sink to receive the test pattern and reply with a different 20 byte test pattern. Test pattern 2 0X183C7EE7 C381FF7F 3F1F0F07 030100EE 77CC33A5 Programming sequence 1. Set DPB AUX Full Test Enable to 1. 2. Program DPB_AUX_CH_DATA 1 5 with test pattern 1 to transmit as the source. 3. Program DPC_AUX_CH_DATA 1 5 with test pattern 2 to reply with as the sink. 4. Program all DPC_AUX_CH_CTL fields and set Send to 1. 5. Program all DPB_AUX_CH_CTL fields and set Send to 1. Then the test will start. Results checking sequence 1. Poll DPB_AUX_CH_CTL for Done. To pass Done must be set within 500us. 2. Read DPB_AUX_CH_CTL register. To pass Timeout Error and Receive Error must be 0. 3. Read DPC_AUX_CH_CTL register. To pass Receive Error must be 0. 4. Read DPB_AUX_CH_DATA 1 5 registers. To pass they must contain test pattern 2. 5. Read DPC_AUX_CH_DATA 1 5 registers. To pass they must contain test pattern 1. Clear this bit to 0 after test is done to return DP AUX to normal operation. Test must be repeated with and without lane reversal to verify DPB AUX buffer combinations. Only enable one DP AUX Full Test at a time To abort a test in progress write the AUX_CH_CTL Send bits to 0 and Full Test Enable to 0. 1 Enable test. 0 Test disabled. Default
23	RW		**DEVCTG_DPC_AUX_FULL_TEST_ENABLE:** See DPB AUX Full Test Enable description. DPC AUX is source and DPD AUX is sink. 1 Enable test. 0 Test disabled. Default DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
22	RW		**DEVCTG_DPD_AUX_FULL_TEST_ENABLE:** See DPB AUX Full Test Enable description. DPD AUX is source and DPB AUX is sink. 1 Enable test. 0 Test disabled. Default DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
21	RW		**DEVCDV_DEVCTG_DPB_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** Enables test for the DPB AUX I O buffer. A 16 cycle clock pattern is output to the I O buffer and compared against the looped back buffer output. The input clock is cdclk for DevCTG A hrawclk for Intel® Atom™ Processor D2000 series and N2000 Series DevCTG B . With input clock at 512MHz the pattern will be 1 MHz clock. It scales down with lower clock frequencies. The result is found in DPB AUX Buffer Loopback Test Result after DPB AUX Buffer Loopback Test Done is set. Clear this bit to 0 after test is done to return DP AUX to normal

Bit	Access	Default Value	Description
			operation. Loopback Test can be run simultaneously on all AUX buffers. Do not enable DP AUX Buffer Loopback Test and DP AUX Full Test simultaneously. Test must be repeated with and without lane reversal to verify DPB AUX buffer combinations. 1 Enable test. 0 Test disabled. Default
20	RW		**DEVCDV_DEVCTG_DPC_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** See DPB AUX Buffer Loopback Test Enable description. 1 Enable test. 0 Test disabled. Default
19	RW		**DEVCTG_DPD_AUX_BUFFER_LOOPBACK_TEST_ENABLE:** See DPB AUX Buffer Loopback Test Enable description. 1 Enable test. 0 Test disabled. Default DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
18:14	RO		**RESERVED0:**
13	RO		**DEVCDV_DEVCTG_DPB_AUX_BUFFER_LOOPBACK_TEST_DONE:** DPB AUX Buffer Loopback Test has been run and completed. This is not the done for the DPB AUX Full Test. 1 Test done. DPB AUX Buffer Loopback Test Result is now valid. 0 Test not done. DPB AUX Buffer Loopback Test Result is not valid.
12	RO		**DEVCDV_DEVCTG_DPC_AUX_BUFFER_LOOPBACK_TEST_DONE:** See DPB AUX Buffer Loopback Test Done description 1 Test done 0 Test not done
11	RO		**DEVCTG_DPD_AUX_BUFFER_LOOPBACK_TEST_DONE:** See DPB AUX Buffer Loopback Test Done description 1 Test done 0 Test not done DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
10	RO		**DEVCDV_DEVCTG_DPB_AUX_BUFFER_LOOPBACK_TEST_RESULT:** Result of the DPB AUX Buffer Loopback Test. Value is only valid after a DPB AUX Loopback Test Done is 1. This is not the result of the DPB AUX Full Test. 1 quote Fail quote 0 quote Pass quote
9	RO		**DEVCDV_DEVCTG_DPC_AUX_BUFFER_LOOPBACK_TEST_RESULT:** See DPB AUX Buffer Loopback Test Result description 1 quote Fail quote 0 quote Pass quote
8	RO		**DEVCTG_DPD_AUX_BUFFER_LOOPBACK_TEST_RESULT:** See DPB AUX Buffer Loopback Test Result description 1 quote Fail quote 0 quote Pass quote DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
7	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPC_CLOCK_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
6	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPC_BLUE_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
5	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPC_GREEN_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
4	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPC_RED_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000

Bit	Access	Default Value	Description
			series and N2000 Series Reserved
3	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPB_CLOCK_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
2	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPB_BLUETEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
1	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPB_GREEN_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
0	RO		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVO_DPB_RED_TEST_RESULT:** 1 Fail 0 Pass DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved

1.11.312 DISPLAY_CONTROLLER.SDVO_DP2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61154h
MMIO: Base/Offset: MMADR/61154h
IO: Base/Offset:

Description DFT DPT control dprrega.v dpr_dpt_dft2_i

Bit	Access	Default Value	Description
31:10	RO		**RESERVED0:** MBZ
9	RW		**PORTC_AUX_LEAKAGE_ENABLE_DEVCDV:**
8	RW		**PORTB_AUX_LEAKAGE_ENABLE_DEVCDV:**
7	RW		**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_PIPE_B_DEVCTG:** DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
6	RW		**TEST_PATTERN_8_BIT_PROGRAMMED_INPUT_ON_PIPE_A_DEVCTG:** DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
5	RW		**SCRAMBLED_0S_ON_PIPE_B:**
4	RW		**SCRAMBLED_0S_ON_PIPE_A:**
3	RW		**PRBS7_TEST_PATTERN_ON_PIPE_B:**
2	RW		**PRBS7_TEST_PATTERN_ON_PIPE_A:**
1	RW		**TEST_MODE_SCRAMBLE_1S_A_FRAME_ON_PIPE_B:**
0	RW		**TEST_MODE_SCRAMBLE_1S_A_FRAME_ON_PIPE_A:**

1.11.313 DISPLAY_CONTROLLER.SDVO_HDMIB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61140h
MMIO: Base/Offset: MMADR/61140h

IO: Base/Offset:

Description HDMIB port control dprrega.v sdvo_bQ Note This Digital Display Port defaults to sDVO port functionality when it is not programmed as a HDMI port. The operating mode of the port is determined by the setting of the encoding register field bits 11 10.

Bit	Access	Default Value	Description
31	RW		**SDVO_HDMIB_ENABLE:** Disabling this port will put it in its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. This port must not be enabled simultaneously with DisplayPort B. 1 Enable. This bit enables the Digital Display Port B interface for HDMI or SDVO modes. 0 Disable and tristates the Digital Display Port B interface for HDMI or SDVO modes.
30	RW		**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 Pipe A 1 Pipe B
29	RW		**DEVCTG_DEVBW_DEVCL_DEVBLC_STALL_SELECT:** This bit selects stall for external scaling functionality only on SDVO. Programming notes It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 Stall input signal is unused on this port 1 Stall input signal is used to stall the pipe attached to this port DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
28:26	RW		**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 8 bits per color Default x3 mode 001 RESERVED for 10 bits per color 010 RESERVED for 6 bits per color 011 RESERVED 1xx RESERVED
25:19	RO		**RESERVED0:**
18	RW		**SDVO_HDMIB_CLOCK_OUTPUT_INVERSION:** Please note that this applies to all modes and is instantly updated. 1 sDVO HDMIB Clock output is inverted 0 sDVO HDMIB Clock output is NOT inverted DEFAULT
17:16	RW		**DEVCDV_DEVCTG_DEVCL_SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external UDI link. 10 90 cycle has been measured to have 13dB EMI improvement over a 50 50 duty cycle. 00 Default 50 50 duty cycle Clock output is 0000011111 01 10 90 duty cycle Clock output is 0111111111 followed by 0000000001 10 20 80 duty cycle Clock output is 0011111111 followed by 0000000011 11 Reserved

Bit	Access	Default Value	Description
15	RW		**DEVBW_DEVCL_DEVBLC_PORT_LANE_REVERSAL:** This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place on the Vblank after being written. It is an OEM configurable feature. 0 Default Not reversed 1 Reversed DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
14	RO		**RESERVED1:**
13	RW		**DEVBW_DEVCL_DEVBLC_CLOCK_OUTPUT_DISABLE:** This bit disables the clock output on the digital output port. For 8b 10b modes the clock output should be disabled. 0 Default Clock output enabled 1 Clock output disabled DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
12	RW		**DEVBW_DEVCL_DEVBLC_DEVCDV_SCRAMBLING_ENABLE:** This bit enables scrambling for UDI related modes using ANSI 8b 10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 Scrambling disabled Default 1 Scrambling enabled
11:10	RW		**DEVCDV_DEVCTG_DEVCL_ENCODING:** 00 SDVO encoding. Default. In this mode the SDVOB hotplug input pin pair is used to generate hotplug. 01 RESERVED 10 TMDS encoding DevCL DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series external link and HDMI only See the HDMI specification for control codes. In this mode the external HPD pin is used to generate hotplug. In fixed frequency mode start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 Reserved
9	RW		**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet 32 bytes of a value of 0 to be sent when Vsync 1 on this port required for HDMI operation. It also enables preambles and guardbands prior to the null packets in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 Disable null infoframe packets when Vsync 1 on this port. Default 1 Enable null infoframe packets when Vsync 1 on this port.
8	RW		**DEVCDV_DEVCTG_DEVCL_COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 Apply full 0 255 color range to the output Default 1 Apply 16 235 color range to the output
7	RW		**DEVCTG_DEVBW_DEVCL_DEVBLC_SDVOB_BORDER_ENABLE:** This bit determines if the border data from native VGA or the timing generator is to be considered valid pixel data at the external component. 1 Border to the sDVOB encoder is enabled. Blank is used to generate the DE output used in all cases except when the external scaler is used in a DVI panel over SDVO . 0 Border to the sDVOB encoder is disabled. DE Display Enable is used DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
6	RW		**DEVCDV_DEVCTG_DEVCL_AUDIO_OUTPUT_ENABLE:**

Bit	Access	Default Value	Description
			This bit directs audio to this port. When enabled and audio data is available the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. Programming note Audio can only be enabled on one port at a time in x3 mode with TMDS encoding. If audio is enabled on both ports B and C audio will be disabled. 0 Default No audio output on this port 1 Enable audio on this port
5	RW		**DEVCDV_DEVCTG_DEVCL_HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own but must be used in conjunction with HDCP registers. Programming note HDCP can only be selected on one port at a time. If both ports are selected encryption will be disabled. 0 Default No HDCP encryption on this port 1 Enable HDCP on this port
4:3	RW		**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC BLANK SYNC and standard polarity is transmitted as BLANK SYNC BLANK. For example if Vsync is not inverted and Hsync is inverted an Hsync period transmitted during Vsync would be transmitted as BLANK VS HS BLANK VS BLANK VS HS. Please note that in native VGA modes these bits have no effect. In native VGA modes sync polarity is determined by VRshr3c2d76b 7 6 the VGA polarity bits in VGA control. 00 VS and HS are active low inverted 01 VS is active low inverted HS is active high 10 VS is active high HS is active low inverted 11 Default VS and HS are active high
2	RW		**DIGITAL_PORT_B_DETECTED:** Read only bit indicating whether a digital port B was detected during initialization. It signifies the level of the GMBUS port 4 sDVO B C data line at boot. This bit is valid regardless of whether the port is enabled. 0 Digital Port B not detected during initialization 1 Digital Port B detected during initialization
1:0	RO		**RESERVED2:** MBZ

1.11.314 DISPLAY_CONTROLLER.SDVO_HDMIC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61160h
MMIO: Base/Offset: MMADR/61160h
IO: Base/Offset:

Description HDMIC port control dprrega.v sdvo_cQ Note This Digital Display Port defaults to sDVO port functionality when it is not programmed as a HDMI port. The operating mode of the port is determined by the setting of the encoding register field bits 11 10.

Bit	Access	Default Value	Description
31	RW		**SDVO_HDMIC_ENABLE:** Disabling this port will put it in

Bit	Access	Default Value	Description
			its lowest power state. Port enable takes place on the Vblank after being written. Both this bit and bit 6 of this register must be enabled to send audio over this port. This port must not be enabled simultaneously with DisplayPort C. 1 Enable. This bit enables the Digital Display Port C interface for HDMI or SDVO modes. 0 Disable and tristates the Digital Display Port C interface for HDMI or SDVO modes.
30	RW		**PIPE_SELECT:** This bit determines from which display pipe the source data will originate. This only applies to devices with dual display pipes. Pipe selection takes place on the Vblank after being written 0 Pipe A 1 Pipe B
29	RW		**STALL_SELECT:** This bit selects stall for external scaling functionality only on SDVO. Programming notes It is only valid to have a single stall indication to a particular pipe. In cases where two ports are being driven from a single pipe one of the ports must set this bit to 0. Only sDVOB or sDVOC can select the stall function as only a single stall input is available between the two interfaces. Set the stall input to unused before programming the external device creating the stall. 0 Stall input signal is unused on this port 1 Stall input signal is used to stall the pipe attached to this port DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
28:26	RW		**COLOR_FORMAT:** This field selects the number of bits per color sent to a receiver device connected to this port. Color format takes place on the Vblank after being written. Color format change must be done as a part of mode set since different color depths require different pixel clock settings. Selecting a pixel color depth higher or lower than the pixel color depth of the frame buffer results in dithering the output stream. 000 8 bits per color Default 001 RESERVED for 10 bits per color 010 RESERVED for 6 bits per color 011 RESERVED 1xx RESERVED
25:19	RO		**RESERVED0:**
18	RW		**SDVO_HDMIC_CLOCK_OUTPUT_INVERSION:** Please note that this applies to all modes and is instantly updated. 1 sDVO HDMIB Clock output is inverted 0 sDVO HDMIB Clock output is NOT inverted DEFAULT
17:16	RW		**SYMBOL_CLOCK_DUTY_CYCLE:** These bits control the output clock duty cycle to enable EMI mitigation on the external HDMI link. 10 90 cycle has been measured to have 13dB EMI improvement over a 50 50 duty cycle. 00 Default 50 50 duty cycle Clock output is 0000011111 01 10 90 duty cycle Clock output is 0111111111 followed by 0000000001 DevCL DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series HDMI only 10 20 80 duty cycle Clock output is 0011111111 followed by 0000000011 DevCL DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series HDMI only 11 Reserved
15	RW		**PORT_LANE_REVERSAL:** This bit reverses the order of the 4 lanes within the port. Port lane reversal takes place

Bit	Access	Default Value	Description
			on the Vblank after being written. It is an OEM configurable feature. 0 Default Not reversed 1 Reversed DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
14	RO		**RESERVED1:**
13	RW		**CLOCK_OUTPUT_DISABLE:** This bit disables the clock output on the digital output port. For 8b 10b modes the clock output should be disabled. 0 Default Clock output enabled 1 Clock output disabled DevCL only DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series Reserved
12	RW		**SCRAMBLING_ENABLE:** This bit enables scrambling for UDI related modes using ANSI 8b 10b or TMDS encoding. It is not used with SDVO encoding. Software must set this bit appropriately when enabling the port. Scrambling is reset at the beginning of horizontal sync. 0 Scrambling disabled Default 1 Scrambling enabled DevCL only
11:10	RW		**ENCODING:** These bits select among encoding types. It is set as part of the display detection process. Control codes for ANSI 8b 10b and TMDS encoding must be programmed using these bits. Please note that ANSI 8b 10b and TMDS encoding can only be enabled on one port at a time as only one HPD pin is available for use between ports B and C. 00 SDVO encoding. In this mode the SDVOB hotplug input pin pair is used to generate hotplug. 01 RESERVED 10 TMDS encoding DevCL DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series external link and HDMI only See the HDMI specification for control codes. In this mode the external HPD pin is used to generate hotplug. In fixed frequency mode start of fill and end of fill values for TMDS must be programmed using register 6114C. 11 Reserved
9	RW		**NULL_PACKETS_ENABLED_DURING_VSYNC:** This bit enables a null packet 32 bytes of a value of 0 to be sent when Vsync 1 on this port required for HDMI operation. It also enables preambles and guardbands prior to the null packets in accordance with the HDMI specification. It is only valid for modes that use TMDS encoding. 0 Disable null infoframe packets when Vsync 1 on this port. Default 1 Enable null infoframe packets when Vsync 1 on this port.
8	RW		**COLOR_RANGE_SELECT:** This bit is used to select the color range of RBG outputs in HDMI mode. It is only valid when using TMDS encoding and 8 bit per color mode. 0 Apply full 0 255 color range to the output Default 1 Apply 16 235 color range to the output DevCL and DevCTG only
7	RW		**SDVOC_BORDER_ENABLE:** This bit determines if the border data from native VGA or the timing generator is to be considered valid pixel data at the external component. 1 Border to the sDVOC encoder is enabled. Blank is used to generate the DE output used in all cases except when the external scaler is used in a DVI panel over SDVO . 0 Border to the sDVOC encoder is disabled. DE Display

Bit	Access	Default Value	Description
			Enable is used
6	RW		**AUDIO_OUTPUT_ENABLE:** This bit directs audio to this port. When enabled and audio data is available the audio data will be combined with the video data and sent over this port. The audio unit uses the status of this bit to indicate presence of the HDMI output to the audio driver. Programming note Audio can only be enabled on one port at a time in x3 mode with TMDS encoding. If audio is enabled on both ports B and C audio will be disabled. 0 Default No audio output on this port 1 Enable audio on this port DevCL DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series only
5	RW		**HDCP_PORT_SELECT:** This bit directs HDCP to this port. When enabled the information sent on this port will be encrypted using HDCP. Please note that this bit does not enable encryption on its own but must be used in conjunction with HDCP registers. Programming note HDCP can only be selected on one port at a time. If both ports are selected encryption will be disabled. 0 Default No HDCP encryption on this port 1 Enable HDCP on this port DevCL DevCTG DevIntel® Atom™ Processor D2000 series and N2000 Series only
4:3	RW		**SYNC_POLARITY:** Please note that sync polarity does not apply to ANSI coding. Indicates the polarity of Hsync and Vsync. Inverted polarity is transmitted as SYNC BLANK SYNC and standard polarity is transmitted as BLANK SYNC BLANK. For example if Vsync is not inverted and Hsync is inverted an Hsync period transmitted during Vsync would be transmitted as BLANK VS HS BLANK VS BLANK VS HS. Please note that in native VGA modes these bits have no effect. In native VGA modes sync polarity is determined by VRshr3c2d76b 7 6 the VGA polarity bits in VGA control. 00 VS and HS are active low inverted 01 VS is active low inverted HS is active high 10 VS is active high HS is active low inverted 11 Default VS and HS are active high
2	RW		**DIGITAL_PORT_C_DETECTED:** Read only bit indicating whether a digital port C was detected during initialization. It signifies the level of the GMBUS port 3 port C data line at boot. This bit is valid regardless of whether the port is enabled. 0 Digital Port C not detected during initialization 1 Digital Port C detected during initialization default
1:0	RO		**RESERVED2:** MBZ

1.11.315 DISPLAY_CONTROLLER.SHEIGHT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3013Ch
MMIO: Base/Offset: MMADR/3013Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 3Ch R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:26	RO		**RESERVED0:** MBZ
25:16	RO		**UV_SOURCE_HEIGHT:** The number of lines contained in a single planar UV source data. In packed formats this is unused. For planar YUV formats it indicates the number of lines starting at and including the base address line contained in the UV source data. When the last line is reached and the complete destination window has not been filled this line will be repeated until the end of the destination window. The maximum UV height is 1023 lines. The minimum height is the number of vertical taps being used times the vertical chroma subsampling ratio. Height should include the line contributing to the interpolation of the last display overlay line.
15:11	RO		**RESERVED1:** MBZ
10:0	RO		**Y_RGB_SOURCE_HEIGHT:** In packed formats this indicates the number of lines starting at and including the base address line contained in the source data. In planar formats it is the number of Y lines. This is used to determine where the end of the source is in the vertical direction to handle the edge effects related to the vertical filter. When the last line is reached and the complete destination window has not been filled this line will be repeated until the end of the destination window. The maximum height is 2047 lines. The minimum height is the number of vertical taps currently being used. A height must not be specified for lines that are completely not on the active display. Height should include the line contributing to the interpolation of the last display overlay line.

1.11.316 DISPLAY_CONTROLLER.SWFXX

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//00 70410h
MMIO: Base/Offset: MMADR/00 70410h
IO: Base/Offset:

These 32 bit registers are used as scratch pad data storage space and have no direct effect on hardware operation. The use of these registers is defined by the software architecture.

Bit	Access	Default Value	Description
31:0	RO		**RESERVED_0:**

1.11.317 DISPLAY_CONTROLLER.SWIDTH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30134h
MMIO: Base/Offset: MMADR/30134h
IO: Base/Offset:

This register value is mirrored from DDR in address 34h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:** MBZ
26:16	RO		**UV_PIXEL_SOURCE_WIDTH:** The number of valid pixels contained in a single line of planar UV source data. This field is unused in packed modes. For planar modes it s used for the U and V source width. The width for U and V sources is required to be the same. When the last pixel is reached and the complete destination window has not been filled this pixel will be repeated until the end of the destination window. When displaying planar YUV 4 2 0 data this field contains the number of U pixels same as the number of V pixels which should be one half of the Y pixels. When displaying planar YUV 4 1 0 planar data this field contains the number of U pixels same as the number of V pixels which should be one quarter of the Y pixels. The UV source width cannot be more than half the Y source width. Source formats with a Y UV ratio of less than 2 1 such as YUV 4 4 4 with a ratio of 1 1 are not supported.
15:12	RO		**RESERVED1:** MBZ
11:0	RO		**Y_RGB_PIXEL_SOURCE_WIDTH:** The number of valid pixels contained in a single line of source data. In both planar and packed modes this is the Y source width. This field should include all contributing pixel data. When the last pixel is reached and the complete destination window has not been filled this pixel will be repeated until the end of the destination window. For source formats of YUV 4 1 0 data the atomic unit is four pixels For source formats of YUV 4 2 2 or YUV 4 2 0 data the atomic unit is two pixels The starting offset within the buffer must reflect these restrictions.

1.11.318 DISPLAY_CONTROLLER.SWIDTHSW

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30138h
MMIO: Base/Offset: MMADR/30138h
IO: Base/Offset:

This register value is mirrored from DDR in address 38h R W . Hardware uses values in this register to determine the number of SWORDs 32 bytes to be fetched from the memory for each overlay source scan line. The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:24	RO		**RESERVED0:** MBZ
23:18	WO		**UV_SOURCE_SWORD_WIDTH:** This field sets the number of aligned SWords that contains all source U V pixels in a single line of planar U V source data. This field is valid only in planar modes. Minimum size is 1 SWORD. Overlay hardware uses this field to make memory request for each scan line in the planar U V source buffers. In normal overlay horizontal display order left to right software should calculate this field based on the pixel aligned buffer pointer UVAddress and the pixel aligned source window width UVSWidth by UVSWidthSW

Bit	Access	Default Value	Description
			UVAddress UVSWidth 0x3F gt gt 6 UVAddress gt gt 6 lt lt 1 1 In mirrored overlay horizontal display order for right to left software should use UVSWidthSW UVAddress gt gt 6 UVAddress UVSWidth 0x3F gt gt 6 lt lt 1 1
17:9	RO		**RESERVED1:** MBZ
8:2	WO		**Y_RGB_SOURCE_SWORD_WIDTH:** This field sets the number of aligned SWords that contains all source Y RGB pixels in a single source line. In planar modes this is the Y source SWORD width. Minimum size is 1 SWORD. Overlay hardware uses this field to make memory request for each source scan line. In normal overlay horizontal display order left to right software should calculate this field based on the pixel aligned buffer pointer YAddress and the pixel aligned source window width YSWidth by In mirrored overlay horizontal display order for right to left software should use
1:0	RO		**RESERVED2:** MBZ

1.11.319 DISPLAY_CONTROLLER.UVSCALE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30144h
MMIO: Base/Offset: MMADR/30144h
IO: Base/Offset:

This register value is mirrored from DDR in address 44h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:20	RO		**UV_VERTICAL_SCALE_FRACTION:** This is a fractional positive number that represents the scale factor to be used in vertical scaling for UV components. This field represents a value range from 0 to 1 0 Vertical Scale Fraction lt 1 . Defining a Ver_Scale Factor as the ratio of source height over destination height. Ver_Scale_Factor Source Image Height Destination Height For up scaling UV Vertical Scale Fraction is Ver_Scale_Factor which is a fractional number. For downscaling UV Vertical Scale Fraction is the fractional portion of Ver_Scale_Factor. The integer portion is in UV Vertical Downscale Integer field. . For devices with integrated panel fitting the single line mode requires that the vertical scale factor be determined by the panel height instead of the display mode s source height.
19	RO		**RESERVED0:** MBZ
18:16	RO		**UV_HORIZONTAL_DOWNSCALE_FACTOR_INTEGER:**
15	RO		**RESERVED1:** MBZ
14:3	RO		**UV_HORIZONTAL_SCALE_FRACTION:** This is a fractional positive number that represents the scale factor to be used in horizontal scaling for UV components. This field represents a value range from 0 to 1 0 lt Hor Scale

Bit	Access	Default Value	Description
			Fraction It 1 . Defining a Hor_Scale Factor as the ratio of source width over destination width Hor_Scale_Factor Source Width Destination Width For up scaling UV Horizontal Scale Fraction is Hor_Scale_Factor which is a fractional number. For downscaling UV Horizontal Scale Fraction is the fractional portion of Hor_Scale_Factor. The integer portion is in UV Horizontal Downscale Integer field.
2:0	RO		**RESERVED2:** MBZ

1.11.320 DISPLAY_CONTROLLER.UVSCALEV

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//301A4h
MMIO: Base/Offset: MMADR/301A4h
IO: Base/Offset:

This register value is mirrored from DDR in address 4h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:27	RO		**RESERVED0:** MBZ
26:16	RO		**Y_VERTICAL_SCALE_INTEGER:** This field is used for vertical downscale. It specifies the integer portion of the scale factor for packed data or the Y data in planar modes. A zero in this field indicates a vertical upscale operation.
15:11	RO		**RESERVED1:** MBZ
10:0	RO		**UV_VERTICAL_SCALE_INTEGER:** Used only in YUV planar modes. This field is used only for vertical downscale. It specifies the integer portion of the scale factor for U V data. The chrominance data may be subsampled. A zero value specifies a vertical upscale operation.

1.11.321 DISPLAY_CONTROLLER.UV_HCOEFS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30700h
MMIO: Base/Offset: MMADR/30700h
IO: Base/Offset:

This register value is mirrored from DDR in address 600h R W . The memory Address Offset in DDR is Read Write. The offset is 600h 6FFh.

Bit	Access	Default Value	Description
31	RO		**SIGN2:** 0 Positive value 1 Negative value
30:28	RO		**EXPONENT2:** 000 b.bbbbbb 1.6 001 .bbbbbbb 0.7 010 .0bbbbbbb 0.8 011 .00bbbbbbb 0.9 1xx Reserved

27:21	RO		**MANTISSA2:** The mantissa varies in size based on which filter and which tap is being specified. Vertical filters use 6 bits except Y center tap is 8 bits Horizontal filters use 7 bits except Y UV center taps are 9 bits
20:16	RO		**RESERVED0:** MBZ
15	RO		**SIGN:** 0 Positive value 1 Negative value
14:12	RO		**EXPONENT:** This field determines the placement of the binary point for each coefficient. Using the value of 000 the coefficient has a maximum value of just less than two. 000 1.6 001 0.7 010 0.8 011 0.9 1xx Reserved
11:5	RO		**MANTISSA:**
4:0	RO		**RESERVED1:** MBZ

1.11.322 DISPLAY_CONTROLLER.UV_VCOEFS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30600h
MMIO: Base/Offset: MMADR/30600h
IO: Base/Offset:

This register value is mirrored from DDR in address 500h R W . The memory Address Offset in DDR is Read Write. The offset is 500h 5FFh

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_UV_VERTICAL_FILTER_COEFFICIENT:**

1.11.323 DISPLAY_CONTROLLER.UV_VPH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30120h
MMIO: Base/Offset: MMADR/30120h
IO: Base/Offset:

This register value is mirrored from DDR in address 20h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:20	RO		**UV_VERTICAL_PHASE_FOR_FIELD_1:** This fractional value is only used in YUV planar formats where the UV plane may have a different vertical initial phase from the Y data. When the overlay buffers are in Interleaved buffer format this value sets the initial vertical phase for field 1 in all UV data buffers. When the overlay buffers are in Non Interleaved format this value is intended for buffers containing field 1 data. The value applies to a particular UV data buffer.
19:16	RO		**RESERVED0:** Software should set all the 16 bits for forward compatibility in case more accurate DDA phase is implemented.
15:4	RO		**UV_VERTICAL_PHASE_FOR_FIELD_0:** This fractional

Bit	Access	Default Value	Description
			value is only used in YUV planar formats where the UV plane may have a different vertical initial phase from the Y data. When the overlay buffers are in Interleave buffer format this value sets the initial vertical phase for field 0 in all UV data buffers. When the overlay buffers are in Non Interleaved format this value is intended for buffers containing field 0 data. The value applies to a particular UV data buffer.
3:0	RO		**RESERVED1:** Software should set all the 16 bits for forward compatibility in case more accurate DDA phase is implemented.

1.11.324 DISPLAY_CONTROLLER.VBLANK_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60010h
MMIO: Base/Offset: MMADR/60010h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Read Only.
28:16	RW		**PIPE_A_VERTICAL_BLANK_END:** This 13 bit field specifies the Vertical Blank End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VBLANK End line position where the first active line is considered line 0 the second active line is considered line 1 etc. The end of vertical blank should be after the start of vertical blank and before or equal to the vertical total. This register should be loaded with the Vactive BottomBorder VBlank 1. For interlaced display modes hardware automatically divides this number by 2 to get the vertical blank end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	RO		**RESERVED1:** Read Only.
12:0	RW		**PIPE_A_VERTICAL_BLANK_START:** This 13 bit field specifies the Vertical Blank Start expressed in terms of the absolute line number relative to the vertical active display start. The value programmed should be the VBLANK Start line position where the first active line is considered line 0 the second active line is considered line 1 etc. Minimum vertical blank size is required to be at least three lines. Blank should start after the end of active. This register is loaded with the Vactive BottomBorder 1. For interlaced display modes hardware automatically divides this number by 2 to get the vertical blank start in each field. It does not count the two half lines that get added when operating in modes with half lines.

1.11.325 DISPLAY_CONTROLLER.VBLANK_BPIPE_BVERTICAL_BLANK_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61010h
MMIO: Base/Offset: MMADR/61010h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_B_VERTICAL_BLANK_END:** See pipe A description.
15:13	RO		**RESERVED1:** Write as zero.
12:0	RW		**PIPE_B_VERTICAL_BLANK_START:** See pipe A description.

1.11.326 DISPLAY_CONTROLLER.VGACNTRL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//71400h
MMIO: Base/Offset: MMADR/71400h
IO: Base/Offset:

This register provides support for VGA compatibility modes. This register is used by video BIOS only.

Bit	Access	Default Value	Description
31	RW		**VGA_DISPLAY_DISABLE:** This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000 BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA register settings. VGA display should only be enabled if all display planes other than VGA are disabled. After enabling the VGA most display planes need to stay disabled only the VGA popup cursor A can be enabled. The VGA display is never trusted. No secrets are allowed in the pre allocated memory and VGA is limited to access only that memory. During trusted operation when registers are locked via Lock this bit will always act as if it was set to a one disabled VGA display . 1 VGA Display Disabled
30	RW		**VGA_POP_UP_2X_CENTERED_MODE_SCALING:** When this bit is set to a one the VGA and pop up data is scaled using pixel doubling in both the horizontal and vertical direction for use on un scaled flat panel displays. Setting this bit allows the VGA to run at higher dot clock frequencies and creates a larger 4x the size image for better quality on larger displays. It is intended for use in one of the centering modes when not using the internal panel fitting. Do not use it for native VGA modes or when internal panel fitting is used to scale VGA. In the situations where it is used for 1280 wide or larger panels this bit should be set. For exactly 1280 wide panels the Nine dot disable bit should also be set. This operation is in addition to the VGA functions that double the pixels and lines. 0 VGA display is normal size 1 VGA and VGA popup data is doubled in the horizontal and vertical direction.

Bit	Access	Default Value	Description
29	RW		**VGA_PIPE_SELECT:** This bit only applies to devices with dual pipe support. For devices with a single display pipe this bit will be ignored. For dual pipe devices this bit determines which pipe is to receive the VGA display data. This must be changed only when the VGA display is in the disabled state via the VGA display disable bit or during the write to enable VGA display. 0 Selects Assigns the VGA display to Pipe A 1 Selects Assigns the VGA display to Pipe B
28:27	RO		**RESERVED0:**
26	RW		**VGA_BORDER_ENABLE:** This bit determines if the VGA border areas during VGA centering modes are included in the active display area and do or do not appear on integrated TV encoder output and devices that use centering such as on DVO connected flat panel TV displays or integrated panels. For use with the internal panel fitting logic the border if enabled will be scaled along with the pixel data. Setting this bit allows the popup to be positioned overlapping the border area of the image. 0 VGA Border areas are not included in the image size calculations for centering only active area. 1 VGA Border areas are enabled and is passed to the display pipe for display and used in the image size calculation for centering modes
25:24	RW		**VGA_CENTERING_ENABLE:** VGA centering modes use the pipe timing generators to determine the actual display timings. This would normally correspond to the display panel size and timings. The VGA registers determine the centered VGA image height and width. The VGA border may or may not be considered in the calculation selected by the VGA Border Enable bit. For a proper image the VGA image size should not exceed the pipe timing generator active rectangle. When using the internal panel fitting logic the horizontal image size needs to be less than or equal to 2048 pixels to generate a proper image. The VGA image will either be centered within the pipe timing rectangle or appear in the upper left corner. Upper left corner centered mode is generally used for external panel scaling where the DVO stall signal is used and is always used for internal panel fitting operation. When panel fitter is enabled on the same pipe as VGA this register setting is ignored and upper left corner centered mode is always selected. When centering is disabled the VGA CRTC registers determine the display timing compatible with legacy VGA devices for driving CRT like devices. 01 VGA centering is enabled VGA image appears in the center of the larger rectangle
23	RW		**VGA_PALETTE_READ_SELECT:** This bit only applies to dual display pipe devices and determines which palette VGA palette read accesses will occur from. 0 VGA palette reads will access Palette A default . 1 VGA palette reads will access Palette B VGA palette reads are reads from I O address 0x3c9.
22	RW		**VGA_PALETTE_A_WRITE_DISABLE:** This determines which palette the VGA palette writes will have as a

Bit	Access	Default Value	Description
			destination. One or both palettes can be the destination. If both are disabled writes will not affect the palette RAM contents. 0 VGA palette writes will update Palette A default . 1 VGA palette writes will not update Palette A VGA palette writes are writes to I O address 0x3C9h.
21	RW		**DUAL_PIPE_VGA_PALETTE_B_WRITE_DISABLE:** This determines which palette the VGA palette writes will have as a destination. One or both palettes can be the destination. If both are disabled writes will not affect the palette RAM contents. 0 VGA palette writes will update Palette B default . 1 VGA palette writes will not update Palette B VGA palette writes are writes to I O address 0x3C9h.
20	RW		**LEGACY_VGA_8_BIT_PALETTE_ENABLE:** This bit only affects reads and writes to the palette through VGA I O addresses. In the 6 bit mode the 8 bits of data are shifted up two bits on the write upper two bits are lost and shifted two bits down on the read. It provides backward compatibility for original VGA programs in it s default state as well as VESA VBE support for 8 bit palette. It does not affect palette accesses through the palette register MMIO path. 0 6 bit DAC default . 1 8 bit DAC.
19	RW		**PALETTE_BYPASS:** 0 Pass VGA data through the palette for translation Normal Operation 1 Bypass the palette for allowing testing without loading palette both VGA and popup data will bypass the palette in this mode.
18	RW		**NINE_DOT_DISABLE:** Prevents DOS applications from setting the VGA display into a real 9 dot per character operation mode instead the device emulates that using 8 dots per character. This is intended to provide VGA compatibility on DVI type connectors and integrated panels where there would otherwise not be room for the 720 horizontal pixels or 1440 pixels when horizontally doubled. The VGA register bit SR01 lt 0 gt functionality is disabled. VGA panning control handles the pseudo 9 dot mode when both this bit is set and SR01 lt 0 gt is clear. 0 Enable use of 9 dot enable bit in VGA registers 1 Ignore the 9 dot per character bit and always use 8
17	RO		**RESERVED1:**
16:8	RO		**RESERVED_2:**
7:6	RW		**BLINK_DUTY_CYCLE:** Controls the VGA text mode blink duty cycle relative to the cursor blink duty cycle. 00 100 Duty Cycle Full Cursor Rate Default 01 25 Duty Cycle Cursor Rate 10 50 Duty Cycle Cursor Rate 11 75 Duty Cycle Cursor Rate
5:0	RW		**VSYNC_BLINK_RATE:** Controls the VGA blink rate in terms of the number of VSYNCs per on off cycle. These bits are programmed with the VSYNCs cycle 2 1. The proper programming of this register is determined by the VSYNC rate that the display requires when in a VGA display mode.

1.11.327 DISPLAY_CONTROLLER.VIDEO_DIP_CTL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61170h
MMIO: Base/Offset: MMADR/61170h
IO: Base/Offset:

Please note that writes to this register take effect immediately. Therefore it is critical for software to follow the write and read sequences as described in the bit 31 text.

Bit	Access	Default Value	Description
31	RW		**ENABLE_GRAPHICS_DATA_ISLAND_PACKET:** Data Island Packet DIP is a mechanism that allows up to 36 bytes to be sent over digital port during VBLANK according to the HDMI specification. This includes header payload checksum and ECC information. Each type of DIP can be sent once per vsync once every other vsync or once. This data can be transmitted on either port digital port B or digital port C but not both simultaneously. Please note that the audio subsystem is also capable of sending Data Island Packets. These packets are programmed by the audio driver and can be read by in MMIO space via the audio control state and audio HDMI widget data island registers addresses 620B4h and 62118h respectively. Programming notes 0 Video DIP is disabled 1 Video DIP is enabled
30:29	RW		**PORT_SELECT:** This selects which port is to transmit the data island. This field must not be changed while data island transmission is enabled. Reserved settings are ignored. 00 Reserved Default DevCL and DevBW 01 Digital port B Default DevCTG DevBLC DevIntel® Atom™ Processor D2000 series and N2000 Series 10 Digital port C 11 Reserved
28	RO		**DIP_BUFFER_TRANSMISSION_ACTIVE_INDICATOR:** This bit indicates whether the DIP buffer referred to by the DIP buffer index bits 20 19 of this register is currently being transmitted. 0 Buffer transmission inactive 1 Buffer transmission active
27:25	RO		**RESERVED0:**
24:21	RW		**DATA_ISLAND_PACKET_TYPE_ENABLE:** These bits enable the output of a given data island packet DIP type. It can be updated while the port is enabled and is immediately updated not double buffered . Within 2 vblank periods the DIP is guaranteed to have been transmitted. XXX1 Enable AVI DIP Default enabled XX1X Enable Vendor specific DIP Default disabled X1XX Reserved 1XXX Enable Source Product Description DIP Default disabled
20:19	RW		**DIP_BUFFER_INDEX:** This field is used during programming of different DIPs. These bits are used as an index to their respective DIP buffers. The transmission frequency must also be written when programming the buffer. 00 Default AVI DIP 31 bytes of space available 01 Vendor specific DIP 10 Reserved 11 Source Product Description DIP
18	RO		**RESERVED1:**

Bit	Access	Default Value	Description
17:16	RW		**VIDEO_DIP_TRANSMISSION_FREQUENCY:** These bits dictate the frequency of Video DIP transmission for the DIP buffer index designated in bits 20 19. When writing Video DIP data this value is also latched when the first DW of the Video DIP is written. When read this value reflects the Video DIP transmission frequency for the Video DIP buffer designated in bits 20 19. 00 Default Send once 01 Send every vsync Default for AVI 10 Send at least every other vsync 11 Reserved
15:12	RO		**RESERVED2:** Read as zeroes
11:8	RO		**VIDEO_DIP_BUFFER_SIZE:** This reflects the buffer size in dwords available for the type of Video DIP being indexed by bits 20 19 of this register including the header. The maximum size of a Video DIP is 36 bytes. Please note that this count includes ECC bytes which are not writable by software. The minimum including the checksum header byte and ECC is ten bytes. These bits are immediately valid after write of the DIP index.
7:4	RO		**RESERVED3:** Read as zeroes
3:0	RW		**VIDEO_DIP_RAM_ACCESS_ADDRESS:** Selects the DWORD address for access to the Video DIP buffers. This value is automatically incremented after each read or write of the Video DIP Data Register. The value wraps back to zero when it auto increments past the max address value of 0xF. This field change takes effect immediately after being written. The read value indicates the current access address.

1.11.328 DISPLAY_CONTROLLER.VIDEO_DIP_DATA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61178h
MMIO: Base/Offset: MMADR/61178h
IO: Base/Offset:

Description Video control dprrega.v only at read if_ramcsrddata

Bit	Access	Default Value	Description
31:0	WO		**VIDEO_DIP_DATA:** When read this returns the current value at the location specified in the Video DIP buffer index select and Video DIP RAM access address fields. The index used to address the RAM is incremented after each read or write of this register. DIP data can be read at any time. Data should be loaded into the RAM before enabling the transmission through the DIP type enable bit. Accesses to this register are on a per DWORD basis.

1.11.329 DISPLAY_CONTROLLER.VSYNCSHIFT_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60028h

MMIO: Base/Offset: MMADR/60028h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:** Write as zero.
12:0	RW		**PIPE_A_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start. This vertical sync shift only occurs during the interlaced second field. In all other cases the vertical sync start positions aligned with horizontal sync start.

1.11.330 DISPLAY_CONTROLLER.VSYNCSHIFT_B

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61028h
MMIO: Base/Offset: MMADR/61028h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:13	RO		**RESERVED0:** Write as zero.
12:0	RW		**PIPE_B_SECOND_FIELD_VERTICAL_SYNC_SHIFT:** This value specifies the vertical sync alignment for the start of the interlaced second field expressed in terms of the absolute pixel number relative to the horizontal active display start.

1.11.331 DISPLAY_CONTROLLER.VSYNC_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//60014h
MMIO: Base/Offset: MMADR/60014h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Read Only.
28:16	RW		**PIPE_A_VERTICAL_SYNC_END:** This 13 bit field specifies the Vertical Sync End position expressed in terms of the absolute Line number relative to the vertical active display start. The value programmed should be the VSYNC End line position where the first active line is considered line 0 the second active line is considered line 1 etc. This register should be loaded with Vactive BottomBorder FrontPorch Sync 1. For interlaced display modes hardware automatically divides this number by 2 to get the vertical sync end in each field. It does not count the two half lines that get added when operating in modes with half lines.
15:13	RO		**RESERVED1:** Read Only.
12:0	RW		**PIPE_A_VERTICAL_SYNC_START:** This 13 bit field specifies the Vertical Sync Start position expressed in

Bit	Access	Default Value	Description
			terms of the absolute line number relative to the vertical active display start. The value programmed should be the VSYNC Start line position where the first active line is considered line 0 the second active line is considered line 1 etc. This register would be loaded with Vactive BottomBorder FrontPorch 1. For interlaced display modes hardware automatically divides this number by 2 to get the vertical sync start in each field. It does not count the two half lines that get added when operating in modes with half lines.

1.11.332 DISPLAY_CONTROLLER.VSYNC_BPIPE_B_VERTICAL_SYNC_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//61014h
MMIO: Base/Offset: MMADR/61014h
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_B_VERTICAL_SYNC_END:** See pipe A description.
15:13	RO		**RESERVED1:** Write as zero.
12:0	RW		**PIPE_B_VERTICAL_SYNC_START:** See pipe A description.

1.11.333 DISPLAY_CONTROLLER.VTOTAL_A

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6000Ch
MMIO: Base/Offset: MMADR/6000Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Read Only.
28:16	RW		**PIPE_A_VERTICAL_TOTAL_DISPLAY_LINES:** This 13 bit field provides Vertical Total up to 8192 lines encompassing the Vertical Active Display Lines top bottom border and retrace period. The value programmed should be the number of lines required minus one. Vertical total needs to be large enough to be greater than the sum of the vertical active vertical border and the vertical blank regions. The vertical counter is incremented on the leading edge of the horizontal sync. For interlaced display modes this indicates the total number of lines in both fields. In interlaced modes hardware automatically divides this number by 2 to get the number of lines in each field.
15:12	RO		**RESERVED1:** Read Only.

Bit	Access	Default Value	Description
11:0	RW		**PIPE_A_VERTICAL_ACTIVE_DISPLAY_LINES:** This 12 bit field provides vertical active display resolutions up to 4096 lines. It should be programmed with the desired number of lines minus one. When using the internal panel fitting logic the minimum vertical active area must be three lines. For interlaced display modes this indicates the total number of lines in both fields. In interlaced modes hardware automatically divides this number by 2 to get the number of lines in each field.

1.11.334 DISPLAY_CONTROLLER.VTOTAL_BPIPE_BVERTICAL_TOTAL_REGISTER

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//6100Ch
MMIO: Base/Offset: MMADR/6100Ch
IO: Base/Offset:

Bit	Access	Default Value	Description
31:29	RO		**RESERVED0:** Write as zero.
28:16	RW		**PIPE_B_VERTICAL_TOTAL_DISPLAY:** See pipe A description.
15:12	RO		**RESERVED1:** Write as zero.
11:0	RW		**PIPE_B_VERTICAL_ACTIVE_DISPLAY:** See pipe A description.

1.11.335 DISPLAY_CONTROLLER.YRGBSCALE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30140h
MMIO: Base/Offset: MMADR/30140h
IO: Base/Offset:

This register value is mirrored from DDR in address 40h R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:20	RO		**Y_RGB_VERTICAL_SCALE_FRACTION:** This is a fractional positive number that represents the scale factor to be used in vertical scaling for Y RGB components. For packed formats it applies to all color components. For planar YUV formats it is use for the Y luma component only. This field represents a value range from 0 to 1 0 lt Vertical Scale Fraction lt 1 . Defining a Ver_Scale_Factor as the ratio of source height to destination height. Ver_Scale_Factor Source Image Height Destination Height

Bit	Access	Default Value	Description
			For up scaling Y RGB Vertical Scale Fraction is Ver_Scale_Factor which is a fractional value. The integer portion should be set to zero. For downscaling Y RGB Vertical Scale Fraction is the fractional portion of Ver_Scale_Factor. The integer portion is in Y RGB Vertical Downscale Integer field. For devices with integrated panel fitting the single line mode requires that the vertical scale factor be determined by the panel height instead of the display mode s source height.
19	RO		**RESERVED0:** MBZ
18:16	RO		**Y_RGB_HORIZONTAL_DOWNSCALE_FACTOR_INTEGER:** This field is used for horizontal down scale. A value of zero is used to indicate upscale. In the case of planar formats it specifies the integer portion of the scale factor for Y data. This is used in backward compatible mode. Only horizontal downscaling of 2 or less is supported through the precision filter. For greater down scale factors it must be done through the render path.
15	RO		**RESERVED1:** MBZ
14:3	RO		**Y_RGB_HORIZONTAL_SCALE_FRACTION:** This is a fractional positive number that represents the scale factor to be used in horizontal scaling for Y RGB components. For both packed formats and planar YUV formats this field applies to all color components. This field represents a value range from 0 to 1 0 lt X Scale Fraction lt 1 . For the situations that are other than downscaling we can define a Hor_Scale_Factor as the ratio of source width to destination width. Hor_Scale_Factor Source Width Destination Width. For up scaling Y RGB Horizontal Scale Fraction is Hor_Scale_Factor which is a fractional value. For downscaling Y RGB Horizontal Scale Fraction is the fractional portion of Hor_Scale_Factor. The integer portion is in Y RGB Horizontal Downscale Integer field. For the situation that is downscaling we can define a Hor_Scale_Factor as the ratio of source width to destination width for up scaling modes Hor_Scale_Factor Destination Width Source Width. For downscaling Y RGB Horizontal Scale Fraction is the fractional portion of Hor_Scale_Factor.
2:0	RO		**RESERVED2:** MBZ

1.11.336 DISPLAY_CONTROLLER.YRGB_VPH

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//3011Ch
MMIO: Base/Offset: MMADR/3011Ch
IO: Base/Offset:

This register value is mirrored from DDR in address 1Ch R W . The memory Address Offset in DDR is Read Write.

Bit	Access	Default Value	Description
31:20	RO		**Y_RGB_VERTICAL_PHASE_FOR_FIELD_1:** This fractional value sets the initial vertical phase for field 1. For packed formats it applies to both YUV and RGB buffers. For planar formats it only applies to Y buffers. When the overlay buffers are in Interleaved buffer format this value sets the initial vertical phase for field 1 in all YUV RGB buffers. When the overlay buffers are in Non Interleaved format this value is intended for field 1. The value now applies to a particular YUV RGB buffer.
19:16	RO		**RESERVED0:** Software should set all the 16 bits for forward compatibility in case more accurate DDA phase is implemented.
15:4	RO		**Y_RGB_VERTICAL_PHASE_FOR_FIELD_0:** This fractional value sets the initial vertical phase for field 0. For packed formats it applies to YUV or RGB buffers. For planar formats it only applies to Y buffers. When the overlay buffers are in Interleaved buffer format this value sets the initial vertical phase for field 0 in all YUV RGB buffers. When the overlay buffers are in Non Interleaved format this value is intended for field 0. The value applies to a particular YUV RGB buffer.
3:0	RO		**RESERVED1:** Software should set all the 16 bits for forward compatibility in case more accurate DDA phase is implemented.

1.11.337 DISPLAY_CONTROLLER.Y_HCOEFS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30400h
MMIO: Base/Offset: MMADR/30400h
IO: Base/Offset:

This register value is mirrored from DDR in address 300h R W . The memory Address Offset in DDR is Read Write. The offset is 300h 4FFh

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_Y_HORIZONTAL_FILTER_COEFFICIENT:**

1.11.338 DISPLAY_CONTROLLER.Y_VCOEFS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 06h//30300h
MMIO: Base/Offset: MMADR/30300h
IO: Base/Offset:

This register value is mirrored from DDR in address 200h R W . The memory Address Offset in DDR is Read Write. The offset is 200h 2FFh

Bit	Access	Default Value	Description
31:0	RO		**OVERLAY_Y_VERTICAL_FILTER_COEFFICIENT:**

1.11.339 DMI.AERECH_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1c0h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f6a90)The PCI Express Advanced Error Reporting (AER) capability is an optional extended capability. It has been implemented in this MCH, but may not be publicly exposed. If it is exposed, as controlled by the Capabilities List Control registers, the INTEL RESERVED note can be removed from all AER registers.

Bit	Access	Default Value	Description
31:20	RO	000000000000b	**NCO:** NCO Next Capability Offset 31:20 000h RO This field contains the offset to the next PCI Express capability structure or 000h if no other items exist in the linked list of capabilities. For Extended Capabilities implemented in device configuration space, this offset is relative to the beginning of PCI compatible configuration space and thus must always be either 000h (for terminating list of capabilities) or greater than 0FFh. This is the last capability in the PCI Express extended capabilities list.
19:16	RO	0001b	**CV:** CV Capability Version 19:16 1h RO This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Must be 1h for this version of the specification.
15:0	RO	0000000000000001b	**PCIEECID:** PCIEECID PCI Express Extended Capability ID 15:0 0001h RO This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. Extended Capability ID for the Advanced Error Reporting Capability is 0001h.

1.11.340 DMI.AFERTMG_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d04h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RW	0b	**RLNGT0SQEN:** #MMR_0_1_0.xml#- This bit defines lane squelch detection behavior in L0s and L1 ;
2:1	RW	00b	**RLNGT0EN:** #MMR_0_1_0.xml#- This field defines lane receiver enable behavior in L0s and L1 ;
31:3	RO	0b	**RSVD3:**

1.11.341 DMI.BGFCTL1_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d6ch/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
11:7	RW	00001b	**RDG1:** #DMI_0_0_0.xml#- This register defines the BGF Ratio delta for Gen 1. Delta between the fast and slow clock multiplier ;
6:1	RW	111000b	**BINITG1:** #DMI_0_0_0.xml#- This register defines the Initial value for the bubble generator bubble mask. ;
16:12	RW	01111b	**SRG1:** #DMI_0_0_0.xml#- This field defines the BGF slow ration for gen1 ;
0	RW	1b	**FBEN:** #DMI_0_0_0.xml#- This bit enable Bubble generator on F clk side of BGF ;
0	RO	0b	**RSV1:**
30	RO	0b	**RSV30:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

1.11.342 DMI.BGFCTL2_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d70h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
11:7	RW	00111b	**RDG2:** #DMI_0_0_0.xml#- This register defines the BGF Ratio delta for Gen 2. Delta between the fast and slow clock multiplier ;
6:1	RW	111100b	**BINITG2:** #DMI_0_0_0.xml#- This register defines the Initial value for the bubble generator bubble mask. ;

16:12	RW	01000b	**SRG2:** #DMI_0_0_0.xml#- This field defines the BGF slow ration for gen2 ;
0	RO	00b	**RSVD0:**
31:17	RO	000000000000000b	**RSVD18:**

1.11.343 DMI.BGFCTL3_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d74h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
16:12	RW	00100b	**SR200MHZ:**
11:7	RW	00001b	**RD200MHZ:**
6:1	RW	111110b	**BINIT200MHZ:**
0	RO	0b	**FBEN200MHZ:**
31:17	RO	00000000000000000b	**RSVD18:**

1.11.344 DMI.BGFCTL4_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d68h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
11:7	RW	00000b	**RDG2:**
6:1	RW	111110b	**BINITG2:**
16:12	RW	00001b	**SRG2:**
0	RO	0b	**RSVD0:**
31:17	RO	00000000000000000b	**RSVD18:**

1.11.345 DMI.CAPID0_ACMN_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/568h/
MMIO: Base/Offset:
IO: Base/Offset:

Control of bits in this register are only required for customer visible SKU differentiation

Bit	Access	Default Value	Description
28	RO	0b	**PEG10D:** #MMR_0_1_0.xml#- 0: Device 1 Function 0 and associated memory spaces are accessible. ;

Bit	Access	Default Value	Description
			#MMR_0_1_0.xml#-1: Device 1 Function 0 and associated memory and IO spaces are disabled by hardwiring the D1F0EN field, bit 3 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to '0'. ;
21	RO	0b	**PEGG2DIS:** #MMR_0_1_0.xml#- 0: Capable of running any of the PEG controllers in Gen 2 mode ; #MMR_0_1_0.xml#-1: Not capable of running any of the PEG controllers in Gen 2 mode ;
24	RO	0b	**RSVD24:** #MMR_0_1_0.xml#- Not Implemented ;
31	RO	0b	**PEG60D:** #MMR_0_1_0.xml#- 0: Device 6 Function 0 and associated memory spaces are accessible. ; #MMR_0_1_0.xml#-1: Device 6 Function 0 and associated memory and IO spaces are disabled by hardwiring the D6F0EN field, bit 13 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to '0'. ;
23	RO	0b	**RSVD23:** #MMR_0_1_0.xml#- Not Implemented ;
30	RO	0b	**PEG12D:** #MMR_0_1_0.xml#- 0: Device 1 Function 2 and associated memory spaces are accessible. ; #MMR_0_1_0.xml#-1: Device 1 Function 2 and associated memory and IO spaces are disabled by hardwiring the D1F2EN field, bit 1 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to '0'. ;
27	RO	0b	**PELWUD:** #MMR_0_1_0.xml#- 0: Link width upconfig is supported. The CPU advertises upconfig capability using the data rate symbol in its TS2 training ordered sets during Configuration. Complete. The CPU responds to link width upconfigs initiated by the downstream device. ; #MMR_0_1_0.xml#-1: Link width upconfig is NOT supported. The CPU does not advertise upconfig capability using the data rate field in TS2 training ordered sets during Configuration. Complete. The CPU does not respond to link width upconfigs initiated by the downstream device. ;
22	RO	0b	**DMIG2DIS:** #MMR_0_1_0.xml#- 0: Capable of running DMI in Gen 2 mode ; #MMR_0_1_0.xml#-1: Not capable of running DMI in Gen 2 mode ;
29	RO	0b	**PEG11D:** #MMR_0_1_0.xml#- 0: Device 1 Function 1 and associated memory spaces are accessible. ; #MMR_0_1_0.xml#-1: Device 1 Function 1 and associated memory and IO spaces are disabled by hardwiring the D1F1EN field, bit 2 of the Device Enable register, (DEVEN Dev 0 Offset 54h) to '0'. ;
25	RO	0b	**RSVD25:** #MMR_0_1_0.xml#- Not Implemented ;
26	RO	0b	**DW:** #MMR_0_1_0.xml#- 0: DMI x4 ; #MMR_0_1_0.xml#-1: DMI x2 ;
18	RO	0b	**PEGX16D:** #MMR_0_1_0.xml#- 0: Capable of x16 PEG Port ; #MMR_0_1_0.xml#-1: Not Capable of x16 PEG port, instead PEG limited to x8 and below. Causes PEG port to enable and train logical lanes 7:0 only. Logical

Bit	Access	Default Value	Description
			lanes 15:8 are powered down (unless in use by the other PEG port or the embedded Display Port), and the Max Link Width field of the Link Capability register reports x8 instead of x16. (In the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down.) ;
20:19	RO	00b	**RSVD2019:** #MMR_0_1_0.xml#- Not Implemented ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**

1.11.346 DMI.CAPID0_B_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/564h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RO	0b	**SPEGFX1:** #MMR_0_1_0.xml#- This bit has no effect on Device 1 unless Device 1 is configured for a single port via PEG1CFGSEL strap. ;
1	RO	0b	**DPEGFX1:** #MMR_0_1_0.xml#- This bit has no effect on Device 1 unless Device 1 is configured for at least two ports via PEG1CFGSEL strap. ;
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**

Bit	Access	Default Value	Description
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.347 DMI.CCCR_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d8ch/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
1	RW	0b	**CTYPE:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This bit defines the command type. ;
7:4	RW	0000b	**RADDR:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This bit defines which of the Credit Released registers we read/write as follows: ;
0	RW1C	0b	**CRB:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This bit is set to 1 whenever SW writes to this register. This bit is cleared to 0 by HW when the command specified in Command Type field is complete. ;
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.348 DMI.CCRPR_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d84h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
23:16	RO	00000000b	**CCRH:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This field holds sampled value from the credit released register pointed to by Register Address field of Cross Clock Command Register as a result of read command. ;
11:0	RO	000000000000b	**CCRD:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This field holds sampled value from the credit released register pointed to by Register Address field of Cross Clock Command Register as a result of read command. ;
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.349 DMI.CCWPR_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d88h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
11:0	RW	000000000000b	**CCWD:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- Data written to this field is copied into the credit released register pointed to by Register Address field of Cross Clock Command Register as a result of write command. Write to this register while CCCR.CRF is not 0 is illegal and yield undefined behavior. ;
23:16	RW	00000000b	**CCWH:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- Header written to

Bit	Access	Default Value	Description
			this field is copied into the credit released register pointed to by Register Address field of Cross Clock Command Register as a result of write command. Write to this register while CCCR.CRF is not 0 is illegal and yield undefined behavior. ;
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.350 DMI.CFG2_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/250h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
7	RW	0b	**CFGR:** #MMR_0_1_0.xml#- Forces PCI Express-G link into the Configure Receiver State. This is cleared automatically once the link successfully retrains. ;
6:5	RW	01b	**DSKWRSTMD:** #MMR_0_1_0.xml#- This register use to enable/disable dskew buffer reset feature. ;
11:10	RW	00b	**SQLCHINFERSEL:**
16	RW	0b	**ERRMSKRXL0:** #MMR_0_1_0.xml#- '0': Rx errors are unmasked whenever the RxL0 indicator to link layer is asserted. ; #MMR_0_1_0.xml#-'1': Rx errors are only unmasked when the main LTSSM is in L0. ;
15	RW	0b	**PA:** #MMR_0_1_0.xml#- Forces PCI Express-G link into the Polling Active State. ; #MMR_0_1_0.xml#- Note: this bit can only be set in L0. This bit should be cleared once LTSSM transitions to Polling Active state. ;
24	RW	0b	**DSBYP:** #MMR_0_1_0.xml#- Forces PCI Express-G link to bypass the COM de-skew process for all lanes. ; #MMR_0_1_0.xml#-Setting this bit is for test only and may cause erroneous behavior. ;

Bit	Access	Default Value	Description
4	RW	0b	**NEDLBE:** #MMR_0_1_0.xml#- 0: normal operation ; #MMR_0_1_0.xml#- 1: enable NEDLB mode ;
23	RW	1b	**RXTODEBE:** #MMR_0_1_0.xml#- Enable to debounce rx squelch exit detection. Wait for 20ns timeout after we see squelch exit to enable receiver turn on. ; #MMR_0_1_0.xml#-1` : Wait for 20ns ;
18	RW	0b	**L1L2ENTRY:** #MMR_0_1_0.xml#- '0': During L1/L2 entry negotiation, upon receiving an EIOS on any lane, we stop scheduling PM messages and wait until link layer is idle before transitioning from L0 to L1/L2. ; #MMR_0_1_0.xml#-'1': Disable this fix. De-assert RxL0 indication immediately upon entering Recovery. ;
25	RW	0b	**IRFELB:** #MMR_0_1_0.xml#- Loop back bit will be set in the TS1/TS2 training sequence causing the component on the other side of the link to enter the Far-end digital loop back mode. This device will act as the ;
17	RW	0b	**L0ENTRYFRMIDLE:** #MMR_0_1_0.xml#- '0': During Configuration. Idle/Recovery. Idle, we indicate RxL0 to link layer after receiving 8 consecutive IDLE data symbols and sending 8 consecutive IDLE data symbols. ; #MMR_0_1_0.xml#-'1': Disable this fix. We indicate RxL0 after receiving 8 consecutive IDLE data symbols and sending 16. ;
26	RW	0b	**FAST_RST:** #MMR_0_1_0.xml#- 0b Normal Training ; #MMR_0_1_0.xml#-1b Fast Training ;
14	RW	0b	**COMPLIANCERECEIVE:**
19	RW	0b	**RCVRYENTL0:** #MMR_0_1_0.xml#- '0': During L0 to Recovery entry, we do not deassert RxL0 indication to link layer until we have received a TS1 or TS2 in either L0 or Recovery.MMR_0_1_0.xml-'1': Disable this fix. De-assert RxL0 indication immediately upon entering Recovery.
9:8	RW	11b	**LNSTAGGERINGVAL:**
13:12	RW	00b	**EIEPREFTS:**
3	RW	0b	**FRCDISPDIS:** #MMR_0_1_0.xml#- By Default, root port will force the disparity on the first COM of a skip ordered set after Latency Fixing is Done in manufacturing mode. Programming this bit to 1 disables forcing disparity.
22:20	RW	101b	**SQEXTDEB:** #MMR_0_1_0.xmlSquelch Exit Debounce Programmability bits. The timeout value is for counting linkclks between when we see a squelchexit and when we turn on receivers.
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
27	RW	0b	**P2INL1EN:** Enables to change to P2 powermode in L1 state (instead of P1)
28	RW	0b	**P2CLKBUFDIS:** Disable the PLL clock buffers in P2

Bit	Access	Default Value	Description
29	RW	1b	**RXL0SSKIPRXON:** Skip RX L0s RXON state and move directly from RXL0SIDLE to RXL0SRXRESET
30	RW	1b	**RXDISABLEL0SIDLE:** Disable the Rx lanes when the LTSSM in RxL0s state.
31	RO	0b	**RSVD31:**

1.11.351 DMI.CFG3_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/254h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC

Bit	Access	Default Value	Description
6:0	RW	0010000b	**RBD:** #DMI_0_0_0.xml#- Number of entries (CL) available in the Retry Buffer. Range is 1 - 48 decimal. Minimum valid value is 0000001 (1 CL or 1 Entry). ;
13:8	RW	001111b	**RBLUTD:** #DMI_0_0_0.xml#- Number of entries available in the Retry Buffer Look-up Table. Range is 1 - 47 decimal. Minimum valid value is 00001 (2 entries). Default value is 2Fh (47 entries). ; #DMI_0_0_0.xml#- BLKC HSDCN#391451 ;
31	RW	0b	**ACRSTEND:** #DMI_0_0_0.xml#- This Bit is used to reset the Accumulator counter within the RX Dispatcher in Link Layer on receiving an END symbol while operating in a Link Width below the max supported (Gen2 x16). ; #DMI_0_0_0.xml#- By Default Accumulator counter will reset only when the counter reaches the max count for the respective width of operation. ;
20:16	RW	01100b	**RBVQD:** #DMI_0_0_0.xml#- There will be a virtual queue within the Retry Buffer based off of the difference between the load and unload pointers that will only advertise enough space to the Transaction Layer such that no more than one non-transmitted, maximum sized packet can be stored within the Retry Buffer at any time. ;
30	RW	0b	**DISMULTDLLPARBITRATION:**
7	RO	0b	**RSVD7:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**

Bit	Access	Default Value	Description
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

1.11.352 DMI.CFG4_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/258h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d4d00)general CFG (interrupt A/b/c/d , enable debug alignment VDM ,clear Error poison downstream , downstream chain disable, vc1 Q size, L1 completion time out)

Bit	Access	Default Value	Description
0	RW	0b	**OUPF:** OUPF Override upstream Posted fields 0:0 0b RW This Bit is used to revert to legacy ILK behavior with regard to TAG and reserved fields of upstream posted request 0 - (default) Tag and reserved bits are forwarded untouched from line to the Primary channel 1 - Send zero in the Tag and reserved bits regardless of the attributes of the request.
10:8	RW	110b	**VC1CQS:** VC1CQS VC1 Completion Q size 10:8 6h RW This field defines the depth of the VC1 completion Queue. This field is valid only for PEG10 in UMA mode. Legal values are 1-6
25:24	RW	00b	**LIBM:** LIBM Legacy Interrupt Binding Map 25:24 00b RW Upstream received Assert/Deassert_INTx interrupt messages are mapped to interrupt messages sent over primary channel based on binding map configuration bits as follows: 00b(Default)- INTA -> INTA
23	RW	0b	**MRGDIS:** MRGDIS Downstream Merge Disable 23:23 0b RW This bit controls chain merging in the downstream Transaction Layer 0 - Merge enabled per max packet size 1 - Merge disabled. Completion and downstream posted are sent CL per transaction.
29	RW	1b	**DALGNDIS:** DALGNDIS Debug Alignment Message Generation Disable 29:29 0b RW This bit disables generation of
2	RW	0b	**L1CTM:** L1CTM L1 Completion Timeout Mode 2:2 0b RW '0' : PCIe Spec Compliant. Completion timeout is disabled during software initiated L1, and enabled during ASPM initiated L1. '1': Completion timeout is enabled during L1, regardless of how L1 entry was initiated
31	RW	0b	**DRPSMCB:** Drop SM fix CB - fix for 2 simultaneous Ur

Bit	Access	Default Value	Description
			request & UR request bigger than 2 fragments
28	RW	0b	**VDMLENCB:** UR request of VDM with length bigger than 16 DW
1	RO	0b	**RSVD1:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
30	RO	0b	**RSVD30:**

1.11.353 DMI.CFG_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/200h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
15	RW	1b	**DKSW_BUF_RST_CTL:**
14:0	RO	000000000000000b	**RSVD0:**
31:16	RO	0b	**RSVD16:**

1.11.354 DMI.CMMPC_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/230h/
MMIO: Base/Offset:
IO: Base/Offset:

control lane reversal , This register contains the control bits and status information for the CMM. Programming of this register must take place prior to Starting CMM (setting 230h[0]=1.

Bit	Access	Default Value	Description
30	RO	0b	**CMMSTS:** The Intel CMM start bit is set by software and controls entry into Intel CMM mode. ; ; When the master LTSSM enters Intel CMM mode, the CMM status bit is set. ; ; When the master LTSSM exits Intel CMM mode, the CMM status bit is cleared. ; ; (The status bit will always be on when the device is in Intel CMM mode, will clear when exited.) ; ; For PCI Express Spec CMM Mode, the status bit is NOT set. (Lakeport doesn't toggle/update this bit either in spec CMM mode.) ;
12:10	RO	000b	**CMMSENI:** Indicates which register number miscompared on the failing lane, if the failing lane was an inverted lane. Only valid when CMM Error Detected is 1. ; ; 000: CMM Data D0 ; ; 001: CMM Data D0 ; ; 010: CMM Data D0 ; ; 011: CMM Data D1 ; ; 100: CMM Data D2 ; ; 101: CMM Data D3 ; ; 110: CMM Data D0 ; ; 111: CMM Data D0 ; ; This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated). ;
9:8	RO	00b	**CMMSEN:** Indicates which register number miscompared on the failing lane, if the failing lane was not inverted. Only valid when CMM Error Detected is 1. ; ; 00: CMM Data 0 ; ; 01: CMM Data 1 ; ; 10: CMM Data 2 ; ; 11: CMM Data 3 ; ; This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated). ;
25:22	RO	0000b	**CMMELN:** This field contains the lane number of the failing lane. ; ; This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated). ;
3	RW	1b	**CMMAI:** Indicates which lanes are inverted ; ; 0h: No inversion ; ; 1h: Lanes 0, 8 ; ; 2h: Lanes 1, 9 ; ; 3h: Lanes 2, 10 ; ; 4h: Lanes 3, 11 ; ; 5h: Lanes 4, 12 ; ; 6h: Lanes 5, 13 ; ; 7h: Lanes 6, 14 ; ; 8h: Lanes 7, 15 ; ; others: Reserved ; ; This field is only valid when CMM Error Detected (bit 7) is asserted. Additionally, when CMM Error Detected is asserted this field is locked (will not be updated). ;
6:4	RW	000b	**CMMILN:** This selects the Lane number modulo 8 to invert. Every eighth lane is inverted. ; ; 000: Lanes 0, 8 ; ; 001: Lanes 1, 9 ; ; 010: Lanes 2, 10 ; ; 011: Lanes 3, 11 ; ; 100: Lanes 4, 12 ; ; 101: Lanes 5, 13 ; ; 110: Lanes 6, 14 ; ; 111: Lanes 7, 15 ;
31	RO	0b	**RSVD:** Previously is Enable Data Scrambling during Intel CMM (CMMSCMBEN) in BLKC ;

Bit	Access	Default Value	Description
2	RW	0b	**CMMIE:** #MMR_0_1_0.xml#- 1: Enables the Inversion of every eighth lane ; #MMR_0_1_0.xml#- 0: No lanes are inverted ;
27	RW	1b	**CMMS1S:** 0: selects CMM Symbol [1] to a control character ; ; 1: selects CMM Symbol [1] as a data character ;
16:13	RO	0000b	**CMMI:** #MMR_0_1_0.xml#- Indicates which lanes are inverted ;
0	RW	0b	**CMMS:** #MMR_0_1_0.xml#- 1: Start CMM Setting this bit results in the CMM status bit being set (214h[24]) ;
7	RO	0b	**CMMED:** 1: An error was detected, see CMM Error Lane Number for lane number. ; ; 0: No error detected. ; ; Note: This bit will be shadowed to an observability pin that can be used for IRQ generation. ;
29	RW	1b	**CMMS3S:** 0: selects CMM Symbol [3] to a control character ; ; 1: selects CMM Symbol [3] as a data character ;
1	RW	1b	**CMMID:** #MMR_0_1_0.xml#- 1b Disparity starts as positive ; #MMR_0_1_0.xml#-0b Disparity starts as negative ;
28	RW	0b	**CMMS2S:** 0: selects CMM Symbol [2] to a control character ; ; 1: selects CMM Symbol [2] as a data character ;
26	RW	0b	**CMMS0S:** 0: selects CMM Symbol [0] to a control character ; ; 1: selects CMM Symbol [0] as a data character ;
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**

1.11.355 DMI.CMMSB_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/234h/
MMIO: Base/Offset:
IO: Base/Offset:

This register contains the symbols that are transmitted on the link. Programming of this register must take place prior to Starting CMM (setting 230h[0]=1). This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.

Bit	Access	Default Value	Description
15:8	RW	10110101b	**CMMD1:** This character contains CMM Data [1].

Bit	Access	Default Value	Description
7:0	RW	10111100b	**CMMD0:** This character contains CMM Data [0].
31:24	RW	01001010b	**CMMD3:** This character contains CMM Data [3].
23:16	RW	10111100b	**CMMD2:** This character contains CMM Data [2].

1.11.356 DMI.DEBUGPL1_0_1_0_PCI

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/fch/
MMIO: Base/Offset:
IO: Base/Offset:

This is an Intel Reserved register to be used for debug purposes

Bit	Access	Default Value	Description
18	RW	0b	**DSKFLE:**
19	RW	0b	**UND2931207:**
20	RW	1b	**SPCE:**
17	RW	0b	**UND2994274:**
16	RW	0b	**TXEIDLE_MSK:**
15	RW	1b	**EIDLEEXIT_TXL0S:**
14	RW	1b	**EIDLEEXIT_L1:**
13	RW	1b	**EIDLEEXIT_POLLING:**
12	RW	1b	**DET2POLL_PHYSTATUS:**
11:0	RO	000000000000b	**RSVD11_0:**
31:21	RO	00000000000b	**RSVD31_21:**

1.11.357 DMI.DEBUGPLU_0_1_0_PCI

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/e4h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
31:16	RO	0000000000000000b	**RSVD:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- ;
4	RW	0b	**DSKWCHARSEL:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This use to switch between Lakeport fix/Broadwater fix on deskew character detect signal that use to achieve SKP deskew. ; /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- 1 - Broadwater Solution. Deskew character detect signal is

Bit	Access	Default Value	Description
			qualify with 8b10b error during SKP deskew. ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**

1.11.358 DMI.DEBUGPL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/f0h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
1:0	RO	00b	**RSVD1_0:** pci_dmi.xml- ;
5:4	RO	00b	**RSVD5_4:** pci_dmi.xml- ;
31:12	RO	00000000000000000000b	**RSVD31_12:** #DMI_0_0_0.xml#- Reserved for Future Use ;
11	RW	0b	**DOV:** Setting this bit forces the detect mechanism to detect the presence of a receiver on all lanes
10	RO	0b	**DMIX2:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- Define if we force detect DMI on 2 or 4 lanes ;
2	RW	0b	**SB:** 0: Normal operation. Scrambler and descrambler are used. ; pci_dmi.xml- Scrambling can only be disabled at the end of Configuration (when the link is disabled)
9:7	RO	000b	**RSVD9_7:** pci_dmi.xml- ;

Bit	Access	Default Value	Description
3	RW	0b	**DIGIFELBEN:** Force digital Far end loopback
6	RO	0b	**RSVD6:**

1.11.359 DMI.DEBUGTLLL1_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/e8h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
0	RW	0b	**SNCD:** #DMI_0_0_0.xml#- 0: Normal Operation. Sequence Number Checking enabled. ; #DMI_0_0_0.xml#- 1: Disables sequence number checking that is normally performed in the Data Link Layer. Corrupted packets will be allowed to be pass on to the Transaction Layer with ACK DLLPs being generated instead of NAK. ;
2	RW	0b	**CRCD:** #DMI_0_0_0.xml#- 0: Normal operation. Cyclic Redundancy Checking enabled. ; #DMI_0_0_0.xml#- 1: Disables CRC (error checking) that is normally performed in the Data Link Layer. Corrupted packets will be allowed to pass on to the Transaction Layer with ACK DLLPs being generated instead of NAK. ;
3	RW	0b	**PRDIS:** #DMI_0_0_0.xml#- This bit only affects operation of the PCI Express for x8 and above widths ; #DMI_0_0_0.xml#- 1: PCI Express will force all packets being transmitted to start in Lane 0. ;
8	RW	0b	**RBVQD:** #DMI_0_0_0.xml#- 0: Normal operation. ; #DMI_0_0_0.xml#- 1: Mask the retry buffer ;
6	RW	0b	**DISNEBF:** #DMI_0_0_0.xml#- Chicken bit for fixing Link layer passing on Header put to x-layer without a corresponding END indication. ;
5	RW	1b	**MSKLNGERR:** chicken bit to mask the writes to the data array in case of length error
4	RW	0b	**OATD:** #DMI_0_0_0.xml#- 0: Ack DLLPs will be scheduled for transmission as soon as possible ; #DMI_0_0_0.xml#- 1: Ack DLLPs will be scheduled for transmission only when the Ack Transmission Latency (PEGLC[18:11], Offset 208h) has been reached. ;
7	RW	0b	**PINVD:** #DMI_0_0_0.xml#- Under normal operating conditions, when the Data Link Layer receives a TLP that has Phy receive errors (i.e. 8b/10b or packet framing errors) associated with it, the packet is invalidated - the packet sequence number and CRC checks are ignored - and a Nak DLLP is sent in response. Setting this bit will allow the Data Link Layer to use the packet sequence and

Bit	Access	Default Value	Description
			CRC validation mechanisms to determine whether the packet should be invalidated or not. ; #DMI_0_0_0.xml#- 1: Packet Invalidate Disabled. ;
1	RW	0b	**DFED:** #DMI_0_0_0.xml#- Disable Frame Error Detection (DFED): When this bit is set ('1'), frame error detection logic related to BWR bug# 1628427 (TLP with DCODE to KCODE error is accepted as a valid tlp when DCODE and KCODE are the same) is disabled in link layer. ; #DMI_0_0_0.xml#- '1' - Fix for the bug is disabled ;
10:9	RW	00b	**RPLYNUM:** override to max replay number
11	RW	0b	**RPLYNUMEN:** enable to max replay num override
12	RW	0b	**CRCERREN:** CRC error injection enable downstream
20:13	RW	0b	**CRCERRBIT:** select the bit to inject the Error
21	RW	0b	**CLRINJECTION:** Clear Error injection
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.360 DMI.DEBUGTLLL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/f4h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f4b80)PCI Express debug control that is not required by the PCI Express spec. Place debug control that is not defined until after VHDL freeze in the DEBUP1 register. This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.

Bit	Access	Default Value	Description
5	RW	1b	**ROD:** #DMI_0_0_0.xml#- 0: If the Relaxed Ordering attribute is set, then the root port may be able to allow a Read Completion to pass a previously queued Posted Memory Write. ; #DMI_0_0_0.xml#- 1: The Relaxed Ordering attribute is always ignored. ;

Bit	Access	Default Value	Description
16	RW	1b	**BEMTED:** BEMTED Byte Enable Malformed TLP Error Disable 16:16 1b RW 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
19	RW	0b	**TVMMTED:** TVMMTED TC/VC Mapping Malformed TLP Error Disable 19:19 0b RW 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
17	RW	0b	**LMTED:** LMTED Length Malformed TLP Error Disable 17:17 0b RW Completion including data must specify the actual amount of data returned in that Completion, and must include the amount of data specified in TLP. 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
13	RW	0b	**VC0SNRO:** VC0SNRO VC0 SNR Override 13:13 0b RW 0: Use the Vc0 upstream
18	RW	0b	**FOURKBMTED:** FOURKBMTED Four K Boundary Malformed TLP Error Disable 18:18 1b RW Requests must not specify an Address/Length combination which causes a Memory Space access to cross a 4K boundary. 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
20	RW	0b	**NTMMTD:** NTMMTD Non-TC0 Message Malformed TLP Error Disable 20:20 0b RW One of the following Messages did not use the default Traffic Class designator (TC0) as required: - Assert_INTx and Deassert_INTx interrupt Messages - Power Management Messages - Error Signaling Messages 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
22	RW	0b	**TDMTED:** TDMTED TLP Digest Malformed TLP Error Disable 22:22 0b RW A TLP where the TD (TLP Digest) field value does not correspond with the observed size (accounting for the data payload, if present) with a 1b in the TD field but without a TLP Digest, or a TLP with a TLP Digest but without a 1b in the TD field, is a Malformed TLP. TLP length checking related to TD is a subset of the TLP length checking controlled by bit 17 (Length Malformed) of this register. That bit must also be set in order to fully prevent TLP Digest Malformed Length errors from being checked and potentially generating Malformed TLP errors. 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
31:24	RO	000000000b	**RSVD:**
21	RW	0b	**UCCMTED:** UCCMTED Unexpected CRS Completion Malformed TLP Error Disable 21:21 0b RW Received

Bit	Access	Default Value	Description
			CRS completion for other than down-stream config cycle. 0: Check for this Malformed TLP Error condition WILL be performed. 1: Check for this Malformed TLP Error condition will NOT be performed.
12	RW	0b	**VC0SNROV:** VC0SNROV VC0 SNR Override Value 12:12 0b RW Bit 13 must be set for this bit to be meaningful. 0: All VC0 upstream read and write accesses are snooped regardless of the
23	RO	0b	**MSK_BAD_AT:** this field is masking the report for bad AT fields
15	RW	0b	**MALFDIS:** 1 : malformed detection at link layer is disabled when ; 0 : detection of all malformed is in the link layer
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
14	RO	0b	**RSVD14:**

1.11.361 DMI.DEBUP3_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d14h/
MMIO: Base/Offset:

IO: Base/Offset:

Bit	Access	Default Value	Description
31:16	RW	1111111111111111b	**RSVDH:** #DMI_0_0_0.xml#- Reserved ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**

Bit	Access	Default Value	Description
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**

1.11.362 DMI.DMIATM_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/20ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f8fe0)Address translation config

Bit	Access	Default Value	Description
28:27	RW	00b	**ATMA:** ATMA Attribute Translation Mode Attribute 28:27 00b RW Use this Attribute when Attribute Translation Mode is enabled and corresponding mask bits are set. Bit 17 corresponds to Relaxed Ordering. Bit 16 corresponds to No Snoop.
30:29	RW	00b	**ATMATM:** ATMATM Attribute Translation Mode Attribute Mask 30:29 00b RW When these bits are set and the Attribute Translation Mode is enabled the corresponding ATM Attribute bits are used. Bit 19 corresponds to Relaxed Ordering. Bit 18 corresponds to No Snoop.
18:0	RW	00000000000000000b	**ATMADM:** ATMADM Attribute Translation Mode Address Mask 18:0 00000h RW Set these bits to mask address bits 38:20 when Attribute Translation Mode is enabled.
22:19	RO	0000b	**ATMTC:** ATMTC Attribute Translation Mode Traffic Class 22:19 0000b RO-FW Use this Traffic Class when Attribute Translation Mode is enabled and corresponding mask bits are set.
26:23	RW	0000b	**ATMTCM:** ATMTCM Attribute Translation Mode Traffic Class Mask 26:23 0000b RW When these bits are set and the Attribute Translation Mode is enabled the

Bit	Access	Default Value	Description
			corresponding ATM Traffic Class bits are used.
31	RW	0b	**ATME:** ATME Attribute Translation Mode Enable 31:31 0b RW 0: Programming this register has no effect. 1: The values in this register are used.

1.11.363 DMI.DMICC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/208h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f8f80)

Bit	Access	Default Value	Description
31:30	RW	00b	**PMET:**
21:20	RW	00b	**L0SEP:** L0SEP L0s Entry Policy 21:20 00b RW Once this bit is set, PCI Express Initialization unit will use aggressive L0s entry policy where 1/4th of the normally waited IDLE time is required. 00: Initialization Unit waits for
14:12	RW	111b	**CT:** CT Completion Timeout 14:12 000b RW Determines the number of milliseconds the Transaction Layer will wait to receive an expected completion. To avoid hang conditions, the Transaction Layer will generate a dummy completion to the requestor if it does not receive the completion within this time period. 000b Completion Timeout Disabled 001b 1 Fclk Cycle (1.25ns), Required to hit some boundary conditions while testing (DFV) 010b 1 µsec, Used for production test 100b Reserved 101b Reserved 110b 12 msec, Used for system debug to allow for decent LA tracing x11b 48 ms, For normal operation
10:0	RW	10010110000b	**SOSL:** SOSL SKIP Ordered-Set Latency 10:0 4B0h RW Minimum number of symbol times (i.e. number of Lclk cycles) the Data Link Layer will wait between transmitting SKIP ordered-sets. Range is 0 - 2048. Register is initialized to 1200 Symbol Times, but should be programmed between 1180 and 1538 Symbol Times per PCI Express spec. When value N is configured, the gap between 2 consecutive SKP_OS will be N+2 The SKIP ordered-set is a sequence of control symbols (one COM symbol followed by three SKP symbols) that are transmitted onto each lane of the PCI Express Link to compensate for clock frequency differences between the transmitting agent and the receiving agent.
11	RO	0b	**RSVD11:**
15	RO	0b	**RSVD15:**

Bit	Access	Default Value	Description
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

1.11.364 DMI.DMICEMSK_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1d4h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f8dd0)This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.

Bit	Access	Default Value	Description
13	RW	1b	**ANFEM:** ANFEM Advisory Non-Fatal Error Mask 13:13 1b RWS When set, masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register, and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting.
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**

Bit	Access	Default Value	Description
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.365 DMI.DMICESTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1d0h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f8d40)This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation

Bit	Access	Default Value	Description
8	RO	0b	**RNRS:** RNRS REPLAY_NUM Rollover Status 8:8 0b RW1CS
7	RO	0b	**BDLLPS:** BDLLPS Bad DLLP Status 7:7 0b RW1CS
12	RO	0b	**RTTS:** RTTS Replay Timer Timeout Status 12:12 0b RW1CS

Bit	Access	Default Value	Description
13	RO	0b	**ANFES:** ANFES Advisory Non-Fatal Error Status 13:13 0b RW1CS When set, indicates that an Advisory Non-Fatal Error occurred.
0	RO	0b	**RES:** RES Receiver Error Status 0:0 0b RW1CS Physical layer receiver Error occurred. These errors include: elastic Buffer Collision, 8b/10b error, De-skew Timeout Error.
6	RO	0b	**BTLPS:** BTLPS Bad TLP Status 6:6 0b RW1CS
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.366 DMI.DMIESD_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/44h/

MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6b1db0)Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access	Default Value	Description
23:16	RWO	00000000b	**CID:** CID Component ID 23:16 00h RW-O Identifies the physical component that contains this Root Complex Element.
31:24	RO	00000001b	**PORTNUM:** PORTNUM Port Number 31:24 01h RO Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
3:0	RO	0010b	**ETYP:** ETYP Element Type 3:0 2h RO Indicates the type of the Root Complex Element. Value of 2h represents an Internal Root Complex Link (DMI
15:8	RO	00000010b	**NLE:** NLE Number of Link Entries 15:8 02h RO Indicates the number of link entries following the Element Self Description. This field reports 2 (one for MCH egress port to main memory and one to egress port belonging to ICH on other side of internal link).
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**

1.11.367 DMI.DMIETVM_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1b0h/
MMIO: Base/Offset:
IO: Base/Offset:
DOC .

Bit	Access	Default Value	Description
23:16	RW	11111111b	**VCPETVM:** #DMI_0_0_0.xml#- This is the upper 8 bits TC/VC mapping for VCp, and when combined with the DMIVCPRCTL forms a 16-bit TC/VC map using the TC[3:0] traffic class. ;
15:8	RW	00000000b	**VC1ETVM:** #DMI_0_0_0.xml#- This is the upper 8 bits TC/VC mapping for VC1, and when combined with the DMIVC1RCTL forms a 16-bit TC/VC map using the TC[3:0] traffic class. ;
7:0	RW	00000000b	**VC0ETVM:** #DMI_0_0_0.xml#- This is the upper 8 bits TC/VC mapping for VC0, and when combined with the DMIVC0CTL forms a 16-bit TC/VC map using the

Bit	Access	Default Value	Description
			TC[3:0] traffic class. ;
31:24	RO	00000000b	**VCMETVM:** #DMI_0_0_0.xml#- VCm Extended TC/VC Map (VCMETVM) ; #DMI_0_0_0.xml#-This is the upper 8 bits TC/VC mapping for VCm, and when combined with the DMIVCMRCTL forms a 16-bit TC/VC map using the TC[3:0] traffic class. ;

1.11.368 DMI.DMIPVCCAP1_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/4h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afa90)DMI Port VC Capability Register 1. Describes the configuration of PCI Express Virtual Channels associated with this port

Bit	Access	Default Value	Description
2:0	RWO	000b	**EVCC:** EVCC Extended VC Count 2:0 000b RW-O Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel, VC1 and the Manageability Virtual Channel are not included in this count.
6:4	RO	000b	**LPEVCC:** LPEVCC Low Priority Extended VC Count 6:4 000b RO Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO	0b	**RSVD3:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**

Bit	Access	Default Value	Description
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.369 DMI.DMIPVCCAP2_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/8h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afae0)DMI Port VC Capability Register 2. Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access	Default Value	Description
7:0	RO	00000000b	**VCAC:** VCAC Reserved for VC Arbitration Capability 7:0 00h RO
31:24	RO	00000000b	**VCATO:** VCATO Reserved for VC Arbitration Table Offset 31:24 00h RO
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**

Bit	Access	Default Value	Description
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**

1.11.370 DMI.DMIPVCCTL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afb40)DMI Port VC Control

Bit	Access	Default Value	Description
3:1	RW	000b	**VCAS:** VCAS VC Arbitration Select 3:1 000b RW This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 000b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field cannot be modified when more than one VC in the LPVC group is enabled. 000: Hardware fixed arbitration scheme. E.G. Round Robin Others: Reserved See the PCI express specification for more details.
0	RO	0b	**LVCAT:** LVCAT Reserved for Load VC Arbitration Table 0:0 0b RO
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**

Bit	Access	Default Value	Description
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.371 DMI.DMIRCILCECH_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/80h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6c2630)This capability contains controls for the Root Complex Internal Link known as DMI

Bit	Access	Default Value	Description
15:0	RO	0000000000000110b	**ECID:** ECID Extended Capability ID 15:0 0006h RO Value of 0006h identifies this linked list item (capability structure) as being for PCI Express Internal Link Control Capability
31:20	RO	000000000000b	**PNC:** PNC Pointer to Next Capability 31:20 000h RO This value terminates the PCI Express extended capabilities list associated with this RCRB. This field contains offset to the next PCI express capability structure in the linked list of capabilities (Root Complex Cache Capability)
19:16	RO	0001b	**LDCV:** LDCV Link Declaration Capability Version 19:16 1h RO Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.

1.11.372 DMI.DMIRCLDECH_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/40h/
MMIO: Base/Offset:

IO: Base/Offset:

HASH(0x6b1d40)This capability declares links from the respective element to other elements of the root complex component to which it belongs and to an element in another root complex component. See PCI Express specification for link/topology declaration requirements.

Bit	Access	Default Value	Description
15:0	RO	0000000000000101b	**ECID:** ECID Extended Capability ID 15:0 0005h RO Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability
31:20	RO	000010000000b	**PNC:** PNC Pointer to Next Capability 31:20 080h RO This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Internal Link Control Capability).
19:16	RO	0001b	**LDCV:** LDCV Link Declaration Capability Version 19:16 1h RO Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.

1.11.373 DMI.DMISSTSU_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/21ch/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
27:16	RO	000000000000b	**NTSN:** #DMI_0_0_0.xml#- Value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time. ;
11:0	RO	000000000000b	**NPSN:** #DMI_0_0_0.xml#- Packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link. ;
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.374 DMI.DMISSTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/218h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
11:0	RO	111111111111b	**LASN:** #DMI_0_0_0.xml#- This is the sequence number associated with the last acknowledged TLP. ;
27:16	RO	000000000000b	**NRSN:** #DMI_0_0_0.xml#- This is the sequence number associated with the TLP that is expected to be received next. ;
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.375 DMI.DMISTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/214h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6fae00)retry counters & link and lane status

Bit	Access	Default Value	Description
31:30	RO	00b	**RN:** RN Replay Number 31:30 00b RO-V Number of times the Retry Buffer has been replayed since the last Link initialization/retraining. When the Data Link Layer has replayed the contents of the Retry Buffer four times, a Link re-training will be initiated which will reset this value back to zero.
19:16	RO	0000b	**LKS:** LKS Link Status 19:16 0h RO-V During Link initialization the Link will always traverses this list of state from the top (0000b) to L0 (0111b). One or more power management states may be skipped, but the direction of list traversal will remain the same. 0000b Link Down 0001b Link in Training 0011b L1 0101b L2 0111b L0 (Link Up) 1000b L0s (Transmit & Receive) 1001b L0s (Transmit Only) 1010b L0s (Receive Only) All other encodings are reserved.

Bit	Access	Default Value	Description
15:0	RO	0000000000000000b	**LNS:** MOVED TO COMMON (gkamelo) LNS Lane Status 15:0 FFFFh RO-V Indicates which lanes are trained. A '1' indicates that the corresponding lane is trained (i.e. bit 0 = '1' means lane 0 is trained).
29	RO	0b	**DLLR:** DLLR Data Link Layer Retry 29:29 0b RO-V Indicates when the Data Link Layer has received a corrupted TLP or has detected a dropped packet and is currently waiting for the remote agent to re-transmit the corrupted/dropped packet. The value of Next Receive Sequence Number (DMISSTS, offset 218h [27:16]) will be the sequence number associated with the corrupted packet.
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**

1.11.376 DMI.DMITC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/204h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
19:15	RW	01111b	**UFCRTP:** #DMI_0_0_0.xml#- This field determines the number of symbol times the scheduled Updated Flow Control needs to wait before transmitting the updated flow control information to the other agent. ;
28	RW	0b	**IFCRT:** #DMI_0_0_0.xml#- Defines the amount of time the init flow control needs to wait before re-transmitting to the other agent (in order to avoid collisions). ;
27:20	RW	00001111b	**UFCRTNP:** #DMI_0_0_0.xml#- This field determines the number of symbol times the scheduled Updated Flow Control needs to wait before transmitting the updated flow control information to the other agent. ;
0	RO	0b	**RSVD0:**

Bit	Access	Default Value	Description
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.377 DMI.DMIUEMSK_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1c8h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f6b90)

Bit	Access	Default Value	Description
16	RW	0b	**UCM:** UCM Unexpected Completion Mask 16:16 0b RWS
20	RW	0b	**UREM:** UREM Unsupported Request Error Mask 20:20 0b RWS
17	RW	0b	**ROM:** ROM Receiver Overflow Mask 17:17 0b RWS
12	RW	0b	**PTLPM:** PTLPM Poisoned TLP Mask 12:12 0b RWS
4	RW	0b	**DLPEM:** DLPEM Data Link Protocol Error Mask 4:4 0b RWS
14	RW	0b	**CPLTM:** CPLTM Completion Timeout Mask 14:14 0b RWS
18	RW	0b	**MTLPM:** MTLPM Malformed TLP Mask 18:18 0b RWS
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**

Bit	Access	Default Value	Description
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
13	RO	0b	**RSVD13:**
15	RO	0b	**RSVD15:**
19	RO	0b	**RSVD19:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.378 DMI.DMIUESEV_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1cch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f6c30)Controls whether an individual error is reported as a non-fatal or fatal error. An error is reported as fatal when the corresponding error bit in the severity register is set. If the bit is cleared, the corresponding error is considered nonfatal.

Bit	Access	Default Value	Description
19	RO	0b	**ECRCES:** ECRCES Reserved for ECRC Error Severity 19:19

Bit	Access	Default Value	Description
			0b RO
15	RO	0b	**CAES:** CAES Reserved for Completer Abort Error Severity 15:15 0b RO
16	RW	0b	**UCES:** UCES Unexpected Completion Error Severity 16:16 0b RWS
4	RW	1b	**DLPES:** DLPES Data Link Protocol Error Severity 4:4 1b RWS
13	RO	0b	**FCPES:** FCPES Reserved for Flow Control Protocol Error Severity 13:13 0b RO
20	RW	0b	**URES:** URES Unsupported Request Error Severity 20:20 0b RWS
14	RW	0b	**CTES:** CTES Completion Timeout Error Severity 14:14 0b RWS
12	RW	0b	**PTLPES:** PTLPES Poisoned TLP Error Severity 12:12 0b RWS
17	RW	1b	**ROEV:** ROEV Receiver Overflow Error Severity 17:17 1b RWS
18	RW	1b	**MTLPES:** MTLPES Malformed TLP Error Severity 18:18 1b RWS
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

Bit	Access	Default Value	Description
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.379 DMI.DMIUESTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1c4h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6f6af0)This is an INTEL RESERVED register and should NOT be disclosed to customers. It is for test and debug purposes only and will not be included in external documentation.

Bit	Access	Default Value	Description
16	RO	0b	**UCS:** UCS Unexpected Completion Status 16:16 0b RW1CS
18	RO	0b	**MTLPS:** MTLPS Malformed TLP Status 18:18 0b RW1CS
12	RO	0b	**PTLPS:** PTLPS Poisoned TLP Status 12:12 0b RW1CS
17	RO	0b	**ROS:** ROS Receiver Overflow Status 17:17 0b RW1CS
20	RO	0b	**URES:** URES Unsupported Request Error Status 20:20 0b RW1CS
4	RO	0b	**DLPES:** DLPES Data Link Protocol Error Status 4:4 0b RW1CS
14	RO	0b	**CTS:** CTS Completion Timeout Status 14:14 0b RW1CS
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
13	RO	0b	**RSVD13:**
15	RO	0b	**RSVD15:**
19	RO	0b	**RSVD19:**
21	RO	0b	**RSVD21:**

Bit	Access	Default Value	Description
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.380 DMI.DMIVC0CCC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/318h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d5010) Total number of flow control units consumed by the local agent since initialization. These values are incremented when the Transaction Layer commits to sending information on the Link Layer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express

Bit	Access	Default Value	Description
11:0	RO	000000000000b	**CCCD:** CCCD DMIVC0CCC Data 11:0 000h RW-V
23:16	RO	00000000b	**CCCH:** CCCH DMIVC0CCC Header 23:16 00h RW-V
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.381 DMI.DMIVC0CCL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/31ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d5060)

Bit	Access	Default Value	Description
23:16	RO	00000000b	**CCLH:** CCLH DMIVC0CCL Header 23:16 00h RO-V
11:0	RO	000000000000b	**CCLD:** CCLD DMIVC0CCL Data 11:0 000h RO-V
31	RO	0b	**ICRH:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- 0 - Not infinite credit received ; /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main-1 - Infinite credit received ;
15	RO	0b	**ICRD:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- 0 - Not infinite credit received ; /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main-1 - Infinite credit received ;
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**

1.11.382 DMI.DMIVC0NPRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/314h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d4fc0) Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. For testing purposes a value can be written into this register that will be read only one time, when the PCI Express functionality is initialize

Bit	Access	Default Value	Description
22:16	RWO	0001100b	**NPRCALH:** NPRCALH DMIVC0NPRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register defines the non-posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is in L0 state.
23	RO	0b	**NPRCAHH:** NPRCAHH DMIVC0NPRCA High Header 23:23 0h RO Reserved
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.383 DMI.DMIVC0NPRCC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/30ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d4f00)

Bit	Access	Default Value	Description
23:16	RO	00000000b	**NPRCCH:** NPRCCH DMIVC0NPRCC Header 23:16 00h RW-V
11:0	RO	000000000000b	**NPRCCD:** NPRCCD DMIVC0NPRCC Data 11:0 000h RW-V
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.384 DMI.DMIVC0NPRCL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/310h/
MMIO: Base/Offset:
IO: Base/Offset:

Contains the limit for maximum number of flow control units which may be consumed by the local agent. Set to the value indicated in the Flow Control Packet upon receipt, which reflects the available space in the remote receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express

Bit	Access	Default Value	Description
23:16	RO	00000000b	**NPRCLH:** NPRCLH DMIVC0NPRCL Header 23:16 00h RO-V
11:0	RO	000000000000b	**NPRCLD:** NPRCLD DMIVC0NPRCL Data 11:0 000h RO-V
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**

Bit	Access	Default Value	Description
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.385 DMI.DMIVC0PRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/308h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d4e90) Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification

Bit	Access	Default Value	Description
23	RO	0b	**PRCAHH:** PRCAHH DMIVC0PRCA High Header 23:23 0h RO Reserved
22:16	RWO	0001100b	**PRCALH:** PRCALH DMIVC0PRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register defines the posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is in L0 state.
7:0	RWO	01000000b	**PRCALD:** PRCALD DMIVC0PRCA Low Data 7:0 40h RW-O 16 CL in data queue * 64B/CL * 1 FCU/16B =64 FCU (Flow Control Units). Write, allowed only once, to this register defines the posted data credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is in L0 state.
11:8	RO	0000b	**PRCAHD:** PRCAHD DMIVC0PRCA High Data 11:8 0h RO Reserved
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**

Bit	Access	Default Value	Description
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.386 DMI.DMIVC0PRCC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/300h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d4dd0)Total number of flow control units consumed by the local agent since initialization. These values are incremented when the Transaction Layer commits to sending information on the Link Layer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express

Bit	Access	Default Value	Description
23:16	RO	00000000b	**PRCCH:** PRCCH DMIVC0PRCC Header 23:16 00h RW-V
11:0	RO	000000000000b	**PRCCD:** PRCCD DMIVC0PRCC Data 11:0 000h RW-V
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.387 DMI.DMIVC0PRCL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/304h/
MMIO: Base/Offset:

IO: Base/Offset:

HASH(0x6d4e20)Contains the limit for maximum number of flow control units which may be consumed by the local agent. Set to the value indicated in the Flow Control Packet upon receipt, which reflects the available space in the remote receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. When reading the PCI Express

Bit	Access	Default Value	Description
23:16	RO	00000000b	**PRCLH:** PRCLH DMIVC0PRCL Header 23:16 00h RO-V
11:0	RO	000000000000b	**PRCLD:** PRCLD DMIVC0PRCL Data 11:0 000h RO-V
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.388 DMI.DMIVC0RCAP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/10h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afba0)DMI VC0 Resource Capability

Bit	Access	Default Value	Description
31:24	RO	00000000b	**PATO:** PATO Reserved for Port Arbitration Table Offset 31:24 00h RO
22:16	RO	0000000b	**MTS:** MTS Reserved for Maximum Time Slots 22:16 00h RO
15	RO	0b	**REJSNPT:** REJSNPT Reject Snoop Transactions 15:15 1b RO 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
7:0	RO	00000001b	**PAC:** PAC Port Arbitration Capability 7:0 01h RO Having

Bit	Access	Default Value	Description
			only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
23	RO	0b	**RSVD23:**

1.11.389 DMI.DMIVC0RCTL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/14h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
31	RO	1b	**VC0E:** #DMI_0_0_0.xml#- For VC0 this is hardwired to 1 and read only as VC0 can never be disabled. ;
6:1	RW	111111b	**TCVC0M:** #DMI_0_0_0.xml#- Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. ; #DMI_0_0_0.xml#-For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. ;
19:17	RW	000b	**PAS:** #DMI_0_0_0.xml#- Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted. ; #DMI_0_0_0.xml#-This field will always be programmed to '1'. ;
26:24	RO	000b	**VC0ID:** #DMI_0_0_0.xml#- Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only. ;
0	RO	1b	**TC0VC0M:** #DMI_0_0_0.xml#- Traffic Class 0 is always routed to VC0. ;
7	RO	0b	**TCMVC0M:** #DMI_0_0_0.xml#- ;

Bit	Access	Default Value	Description
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**

1.11.390 DMI.DMIVC0RSTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1ah/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afcc0)DMI VC0 Resource Status

Bit	Access	Default Value	Description
17	RO	1b	**VC0NP:** VC0NP Virtual Channel 0 Negotiation Pending 1:1 1b RO-V 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state.
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**

Bit	Access	Default Value	Description
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.391 DMI.DMIVC1NPRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/330h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d5220)DMI VCm Non-Posted Request Credits Allocated

Bit	Access	Default Value	Description
22:16	RWO	0001100b	**NPRCALH:** NPRCALH DMIVC1NPRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register

Bit	Access	Default Value	Description
			defines the non-posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is in L0 state.
23	RO	0b	**NPRCAHH:** NPRCAHH DMIVC1NPRCA High Header 23:23 0h RO Reserved
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.392 DMI.DMIVC1PRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/32ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d51b0)DMI VC1 Posted Request Credits Allocated

Bit	Access	Default Value	Description
23	RO	0b	**PRCAHH:** PRCAHH DMIVC1PRCA High Header 23:23 0h RO Reserved
22:16	RWO	0001100b	**PRCALH:** PRCALH DMIVC1PRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register defines the posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is in L0 state.
7:0	RWO	00101000b	**PRCALD:** PRCALD DMIVC1PRCA Low Data 7:0 28h RW-O 10 CL in data queue * 64B/CL * 1 FCU/16B = 40 FCU (Flow Control Units). Write, allowed only once, to this register defines the posted data credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is in L0 state.
11:8	RO	0000b	**PRCAHD:** PRCAHD DMIVC1PRCA High Data 11:8 0h RO Reserved
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.393 DMI.DMIVC1RCAP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afd20)DMI VC1 Resource Capability

Bit	Access	Default Value	Description
31:24	RO	00000000b	**PATO:** PATO Reserved for Port Arbitration Table Offset 31:24 00h RO
22:16	RO	0000000b	**MTS:** MTS Reserved for Maximum Time Slots 22:16 00h RO
15	RO	1b	**REJSNPT:** REJSNPT Reject Snoop Transactions 15:15 0b RO 0: Transactions with or without the No Snoop bit set within the

Bit	Access	Default Value	Description
			TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
7:0	RO	00000001b	**PAC:** PAC Reserved for Port Arbitration Capability 7:0 01h RO
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
23	RO	0b	**RSVD23:**

1.11.394 DMI.DMIVC1RCTL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/20h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
31	RW	0b	**VC1E:** #DMI_0_0_0.xml#- 0: Virtual Channel is disabled. ;
6:1	RW	000000b	**TCVC1M:** #DMI_0_0_0.xml#- Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. ; #DMI_0_0_0.xml#-For example, when bit 6 is set in this field, TC6 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. ;
26:24	RW	001b	**VC1ID:** #DMI_0_0_0.xml#- Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled. ;
0	RO	0b	**TC0VC1M:** #DMI_0_0_0.xml#- Traffic Class 0 is always routed to VC0. ;
19:17	RW	000b	**PAS:** #DMI_0_0_0.xml#- Configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. ; #DMI_0_0_0.xml#-Only 001b encoding is valid

Bit	Access	Default Value	Description
			;
7	RO	0b	**TCMVC1M:** #DMI_0_0_0.xml#- ;
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**

1.11.395 DMI.DMIVC1RSTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/26h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6b1a70)DMI VC1 Resource Status

Bit	Access	Default Value	Description
17	RO	1b	**VC1NP:** VC1NP Virtual Channel 1 Negotiation Pending 1:1 1b RO-V 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
1:0	RO	00b	**RSVD0:**

Bit	Access	Default Value	Description
1	RO	00b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.396 DMI.DMIVCECH_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/0h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6afa30)Indicates DMI Virtual Channel capabilities.

Bit	Access	Default Value	Description
19:16	RO	0001b	**PCIEVCCV:** PCIEVCCV PCI Express Virtual Channel Capability Version 19:16 1h RO Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification. Note: This version does not change for 2.0 compliance.
15:0	RO	0000000000000010b	**ECID:** ECID Extended Capability ID 15:0 0002h RO Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.
31:20	RO	000001000000b	**PNC:** PNC Pointer to Next Capability 31:20 040h RO This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).

1.11.397 DMI.DMIVCMNPRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/348h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d53a0)DMI VCm Non-Posted Request Credits Allocated

Bit	Access	Default Value	Description
22:16	RWO	0001011b	**NPRCALH:** NPRCALH DMIVCMNPRCA Low Header 22:16 0Bh RW-O Write, allowed only once, to this register defines the non-posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is up.
23	RO	0b	**NPRCAHH:** NPRCAHH DMIVCMNPRCA High Header 23:23 0h RO Reserved
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**

Bit	Access	Default Value	Description
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.398 DMI.DMIVCMPRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/344h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d5330)DMI VCm Posted Request Credits Allocated

Bit	Access	Default Value	Description
23	RO	0b	**PRCAHH:** PRCAHH DMIVCMPRCA High Header 23:23 0h RO Reserved
22:16	RWO	0001100b	**PRCALH:** PRCALH DMIVCMPRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register defines the posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is up.
7:0	RWO	00101000b	**PRCALD:** PRCALD DMIVCMPRCA Low Data 7:0 28h RW-O 10 CL in data queue * 64B/CL * 1 FCU/16B = 40 FCU (Flow Control Units). Write, allowed only once, to this register defines the posted data credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is up
11:8	RO	0000b	**PRCAHD:** PRCAHD DMIVCMPRCA High Data 11:8 0h RO Reserved
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**

Bit	Access	Default Value	Description
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.399 DMI.DMIVCMRCAP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/34h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6b1c20)DMI VCm Resource Capability

Bit	Access	Default Value	Description
15	RO	1b	**REJSNPT:** REJSNPT Reject Snoop Transactions 15:15 1b RO 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on the VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**

Bit	Access	Default Value	Description
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.400 DMI.DMIVCMRCTL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/38h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
31	RW	0b	**VCMEN:** #DMI_0_0_0.xml#- 0: Virtual Channel is disabled. ;
26:24	RW	111b	**VCID:** #DMI_0_0_0.xml#- Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled. ;
7:0	RO	10000000b	**TCVCMMAP:** #DMI_0_0_0.xml#- Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. ; #DMI_0_0_0.xml#-For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link. ;

Bit	Access	Default Value	Description
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**

1.11.401 DMI.DMIVCMRSTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/3eh/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6b1cf0)DMI VCM Resource Status

Bit	Access	Default Value	Description
17	RO	1b	**VCNEGPND:** VCNEGPND Virtual Channel Negotiation

Bit	Access	Default Value	Description
			Pending 1:1 1b RO-V 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
1:0	RO	00b	**RSVD0:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**

Bit	Access	Default Value	Description
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.402 DMI.DMIVCPNPRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/338h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d52e0)Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. For testing purposes a value can be written into this register that will be read only one time, when the PCI Express functionality is initialized. After that this register can only be used for reading the current value. When reading the PCI Express

Bit	Access	Default Value	Description
22:16	RWO	0001100b	**NPRCALH:** NPRCALH DMIVCPNPRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register defines the non-posted header credits advertised to the remote agent during flow control initialization. Reads to this register will return the current value of the corresponding bits of non-posted header credits allocated pointer. The default value of the register will become valid after the link is in L0 state.
23	RO	0b	**NPRCAHH:** NPRCAHH DMIVCPNPRCA High Header 23:23 0h RO Reads to this register will return the current value of the corresponding bits of non-posted header credits allocated pointer.
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**

Bit	Access	Default Value	Description
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.403 DMI.DMIVCPPRCA_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/334h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d5270)DMI VCp Posted Request Credits Allocated . Total number of flow control credits granted to the Transmitter since initialization. Initially set according to the local receive buffer size and allocation policies. These values are incremented as the Receiver Transaction Layer removes processed information from its receive buffer. Flow control credits are communicated and tracked according to the rules in the PCI Express specification. For testing purposes a value can be written into this register that will be read only one time, when the PCI Express functionality is initialized

Bit	Access	Default Value	Description
23	RO	0b	**PRCAHH:** PRCAHH DMIVCPPRCA High Header 23:23 0h RO Reserved
22:16	RWO	0001100b	**PRCALH:** PRCALH DMIVCPPRCA Low Header 22:16 0Ch RW-O Write, allowed only once, to this register defines the posted header credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is up.
7:0	RWO	00101000b	**PRCALD:** PRCALD DMIVCPPRCA Low Data 7:0 28h RW-O 10 CL in data queue * 64B/CL * 1 FCU/16B = 40 FCU (Flow Control Units). Write, allowed only once, to this register defines the posted data credits advertised to the remote agent during flow control initialization. The default value of the register will become valid after the link is up.

Bit	Access	Default Value	Description
11:8	RO	0000b	**PRCAHD:** PRCAHD DMIVCPPRCA High Data 11:8 0h RO Reserved
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.404 DMI.DMIVCPRCAP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/28h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6b1ac0)DMI VCp Resource Capability

Bit	Access	Default Value	Description
31:24	RO	00000000b	**PATO:** PATO Reserved for Port Arbitration Table Offset 31:24 00h RO
22:16	RO	0000000b	**MTS:** MTS Reserved for Maximum Time Slots 22:16 00h RO
15	RO	0b	**REJSNPT:** REJSNPT Reject Snoop Transactions 15:15 0b RO 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: When Set, any transaction for which the No Snoop attribute is applicable but is not Set within the TLP Header will be rejected as an Unsupported Request.
7:0	RO	00000001b	**PAC:** PAC Reserved for Port Arbitration Capability 7:0 01h RO
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**

Bit	Access	Default Value	Description
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
23	RO	0b	**RSVD23:**

1.11.405 DMI.DMIVCPRCTL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/2ch/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
7	RO	0b	**TCMVCPM:** #DMI_0_0_0.xml#- ;
6:1	RW	000000b	**TCVCPM:** #DMI_0_0_0.xml#- It is recommended that private TC6 (01000000b) is the only value that should be programmed into this field for VCp traffic which will be translated by a virtualization engine, and TC2 (00000010b) is the only value that should be programmed into this field for VCp traffic which will not be translated by a virtualization engine. This strategy can simplify debug and limit validation permutations. ;
27:24	RW	1010b	**VCPID:** #DMI_0_0_0.xml#- Assigns a VC ID to the VC resource. This field cannot be modified when the VC is already enabled. No private VCs are precluded by hardware and private VC handling is implemented the same way as non-private VC handling. ; #DMI_0_0_0.xml#-However, to limit validation permutations the only private VC that is being validated is private VC6 (110b) and is the only value that should be programmed into this field. ;
0	RW	0b	**TC0VCPM:** #DMI_0_0_0.xml#- ;
31	RW	0b	**VCPE:** #DMI_0_0_0.xml#- 0: Virtual Channel is disabled. ;
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**

Bit	Access	Default Value	Description
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**

1.11.406 DMI.DMIVCPRSTS_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/32h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6b1bd0)DMI VCP Resource Status

Bit	Access	Default Value	Description
17	RO	1b	**VCPNP:** VCPNP Virtual Channel private Negotiation Pending 1:1 1b RO-V 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
1:0	RO	00b	**RSVD0:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**

Bit	Access	Default Value	Description
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.407 DMI.ECOBNSTLLL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1f8h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
14	RW	0b	**BLKC_BUGFIX1810265:**
21:16	RW	000000b	**RSVD2116:**
22	RW	0b	**RSVD22:**
25:23	RW	000b	**RSVD2325:**
27	RW	1b	**RSVD27:**

Bit	Access	Default Value	Description
26	RW	1b	**RSVD26:**
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RW	0b	**RSVD7:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/pcie_creg.xml-
8	RO	0b	**RSVD8:**
9	RW	0b	**RSVD9:**
10	RW	0b	**RSVD10:**
11	RW	0b	**RSVD11:**
12	RW	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
15	RO	0b	**RSVD15:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.408 DMI.ECOBNS_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/1fch/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
12	RO	0b	**RSVD12:**
18	RW	0b	**HOTRST_TIMEOUT_SEL:**
10	RO	0b	**RSVD10:**
22	RO	0b	**RSVD22:**
11	RO	0b	**RSVD11:**
29	RO	1b	**RSVD29:**
20	RW	0b	**L2ENTRY_WAITLINKIDLE_QEMPTY:**
8	RW	0b	**GDEN:**

Bit	Access	Default Value	Description
16	RW	0b	**RXON_STATEDRIVEN:**
30	RW	1b	**SQUELCH_DET_EN_L0:**
28	RW	1b	**TXL0SDIS_IN_RECOV:**
17	RW	0b	**RXL0S_BLOCK_KALIGNRST:**
19	RW	0b	**L2ENTRY_WAITLINKEMPTY:**
27	RO	1b	**RSVD27:**
7	RO	0b	**RSVD7:**
26	RO	1b	**RSVD26:**
9	RO	0b	**RSVD9:**
25:23	RO	000b	**RSVD2325:**
21	RO	0b	**RSVD21:**
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
31	RO	0b	**RSVD31:**

1.11.409 DMI.FCLKGTTLLL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d24h/
MMIO: Base/Offset:
IO: Base/Offset:

does not affect rtl

Bit	Access	Default Value	Description
9	RW	0b	**CQCGD:** pci_dmi.xml- Disable Clock gating for Downstream completion queue ; pci_dmi.xml-0 - Enabled (Default) ;
1	RW	0b	**SRAMCGCTL:** pci_dmi.xml- This bit controls the turning on/off the clock gating mechanism at the SRAM EBBs in the TL. ;
2	RW	0b	**DIS_CLKGAT_FCLK:** pci_dmi.xml- 0b: Enable dynamic

Bit	Access	Default Value	Description
			clock gating ; pci_dmi.xml-1b: Disable dynamic clock gating ;
0	RO	0b	**RSVD0:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- Reserved ;
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.410 DMI.FUSESCMN_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/504h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
17:16	RO	00b	**PEG1CFGSEL:** #MMR_0_1_0.xml#- This field defines device 1 port split ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

Bit	Access	Default Value	Description
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.411 DMI.L0SLAT_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/22ch/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6fb030)This register controls L0s Exit Latency for both Common and Non-Common clock configurations.

Bit	Access	Default Value	Description
30:24	RW	0000000b	**ANFTSOFF:** ANFTSOFF Adaptive N_FTS Offset 30:24 0000000b RW-V The amount by which the Adaptive N_FTS mechanism has increased the Receiver's advertised N_FTS value relative to the initial value specified in this register.
31	RW	0b	**ANFTSEN:** ANFTSEN Adaptive N_FTS Enable 31:31 0b RW Allows the advertised N_FTS value to increment automatically if the specified value does not result in a successful L0s Exit at least 90% of the time. 0: Adaptive N_FTS Disabled. Adaptive N_FTS Offset field is cleared. 1: Adaptive N_FTS Enabled. If L0s Exit times out to Recovery more often than once out of every 16 attempts, then increment the Adaptive N_FTS Offset field. That Adaptive N_FTS Offset field should be added to the correct initial N_FTS value based on the state of the Common Clock Configuration bit. The offset is limited such that it will not exceed the current initial value, and will not result in a sum that exceeds FFh.
15:8	RW	00101000b	**CCNFTSGEN2:** NCCNFTS Non-Common Clock N_FTS 15:8 32h RW Number of Fast Training Sequence ordered sets required to be transmitted for the root port's Receiver to exit L0s in a non common clock configuration (LCTL[6]=0). The N_FTS value is sent in TS1 and TS2 training sets during link training. 00: 0 FTS sets 01: 1 FTS set ... FF: 255 FTS sets
7:0	RW	00010111b	**CCNFTSGEN1:** CCNFTS Common Clock N_FTS 7:0 28h RW Number of Fast Training Sequence ordered sets required to be transmitted for the root port's Receiver to exit L0s in a common clock configuration (LCTL[6]=1). The N_FTS value is sent in TS1 and TS2 training sets during link training. 00h: 0 FTS sets 01h: 1 FTS set ... FFh: 255 FTS sets
22:20	RW	100b	**NCCLKL0EL:** NCCLKL0EL Non-Common Clock L0s Exit Latency 22:20 100b RW The L0s Exit Latency reported in the Link Capability register for non Common Clock Configurations (LCTL[6]=0). 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less

Bit	Access	Default Value	Description
			than 1 us 101: 1 us to less than 2 us 110: 2 us-4 us 111: More than 4 us
18:16	RW	010b	**CCL0EL:** CCL0EL Common Clock L0s Exit Latency 18:16 010b RW The L0s Exit Latency reported in the Link Capability register for Common Clock Configurations (LCTL[6]=1). 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 us 101: 1 us to less than 2 us 110: 2 us-4 us 111: More than 4 us
19	RO	0b	**RSVD19:**
23	RO	0b	**RSVD23:**

1.11.412 DMI.LCAP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/84h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
3:0	RW	0001b	**MLS:** #DMI_0_0_0.xml#- This default value reflects gen1. ;
17:15	RW	010b	**L1SELAT:** #DMI_0_0_0.xml#- Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010b indicates the range of 2 us to less than 4 us. ;
11:10	RO	11b	**ASLPMS:** #DMI_0_0_0.xml#- L0s & L1 entry supported. ;
14:12	RW	010b	**L0SELAT:** #DMI_0_0_0.xml#- Indicates the length of time this Port requires to complete the transition from L0s to L0. ;
9:4	RO	000100b	**MLW:** #DMI_0_0_0.xml#- Indicates the maximum number of lanes supported for this link. ;
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**

Bit	Access	Default Value	Description
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.413 DMI.LCTL2_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/98h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
9:7	RW	000b	**TXMARGIN:**
6	RW	0b	**SELECTABLEDEEMPHASIS:**
3:0	RW	0010b	**TLS:** pci_dmi.xml- For Downstream ports, this field sets an upper limit on link operational speed by restricting the values advertised by the upstream component in its training sequences. ;
4	RW	0b	**EC:** pci_dmi.xml- Software is permitted to force a link to enter Compliance mode at the speed indicated in the Target Link Speed field by setting this bit to 1b in both components on a link and then initiating a hot reset on the link. ;
5	RW	0b	**HASD:** pci_dmi.xml- When set to 1b this bit disables hardware from changing the link speed for reasons other than attempting to correct unreliable link operation by reducing link speed. ;
10	RW	0b	**ENTERMODCOMPLIANCE:**
11	RW	0b	**COMPSOS:**
12	RW	0b	**COMPLIANCEDEEMPHASIS:**
13	RW	1b	**TXSWING:** from a fuse
16	RO	0b	**CURDELVL:** Current De-emphasis Level - When the Link is operating at 5 GT/s speed, this reflects the level of de-emphasis. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, this bit is 0b.
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**

Bit	Access	Default Value	Description
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.414 DMI.LCTL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/88h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6de4f0)Allows control of PCI Express link.

Bit	Access	Default Value	Description
5	RO	0b	**RL:** RL Retrain Link 5:5 0b RW-V 0: Normal operation. 1: Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
7	RW	0b	**ES:** ES Extended Synch 7:7 0b RW Extended synch 0: Standard Fast Training Sequence (FTS). 1: Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
9	RW	0b	**HAWD:** HAWD Hardware Autonomous Width Disable 9:9 0b RW Hardware Autonomous Width Disable - When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Devices that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b.
1:0	RW	00b	**ASPM:** ASPM Active State PM 1:0 00b RW Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: Reserved 11: L0s and L1 Entry Supported ASPM L0s Entry Policy This field provides for selective enabling of ASPM L0s

Bit	Access	Default Value	Description
			depending on C state. 0b - (Default): ASPM L0s enabled for all states. 1b - ASPM L0s enabled only in C2 state Note: Irrespective of the programming in this field, the final control is provided by the link control register
25:20	RO	000000b	**NWID:** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states ; (after link width negotiation is successfully completed). ; ; 00h: Reserved ; 01h: X1 ; 02h: X2 ; 04h: X4 ; ; All other encodings are reserved. ;
27	RO	0b	**LTRN:** pci_dmi.xml- Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete. ;
19:16	RO	0001b	**NSPD:** #DMI_0_0_0.xml#- Indicates negotiated link speed. ;
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
6	RO	0b	**RSVD6:**
8	RO	0b	**RSVD8:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
26	RO	0b	**RSVD26:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.415 DMI.LFSRSTS_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d80h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
31:16	RW	0000000000000000b	**TXLFSR:** left shift register used for scrambler
15:0	RW	0000000000000000b	**RXLFSR:** left shift register used for de-scrambler

1.11.416 DMI.LLTC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/238h/
MMIO: Base/Offset:
IO: Base/Offset:

DOC .

Bit	Access	Default Value	Description
10:0	RO	00100111111b	**RT:** #DMI_0_0_0.xml#- Determines how many symbol times (i.e. number of Lclk cycles) the Data Link Layer will wait to replay the contents of the Retry Buffer if a valid Ack/Nak DLLP is not received. ;
23:16	RO	00001000b	**ATL:** Minimum number of symbol times (i.e. number of Lclk cycles) the Data Link Layer will wait between successfully receiving a TLP and when the Data Link Layer generates and schedules an Ack DLLP to be sent to the remote agent. This counter is bypassed when Opportunistic Acknowledge Transmission is enabled (0F0h[4] = '0'), or the transmit side of the Link is in L0s.The default for this register is dependent on the MAX_PAYLOAD_SIZE (128B) and the NEGOTIATED_WIDTH. ; ; The default values for this field that are in the PCI Express ?? specification only consider the pin to pin latency. The default values below take into account the HW latencies of receiving a TLP and transmitting an Ack DLLP that is stalled behind a maximum sized TLP (84B) and a SKIP ordered-set (4 symbol times) to satisfy the PCI Express (pin to pin) guidelines for acknowledge latency. ; Width x1 x2 x4 x8 x16 (Gen1 Speed) ; Default 64 20 08 20 09 (symbol times in decimal) ; Default 40 14 08 14 09 (symbol times in hexadecimal) ; Width x1 x2 x4 x8 x16 (Gen2 Speed) ; Default 115 71 59 71 60 (symbol times in decimal) ; Default 73 47 3B 47 3C (symbol times in hexadecimal) ; Only recommended settings should be programmed into this field. Programming values outside the recommended range can result in erroneous behavior. ; The value in this field should always be greater than 0. ;
29	RW	0b	**ERT:** #DMI_0_0_0.xml#- Extended replay time ;
31	RW	0b	**ATLOE:** ATLOE Ack Transmission Latency Override Enable 31:31 0b RW ; 0 - Normal operation Ack Transmission Latency defined by HW ; 1 - Override enable. Ack Transmission Latency defined by ATL field ;
30	RW	0b	**RTOE:** RTOE Replay Timer Override Enable 30:30 0b

Bit	Access	Default Value	Description
			RW ; '0' : Default. HW defined Replay timeout ; '1': Override enable. SW written RT field defines the replay timeout. ;
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**

1.11.417 DMI.LSTS2_0_1_0_PCI

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d2h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RO	0b	**CURDELVL:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- Current De-emphasis Level - When the Link is operating at 5 GT/s speed, this reflects the level of de-emphasis. ;
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**

Bit	Access	Default Value	Description
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.418 DMI.LTSSMC_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/224h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
1	RW	1b	**X2LWS:** #DMI_0_0_0.xml#- 0: Not Supported. Prevents link width negotiation at this width and also disables receiver termination for logical lane 1 if all higher link widths are also not supported. ;
3	RO	0b	**X8LWS:** #DMI_0_0_0.xml#- 0: Not Supported. Prevents link width negotiation at this width and also disables receiver termination for logical lanes 7:4 if higher link widths are also not supported. ;
11	RW	0b	**SKPDISALWY:** #DMI_0_0_0.xml#- SKP Generation Completely Disabled: SKP generation will be disabled at all times. ;
20:16	RW	00000b	**PHYLAT:** #DMI_0_0_0.xml#- Configurable delay from when the squelch entry request. is received to when the AFE sequence to put the bus into squelch begins. This delay is due to the latency in the PHY. Needed to allow the transmitted data (prior clocks) to reach the other side

Bit	Access	Default Value	Description
			before shutting off the bus. ;
0	RO	1b	**X1LWS:** #DMI_0_0_0.xml#- 0: Not Supported. Prevents link width negotiation at this width and also disables receiver termination for logical lane 0 if all higher link widths are also not supported. ;
10	RW	0b	**SKPDIS:** #DMI_0_0_0.xml#- SKP Generation disabled in certain LTSSM states. ;
4	RO	0b	**X16LWS:** #DMI_0_0_0.xml#- 0: Not Supported. Prevents link width negotiation at this width and also disables receiver termination for logical lanes 15:8. ;
2	RW	1b	**X4LWS:** #DMI_0_0_0.xml#- 0: Not Supported. Prevents link width negotiation at this width and also disables receiver termination for logical lanes 3:2 if all higher link widths are also not supported. ;
8	RW	0b	**BDQDQ:** #DMI_0_0_0.xml#- 0: Allow transition (Normal Operation) ;
9	RW	0b	**BPAPC:** #DMI_0_0_0.xml#- 0: Allow transition (Normal Operation) ; #DMI_0_0_0.xml#- Note that this bit has no effect unless the LTSSM is in the Polling. Active state. It will not force the LTSSM into Polling. Active from any other state. Typically a Warm Reset of the platform is required after this bit is set. ;
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.419 DMI.NEGSTS_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d78h/
MMIO: Base/Offset:
IO: Base/Offset:

Negotiation Status - expose the value of the partner speed/scramble/emphasis/N_FTS request

Bit	Access	Default Value	Description
13	RO	0b	**LPUPCFGE:** #MMR_0_1_0.xml#- This register expose the value of Upconfig enable reported by the link partner ;
8	RO	0b	**LPDEMP:** #MMR_0_1_0.xml#- This register expose the value of de-emphasis requested by the link partner ;
7:0	RO	00000000b	**LPN_FTS:** #MMR_0_1_0.xml#- This register expose the value of N_FTS requested by the link partner ;
9	RO	0b	**LPSE:** #MMR_0_1_0.xml#- This register expose the value of scramble enable requested by the link partner ;
11:10	RO	00b	**LPSSPD:** #MMR_0_1_0.xml#- This register expose the value of supported speed requested by the link partner ;
12	RO	0b	**RSVD12:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.420 DMI.PCLKGTTLLL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d28h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
1	RW	0b	**DIS_CLKGAT_PCLK:**
2	RW	0b	**SRAMCGCLL:**
0	RW	0b	**DIS_CLKGAT_FCLK:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

Bit	Access	Default Value	Description
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.421 DMI.PEGBDWTHCHGTO_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/4bch/
MMIO: Base/Offset:
IO: Base/Offset:

PEG should be removed

Bit	Access	Default Value	Description
7:0	RW	11001000b	**WDHCHGTMOUT:** #MMR_0_1_0.xml#- Indicates the number of ms that we must wait upon a failed root port-initiated link width change before we are permitted to initiate another link width change. ; #MMR_0_1_0.xml#-Default: C8h (200ms) ;
15:8	RW	11001000b	**SPDCHGTMOUT:** #MMR_0_1_0.xml#- Indicates the number of ms that we must wait upon a failed root port-initiated speed change before we are permitted to initiate another speed change. ; #MMR_0_1_0.xml#-Default: C8h (200ms) ;
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.422 DMI.PEGCLKGTCMN_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d2ch/
MMIO: Base/Offset:
IO: Base/Offset:

PEG relate should be removed

Bit	Access	Default Value	Description
30	RW	0b	**MSGCHPCLKGTOVR:**
31	RW	0b	**GIGPGLBCLKGTDIS:** #MMR_0_1_0.xml#- This bit controls clock gating for GI/GP global logic (logic that is not per lane). ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**

Bit	Access	Default Value	Description
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

1.11.423 DMI.PEGCOMLCGCTRL_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d20h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
30	RW	0b	**PRVTEXTDETQ:** #MMR_0_1_0.xml#- This bit prevents PEG0 LTSSM from exiting Detect. Quiet state. ;
31	RO	0b	**LTSSMDETQ:** #MMR_0_1_0.xml#- This bit is set once Prevent PEG0 LTSSM From Exiting Detect. Quiet bit is set (1b) and PEG LTSSM is in Detect. Quiet state. ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**

Bit	Access	Default Value	Description
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**

1.11.424 DMI.PEGINITLCGCTR_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d1ch/
MMIO: Base/Offset:
IO: Base/Offset:

PEG should be removed

Bit	Access	Default Value	Description
6	RW	1b	**LGCGLNKSTPLY:** #MMR_0_1_0.xml#- Reserved ;
5:0	RW	000000b	**ILCGSETTMR:** #MMR_0_1_0.xml#- Reserved ;
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**

Bit	Access	Default Value	Description
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.425 DMI.PEGLATFIXCTL_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d38h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
5	RW	0b	**ARMLATFIX:**
6	RO	0b	**LATFIXFAIL:**
7	RO	0b	**LATFIXDONE:**
4:0	RW	00000b	**PXPRXLAT:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**

Bit	Access	Default Value	Description
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.426 DMI.PEGSQSTAT_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d08h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
9	RO	0b	**SQSTAT9:** #MMR_0_1_0.xml#- Squelch Status - Lane 9 (sqstat9) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
14	RO	0b	**SQSTAT14:** #MMR_0_1_0.xml#- Squelch Status - Lane 14 (sqstat14) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
10	RO	0b	**SQSTAT10:** #MMR_0_1_0.xml#- Squelch Status - Lane 10 (sqstat10) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
1	RO	0b	**SQSTAT1:** #MMR_0_1_0.xml#- Squelch Status - Lane 1 (sqstat1) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
2	RO	0b	**SQSTAT2:** #MMR_0_1_0.xml#- Squelch Status - Lane 2 (sqstat2) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
15	RO	0b	**SQSTAT15:** #MMR_0_1_0.xml#- Squelch Status - Lane 15 (sqstat15) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
16	RW	0b	**PEGSQSTATEN:**

Bit	Access	Default Value	Description
5	RO	0b	**SQSTAT5:** #MMR_0_1_0.xml#- Squelch Status - Lane 5 (sqstat5) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
7	RO	0b	**SQSTAT7:** #MMR_0_1_0.xml#- Squelch Status - Lane 7 (sqstat7) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
4	RO	0b	**SQSTAT4:** #MMR_0_1_0.xml#- Squelch Status - Lane 4 (sqstat4) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
12	RO	0b	**SQSTAT12:** #MMR_0_1_0.xml#- Squelch Status - Lane 12 (sqstat12) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
0	RO	0b	**SQSTAT0:** #MMR_0_1_0.xml#- Squelch Status - Lane 0 (sqstat0) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
3	RO	0b	**SQSTAT3:** #MMR_0_1_0.xml#- Squelch Status - Lane 3 (sqstat3) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
6	RO	0b	**SQSTAT6:** #MMR_0_1_0.xml#- Squelch Status - Lane 6 (sqstat6) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
11	RO	0b	**SQSTAT11:** #MMR_0_1_0.xml#- Squelch Status - Lane 11 (sqstat11) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
8	RO	0b	**SQSTAT8:** #MMR_0_1_0.xml#- Squelch Status - Lane 8 (sqstat8) ; #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
13	RO	0b	**SQSTAT13:** #MMR_0_1_0.xml#- Squelch Status - Lane 13 (sqstat13) #MMR_0_1_0.xml#- If enable bit is set, then this bit will toggle depending on the state of the corresponding squelch signal from the AFE ;
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**

Bit	Access	Default Value	Description
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.427 DMI.PEGTRANSLCGCTRL_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d18h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
5	RW	0b	**BPRDFCLOSIDLE:** blocks the fc update based on the timeout counter
6	RW	0b	**BALLFCLOSIDLE:** block all FC update
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**

Bit	Access	Default Value	Description
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.428 DMI.PEGTST_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d0ch/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
20	RO	0b	**LANEREVSTS:** #MMR_0_1_0.xml#- This register bit reflects the status of the PEG lane reversal strap. The PEGLaneReversal strap is mirrored in this register bit. ;
19:16	RW	0000b	**LN0ANY:** #MMR_0_1_0.xml#- Force any PEG lane to be Lane0. These bits do NOT apply if the lane reversal bit is set. ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**

Bit	Access	Default Value	Description
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.429 DMI.PEGUPDNCFG_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d34h/
MMIO: Base/Offset:
IO: Base/Offset:

PEG relate . should be removed

Bit	Access	Default Value	Description
1	RW	0b	**UPDNCFGX2:** Upconfig/Downconfig to x2 Link Width: MMR_0_1_0.xml#-If our link width x1, we will initiate an upconfig to x2 if upconfig is supported by both devices. Else, if the link width > x2 and UPCFGX16, UPDNCFGX8 and UPDNCFGX4 are not set, we will initiate a downconfig to x2.
6	RW	0b	**ADUPCFG:** Advertise upconfig Capability: Set the upconfig capable bit to 1 in our transmitted TS2s during Config. Complete.
2	RW	0b	**UPDNCFGX4:** If our link width ;lt; x4, we will initiate an upconfig to x4 if upconfig is supported by both devices. Else, if the link width > x4 and UPCFGX16 and UPDNCFGX8 are not set, we will initiate a downconfig to x4.
0	RW	0b	**DNCFGX1:** If our link width > x1 and {UPDNCFGXi , i=2,4,8
5	RO	0b	**BLKUPCFG:** Reserved
3	RW	0b	**UPDNCFGX8:** If our link width < x8, we will initiate an upconfig to x8 if upconfig is supported by both devices.

Bit	Access	Default Value	Description
			Else, if the link width = x16 and UPCFGX16 is not set, we will initiate a downconfig to x8
4	RW	0b	**UPCFGX16:** If our link width < x16, we will initiate an upconfig to x16 if upconfig is supported by both devices.
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.430 DMI.PMONDLMASK_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/68h/
MMIO: Base/Offset:
IO: Base/Offset:

This CR control the mask for the PMON - each field control separated counter

Bit	Access	Default Value	Description
5:0	RW	00000b	**MSK0:** this value turn into 1 hot vector that select which pmon event is forwarded to the tl pmon mux
13:8	RW	00000b	**MSK1:** this value turn into 1 hot vector that select which pmon event is forwarded to the tl pmon mux
21:16	RW	00000b	**MSK2:** this value turn into 1 hot vector that select which pmon event is forwarded to the tl pmon mux
29:24	RW	00000b	**MSK3:** this value turn into 1 hot vector that select which pmon event is forwarded to the tl pmon mux
31:30	RO	00b	**RSV3:**
23:22	RO	00b	**RSV2:**
15:14	RO	00b	**RSV1:**
7:6	RO	00b	**RSV0:**

1.11.431 DMI.PMONTLMASK_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/70h/
MMIO: Base/Offset:
IO: Base/Offset:

This CR control the mask for the PMON - each field control separated counter

Bit	Access	Default Value	Description
4:0	RW	00000b	**MSK0:** this value turn into 1 hot vector that select which pmon event is forwarded
12:8	RW	00000b	**MSK1:** this value turn into 1 hot vector that select which pmon event is forwarded
20:16	RW	00000b	**MSK2:** this value turn into 1 hot vector that select which pmon event is forwarded
28:24	RW	00000b	**MSK3:** this value turn into 1 hot vector that select which pmon event is forwarded
31:29	RO	000b	**RSV3:**
23:21	RO	000b	**RSV2:**
15:13	RO	000b	**RSV1:**
7:5	RO	000b	**RSV0:**

1.11.432 DMI.PMTRL0S_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/534h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO	00000000000000000000000000000000b	**PMTRL0S:** #MMR_0_1_0.xml#- Counter granularity is 500MHz regardless of data rate. Counter is incremented once per an receive lane in L1 or L0s. ;

1.11.433 DMI.PMTRL0_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/530h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
31:0	RO	00000000000000000000000000000000b	**PMTRL0:** #MMR_0_1_0.xml#- Counter granularity is 500MHz regardless of data rate. ;

1.11.434 DMI.PSPC_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/210h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RW	0b	**C2RE:** #MMR_0_1_0.xml#- This bit controls the response of PxP to C2 request. ; #MMR_0_1_0.xml#- 1: Follow C2 policies for power saving. ;
15:8	RW	00000000b	**CLEIT:** #MMR_0_1_0.xml#- C2 L0s Entry Idle Timer ;
1	RW	0b	**ASPML0SEP:** #MMR_0_1_0.xml#- ASPM L0s Entry Policy ;
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**

Bit	Access	Default Value	Description
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.435 DMI.PTHERMCTL_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/538h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
2	RW	0b	**FGEN1:** #MMR_0_1_0.xml#- This bit allows Pcode to force gen1 due to thermal condition. (i.e. disable gen2) ;
5	RW	0b	**TL0SDIS:** #MMR_0_1_0.xml#- This bit enables Pcode to disable L0s. ; #MMR_0_1_0.xml#-Pcode may disable L0s based on package C state. ;
6	RW	0b	**INC2:** #MMR_0_1_0.xml#- 0b Normal Mode (Default) ; #MMR_0_1_0.xml#-1b In C2 State ;
0	RW	0b	**FTL0S:** #MMR_0_1_0.xml#- This bit allows Pcode to force TX L0s due to thermal condition ;
1	RW	0b	**FTL1:** #MMR_0_1_0.xml#- This bit allows Pcode to force L1 due to thermal condition ;
4:3	RW	00b	**PMMXWIDTH:** #MMR_0_1_0.xml#- This field allows Pcode to limit Max width of the controller due to thermal or other conditions. ;
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**

Bit	Access	Default Value	Description
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.436 DMI.ROE0_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/e08h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
3:0	RW	0001b	**RXSQLCHEN:**
7:4	RW	1111b	**RXDRCSQSEL:**
8	RW	0b	**RXCMP:**
29	RW	0b	**RXCMPOVEN:**
31	RW	0b	**ROE:**
28:9	RW	0b	**RSVD2809:**
30	RW	0b	**RSVD30:**

1.11.437 DMI.SLOTSTS_0_1_0_PCI

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/bah/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RO	0b	**ABP:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set. ;
4	RO	0b	**CC:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no guarantee that the action corresponding to the command is complete. ; /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- If Command Completed notification is not supported, this bit must be hardwired to 0b. ;
5	RO	0b	**MSS:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This register reports the status of the MRL sensor if it is implemented. ;
7	RO	0b	**EIS:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- If an Electromechanical Interlock is implemented, this bit indicates the current status of the Electromechanical Interlock. ;
1	RO	0b	**PFD:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set. ;
8	RO	0b	**DLLSC:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed. In response to a Data Link Layer State Changed event, software must read the Data Link Layer Link Active field of the Link Status register to determine if the link is active before initiating configuration cycles to the hot plugged device. ;
6	RO	0b	**PDS:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- --In band presence detect state: ;

Bit	Access	Default Value	Description
3	RO	0b	**PDC:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- --A pulse indication that the inband presence detect state has changed ; /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- This bit is set when the value reported in Presence Detect State is changed. ;
2	RO	0b	**MSC:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/acreg_main- If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set. ;
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.438 DMI.THERMALCTRL_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/4b8h/
MMIO: Base/Offset:
IO: Base/Offset:

Thermal Throttling Controls , This register holds the counters values that force Tx entry to LOs

Bit	Access	Default Value	Description
31:16	RW	0000000000000000b	**FORCEL0STMOUT:** #MMR_0_1_0.xml#- For Force TxL0s. This is the minimum amount of time (in 4ns units) we must spend in TxL0s, regardless if the TxL0s exit conditions are met. Default is set to 0 ;
15	RW	0b	**FORCETXL0STMOUTDIS:** #MMR_0_1_0.xml#- For Force TxL0s. When TxL0s exit conditions are met, this bit selects whether we exit TxL0s upon a timeout or once PMunit removes the Force TxL0s condition. ; #MMR_0_1_0.xml#-1: Only exit TxL0s when Force TxL0s condition is removed ;
14	RW	0b	**FORCETXL0SDIS:** #MMR_0_1_0.xml#- Disable Force TxL0s. ; #MMR_0_1_0.xml#-1: Ignore PM force TxL0s throttling requests ;
12	RW	0b	**FORCEMAXDIS:** #MMR_0_1_0.xml#- '0': (Default) Respect PM Max Width requests ; #MMR_0_1_0.xml#-'1': Ignore PM Max Width requests ;
11	RW	0b	**FORCETXL0SCTRL:** #MMR_0_1_0.xml#- 0: PEG Force TX L0s is not qualified with ASPM L0s being enabled. (Default) ; #MMR_0_1_0.xml#-Notes: ASPM L0s enable control is in LCTL[0]. ;
13	RW	0b	**FORCEGEN1DIS:** #MMR_0_1_0.xml#- '0': (Default) Respect PM Force Gen requests ; #MMR_0_1_0.xml#-'1': Ignore PM Force Gen1 requests ;
9:0	RW	0011111010b	**FORCETXL0SLAT:** #MMR_0_1_0.xml#- For Force TxL0s. This indicates the time we wait during L0 before requesting TxL0s entry to link layer in units of 4 ns. ; #MMR_0_1_0.xml#- Default: 0FAh (1us) ;
10	RO	0b	**RSVD10:**

1.11.439 DMI.TOE0_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/e04h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RW	0b	**TXSQLCH:** #MMR_0_1_0.xml#- If TOA = 1b than this bit is replaces the value driven by AFE control to appropriate signal. ;
1	RW	1b	**TXDEEMPHEN:** #MMR_0_1_0.xml#- Regardless of TOE = 1b or not this bit defines if we do deemphasis or not in full

Bit	Access	Default Value	Description
			swing mode. ;
2	RW	0b	**TXSWING:**
3	RW	0b	**TDEMPSEL:** #MMR_0_1_0.xml#- Tx Deemphasis select override ;
4	RW	0b	**GEN2EN:** #MMR_0_1_0.xml#- AFE gen 2 enable ;
7:5	RW	000b	**TXMARGINO:**
30	RW	0b	**TXSQLCHOVEN:**
29	RW	0b	**TXDEEMPHENOVEN:**
28	RW	0b	**TXSWINGOVEN:**
27	RW	0b	**TDEMPSELOVEN:**
26	RW	0b	**GEN2ENOVEN:**
25	RW	0b	**TXMARGINOVEN:**
31	RW	0b	**TOE:**
24:8	RW	00b	**RSVD2408:**

1.11.440 DMI.TRNEN_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/508h/
MMIO: Base/Offset:
IO: Base/Offset:

Bit	Access	Default Value	Description
0	RWO	1b	**TREN:** #MMR_0_1_0.xml#- This bit when set to one enable controller initial training. ;
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
12	RO	0b	**RSVD12:**
13	RO	0b	**RSVD13:**

Bit	Access	Default Value	Description
14	RO	0b	**RSVD14:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.441 DMI.UPCFGSTS_0_1_0_MMR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/d7ch/
MMIO: Base/Offset:
IO: Base/Offset:

Current width reached after up/down config & This field exposes the initial configuration width. ;

Bit	Access	Default Value	Description
18:16	RO	101b	**CCFGWDTH:** This register expose the current width reached after up/down config. ;
15:0	RO	0000000000000000b	**ICFGWDTH:** This field exposes the initial configuration width.
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**

Bit	Access	Default Value	Description
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
28	RO	0b	**RSVD28:**
29	RO	0b	**RSVD29:**
30	RO	0b	**RSVD30:**
31	RO	0b	**RSVD31:**

1.11.442 DMI.VC01CL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/320h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d50d0) Contains the limit for maximum number of request transactions` fragments which may be chained for vc0 & vc1

Bit	Access	Default Value	Description
5:0	RW	001000b	**VC0NPCL:** VC0NPCL VC 0 Non Posted Chain Limit 5:0 08h RW Defines the maximum number of consecutive fragments marked as chain. For any transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
14:12	RW	011b	**VC0PCL:** VC0PCL VC 0 Posted Chain Limit 14:12 011b RW Defines the maximum number of consecutive fragments marked as chain. For transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
21:16	RW	001000b	**VC1NPCL:** VC1NPCL VC1 Non Posted Chain Limit 21:16 08h RW Defines the maximum number of consecutive fragments marked as chain. For any transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
30:28	RW	011b	**VC1PCL:** VC1PCL VC1 Posted Chain Limit 30:28 011b RW Defines the maximum number of consecutive fragments marked as chain. For transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**

11	RO	0b	**RSVD11:**
15	RO	0b	**RSVD15:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
31	RO	0b	**RSVD31:**

1.11.443 DMI.VC01DATABUF_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/48h/
MMIO: Base/Offset:
IO: Base/Offset:

this CR control the separation of the data memory allocated at the downstream iosf to scl block

Bit	Access	Default Value	Description
6:0	RW	0000000b	**VC0NP:** holds the overlap values of the downstream iosf2scl block
13:7	RW	0000001b	**VC0P:** holds the overlap values of the downstream iosf2scl block
20:14	RW	0010001b	**VC0CMP:** holds the overlap values of the downstream iosf2scl block
27:21	RW	0100001b	**VC1NP:** holds the overlap values of the downstream iosf2scl block
31:28	RO	0000b	**RSV3:**

1.11.444 DMI.VC01TP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/350h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d53f0)VC0 and Vc1 transactions pending in TL queue

Bit	Access	Default Value	Description
14:8	RO	0000000b	**VC0NPTP:** VC0NPTP VC0 Non Posted Transaction Pending 14:8 00h RO-V
6:0	RO	0000000b	**VC0PTP:** VC0PTP VC0 Posted Transaction Pending 6:0

Bit	Access	Default Value	Description
			00h RO-V
30:24	RO	0000000b	**VC1TP:** VC1TP VC1 Posted Transaction Pending 30:24 00h RO-V
7	RO	0b	**RSVD7:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
31	RO	0b	**RSVD31:**

1.11.445 DMI.VCPMCL_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/324h/
MMIO: Base/Offset:
IO: Base/Offset:

HASH(0x6d5140) Contains the limit for maximum number of request transactions` fragments which may be chained for vcp & vcm

Bit	Access	Default Value	Description
5:0	RW	001000b	**VCPNPCL:** VCPNPCL VCp Non Posted Chain Limit 5:0 08h RW Defines the maximum number of consecutive fragments marked as chain. For any transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
14:12	RW	011b	**VCPPCL:** VCPPCL VCp Posted Chain Limit 14:12 011b RW Defines the maximum number of consecutive fragments marked as chain. For transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
21:16	RW	001000b	**VCMNPCL:** VCMNPCL VCm Non Posted Chain Limit 21:16 08h RW Defines the maximum number of consecutive fragments marked as chain. For any transaction that is fragmented to more fragments than defined here, the fragments will be separated to different chain groups.
30:28	RW	011b	**VCMPCL:** VCMPCL VCm Posted Chain Limit 30:28 011b RW Defines the maximum number of consecutive fragments marked as chain. For transaction that is fragmented to more fragments than defined here, the

Bit	Access	Default Value	Description
			fragments will be separated to different chain groups.
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
8	RO	0b	**RSVD8:**
9	RO	0b	**RSVD9:**
10	RO	0b	**RSVD10:**
11	RO	0b	**RSVD11:**
15	RO	0b	**RSVD15:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
24	RO	0b	**RSVD24:**
25	RO	0b	**RSVD25:**
26	RO	0b	**RSVD26:**
27	RO	0b	**RSVD27:**
31	RO	0b	**RSVD31:**

1.11.446 DMI.VCPMDATABUF_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/4ch/
MMIO: Base/Offset:
IO: Base/Offset:

this CR control the separation of the data memory allocated at the downstream iosf to scl block

Bit	Access	Default Value	Description
6:0	RW	0110001b	**VCPNP:** holds the overlap values of the downstream iosf2scl block
13:7	RW	1000001b	**VCMNP:** holds the overlap values of the downstream iosf2scl block
20:14	RW	1010001b	**TOP:** holds the overlap values of the downstream iosf2scl block
31	RW	0b	**CHIDMAPPING:** 1: downstream transaction is mapped base on chid 0: DMI internal logic
30:21	RO	0000b	**RSV3:**

1.11.447 DMI.VCPMTP_0_0_0_DMIBAR

PCI: B/D/F/Reg: 0/0h/0/
SBI: Port/Reg/Mem: 80h/354h/
MMIO: Base/Offset:

IO: Base/Offset:

HASH(0x6d5470)VCp and Vcm transactions pending in TL queue

Bit	Access	Default Value	Description
14:8	RO	0000000b	**VCPTP:** VCPTP VCp Transaction Pending 14:8 00h RO-V VCp Transactions Pending
30:24	RO	0000000b	**VCMTP:** /nfs/iil/stod/stod070/w.alandau.100/gsr-d0/target/creg/gen/pcie_creg.xml- This counter is used to expose how many TLP are blocked for allowing proper ;
0	RO	0b	**RSVD0:**
1	RO	0b	**RSVD1:**
2	RO	0b	**RSVD2:**
3	RO	0b	**RSVD3:**
4	RO	0b	**RSVD4:**
5	RO	0b	**RSVD5:**
6	RO	0b	**RSVD6:**
7	RO	0b	**RSVD7:**
15	RO	0b	**RSVD15:**
16	RO	0b	**RSVD16:**
17	RO	0b	**RSVD17:**
18	RO	0b	**RSVD18:**
19	RO	0b	**RSVD19:**
20	RO	0b	**RSVD20:**
21	RO	0b	**RSVD21:**
22	RO	0b	**RSVD22:**
23	RO	0b	**RSVD23:**
31	RO	0b	**RSVD31:**

1.11.448 DCAL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/0Ah/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Calibration Control

Bit	Access	Default Value	Description
31:14	RO	0b	**RESERVED:**
13:12	RW	01b	**ZQCL_SER:** ZQCL to different ranks after SRX is serial, parallel, or disabled
11	RO	0b	**RESERVED:**

10:8	RW	11b	**ZQ_INTRVL:**
7:0	RO	0b	**RESERVED:**

1.11.449 DCO

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/0Fh/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Controller Operation Register

Bit	Access	Default Value	Description
31	RW	0b	**INITIALIZATION_COMPLETE:** Indicates that initialization of the memory subsystem has completed. Memory accesses are permitted and maintenance operation begins.
30	RO	0b	**DDRIO_INITIALIZATION_COMPLETE:** Reflects the DDRIO init complete config bit - `dconfig1.dio_spid_init_complete
29	RO	0b	**RESERVED:**
28	RW	0b	**PRI_CONTROL_SELECT:** Request bus source select; 0-"DRAM buffering and arbitration unit", 1-REUT
27:9	RO	0b	**RESERVED:**
8	RW	0b	**REUT_LOCK:** Writing 1 to this bit will lock PRI_CONTROL_SELECT to changes
7:1	RO	0b	**RESERVED:**
0	RW	0b	**DRP_LOCK:** Writing 1 to this bit will lock DRP to changes

1.11.450 DPMC0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/06h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Power Management Control Register 0

Bit	Access	Default Value	Description
31:27	RO	0	**RESERVED:**
26	RW	0b	**BURST_LENGTH_MODE:** Burst Length Mode - BL8 or OTF BL8/BC4
25	RW	1b	**DISABLE_POWER_DOWN:** When set to 1, the "DRAM controller" will not drive CKE low to place the DRAM in Active or Precharge power down mode. The setting of this defeature bit applies to both DDR2 and LPDDR. (Defeature)
24	RW	1b	**CLOCK_GATING_DISABLED:** This is a global clock gate disable bit for the whole "DRAM controller". When set to 1,

Bit	Access	Default Value	Description
			it disables all clock gating logic in the “DRAM controller”.
23	RW	0b	**DYNAMIC_SELF_REFRESH:** When set to 1, enables a mode that will automatically place the memory into a low power state following the data phase for the last request if there are no more requests pending in the memory controller regardless of CPU state. The memory will be brought out of Self Refresh when a new memory request is detected from either the “DRAM buffering and arbitration unit” or the “Power Management Controller (PMU)” with a status of 2 or 3. The DRAM will remain in Self Refresh and all requests from the “DRAM buffering and arbitration unit” and “Power Management Controller (PMU)” are ignored if the status from both units is 0 or 1.
22	RO	0	**RESERVED:**
21	RW	0b	**PRECHARGE_ALL_BEFORE_PWD:**
20	RW	0b	**WAKE_ALLOWED_FOR_PAGE_CLOSE_TIMEOUT:** A 1 in this field indicates that the controller is allowed to wake the memory devices for individual page closes due to page timer expiration. Trades some increased performance for potential additional average power consumption.
19	RO	0	**RESERVED:**
18:16	RW	0b	**PAGE_CLOSE_TIMEOUT_PERIOD:** This specifies the time from the last access of a DRAM page until that page is scheduled for closing. This is implemented with a single sliding widow, which results in a range rather than a precise value. ;000 - Page Close Timer disabled;001 - 15-8 DRAM Clocks;010 - 31-16 DRAM Clocks;011 - 63-32 DRAM Clocks;100 - 127-64 DRAM clocks;101 - 255-128 DRAM clocks;110 - 511-256 DRAM clocks;111 - 1023-512 DRAM clocks
15:13	RO	0b	**RESERVED:**
12:8	RW	0h	**POWERMODE_MESSAGE:** This is the power mode message that is sent to the DDRIO upon entering self refresh
7:0	RW	0h	**SELF_REFRESH_ENTRY_DELAY:** This value specifies the number of “DRAM controller” clocks (coreclock) that the “DRAM controller” will wait before it enters Dynamic Self Refresh mode when there are no pending requests from the “DRAM buffering and arbitration unit” and “Power Management Controller (PMU)”, and the status from both units are 0 or 1.

1.11.451 DPMC1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/07h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Power Management Register 1

Bit	Access	Default Value	Description
31:22	RO	0b	**RESERVED:**
21:20	RO	0b	**MPLL_REF_CLK:** MPLL Bypass reference clock select
19:6	RO	0b	**RESERVED:**
5:4	RW	1b	**TRISTATE_CMD:** Command Tristate Control
3:1	RO	0b	**RESERVED:**
0	RW	1b	**TRISTATE_CS:** Command Tristate Control

1.11.452 DRMC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/0Bh/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Scheduler control Register

Bit	Access	Default Value	Description
31:17	RO	0b	**RESERVED:**
16	RW	0b	**COLD_WAKE:**
15:13	RO	0b	**RESERVED:**
12	RW	0b	**ODTMODE:** control over ODT pins is MC or BIOS
11:8	RW	0b	**ODTVAL:** ODT values when BIOS controls
7:5	RO	0b	**RESERVED:**
4	RW	0b	**CKEMODE:** control over CKE is MC or BIOS
3:0	RW	0b	**CKEVAL:** CKE value when BIOS controls

1.11.453 DRP

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/00h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Rank Population Register; This register identifies the type of memory populated on each of the two memory DIMMs and the enabling and disabling of certain Ranks in them. It should not be changed after the Initialization Complete bit is set in the DCO register.

Bit	Access	Default Value	Description
31:22	RO	0	**RESERVED:**
21	RW	0	**DIMM1_MIRROR:** DIMM1MIRROR - address bits are mirrored in rank 1 of DIMM 1
20	RW	0	**DIMM0_MIRROR:** DIMM0MIRROR - address bits are

Bit	Access	Default Value	Description
			mirrored in rank 1 of DIMM 0
19:17	RO	0	**RESERVED:**
16	RW	0	**DIMM_FLIP:** DIMM_FLIP = (DIMM1 size > DIMM0 size)
15:13	RO	0	**RESERVED:**
12	RW	0b	**ADDR_MAP_SEL:** Address Map Select. 0-Map 0, 1-Map 1
11	RO	0	**RESERVED:**
10:9	RW	0b	**DEV_1_DEVICE_DENSITY:** This sets the density of the DRAMs populated in DIMM 1. 00-1Gb, 01-2Gb, 10-4Gb, 11-Reserved
8	RW	0b	**DEV_1_DEVICE_WIDTH:** Indicates the width of the DRAMs populated in DIMM 1. 0-x8 Devices 1-x16 Devices
7	RO	0b	**RESERVED:**
6:5	RW	0b	**DEV_0_DEVICE_DENSITY:** This sets the density of the DRAMs populated in DIMM 0. 00-1Gb, 01-2Gb, 10-4Gb, 11-Reserved
4	RW	0b	**DEV_0_DEVICE_WIDTH:** Indicates the width of the DRAMs populated in DIMM 0. 0-x8 Devices 1-x16 Devices
3	RW	0b	**RANK_3_ENABLED:** Should be set to 1 when rank 3 is populated to enable the use of this rank. Otherwise this must be left cleared to 0.
2	RW	0b	**RANK_2_ENABLED:** Should be set to 1 when rank 2 is populated to enable the use of this rank. Otherwise this must be left cleared to 0.
1	RW	0b	**RANK_1_ENABLED:** Should be set to 1 when rank 1 is populated to enable the use of this rank. Otherwise this must be left cleared to 0.
0	RW	0b	**RANK_0_ENABLED:** Should be set to 1 when rank 0 is populated to enable the use of this rank. Otherwise this must be left cleared to 0.

1.11.454 DTR0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/01h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Timing Register 0; This identifies the timing to be used to interface to the DRAM devices. This information is based on the specifications for the memory devices populated as well as the specifications driven by the system requirements. It should not be changed after the Initialization Complete bit is set in the DCO register.

Bit	Access	Default Value	Description
31:28	RW	0100b	**CKE_DLY:** CKE Delay
27:26	RO	0b	**RESERVED:**

Bit	Access	Default Value	Description
25:24	RW	11b	**POWER_MODE_ENTRY_DELAY:** SR Entry to PM Message delay
23	RO	0b	**RESERVED:**
22	RW	0b	**ZCAL_LONG_RECOVERY_PERIOD:** ZQCAL Long recovery period
21	RO	0b	**RESERVED:**
20	RW	0b	**ZQCAL_SHORT_RECOVERY_PERIOD:**
19	RO	0b	**RESERVED:**
18	RW	0b	**SELF_REFRESH_EXIT_TXSDLL:** SR Exit delay to commands requiring locked DLL
17	RO	0b	**RESERVED:**
16	RW	0b	**SELF_REFRESH_EXIT_TXS:** SR Exit delay to commands not requiring locked DLL
15	RO	0b	**RESERVED:**
14:12	RW	1b	**CAS_LATENCY_TCL:** This specifies the delay from issuing a Read command until data return begins.; 000 - 5 DRAM Clocks (DDR3-800);001 - 6 DRAM Clocks (DDR3-800, 1066);010 - 7 DRAM Clocks (DDR3-1066, 1333);011 - 8 DRAM Clocks (DDR3-1066, 1333);100 - 9 DRAM Clocks (DDR3-1333);101 - 10 DRAM Clocks (DDR3-1333);110 - 111 - Reserved
11	RO	0b	**RESERVED:**
10:8	RW	1b	**ACTIVATE_TO_CAS_DELAY_TRCD:** This specifies the delay required from when an Activate command is sent until a Read or a Write command may be sent to the same bank.;000 - 5 DRAM Clocks (DDR3-800);001 - 6 DRAM Clocks (DDR3-800, 1066);010 - 7 DRAM Clocks (DDR3-1066, 1333);011 - 8 DRAM Clocks (DDR3-1066, 1333);100 - 9 DRAM Clocks (DDR3-1333);101 - 10 DRAM Clocks (DDR3-1333);110 - 111 - Reserved
7	RO	0b	**RESERVED:**
6:4	RW	1b	**PRECHARGE_TO_ACTIVATE_DELAY_TRP:** This specifies the delay required from when a Precharge command is sent until an Activate command may be sent to the same bank.;000 - 5 DRAM Clocks (DDR3-800);001 - 6 DRAM Clocks (DDR3-800, 1066);010 - 7 DRAM Clocks (DDR3-1066, 1333);011 - 8 DRAM Clocks (DDR3-1066, 1333);100 - 9 DRAM Clocks (DDR3-1333);101 – 10 DRAM Clocks (DDR3-1333);110 - 111 – Reserved
3:2	RO	0b	**RESERVED:**
1:0	RW	0b	**DRAM_FREQUENCY:** This specifies the frequency that is used for computing proper cycle to cycle timings. It has no control on the actual clock frequency.;00 - DDR3-800; 01 - DDR3-1066 ; 10 DDR3-1333 ; 11 - reserved

1.11.455 DTR1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/02h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Timing Register 1;This identifies the timing to be used to interface to the DRAM devices. This information is based on the specifications for the memory devices populated as well as the specifications driven by the system requirements. It should not be changed after the Initialization Complete bit is set in the DCO register.

Bit	Access	Default Value	Description
31:30	RO	0b	**RESERVED:**
29:28	RW	0b	**READ_TO_PRECHARGE_DELAY_TRTP:** The time interval between a Read and a Precharge command; 00 - 4 DRAM Clocks (DDR3-800 DDR3-1067), 01 - 5 DRAM Clocks (DDR3-1333), 10-11 - reserved
27:26	RO	0b	**RESERVED:**
25:24	RW	10b	**ROW_ACT_TO_ROW_ACT_TRRD:** Row activation to Row activation Delay
23:20	RW	0110b	**ROW_ACTIVATION_PERIOD_TRAS:** Row Activation Period: Time interval between Activate to Precharge
19:16	RW	1001b	**FOUR_BANK_ACTIVATION_WINDOW_TFAW:** Four bank Activation Window
15:14	RO	0b	**RESERVED:**
13:12	RW	0b	**CAS_TO_CAS_DELAY_TCCD:** The minimal gap between any 2 read or write data
11	RO	0b	**RESERVED:**
10:8	RW	11b	**WRITE_TO_PRECHARGE_DELAY:** Write to Precharge Delay Same Bank = 4 + tWCL + tWR
7:6	RO	0b	**RESERVED:**
5:4	RW	10b	**COMMAND_TRANSPORT_DURATION_TCMD:** The time period that a command occupies the command bus
3:2	RO	0b	**RESERVED:**
1:0	RW	0b	**CAS_WRITE_LATENCY_TWCL:** CAS Write latency. 00-5 clocks, 01-6 clocks, 10-7 clocks, 11-8 clocks

1.11.456 DTR2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/03h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Timing Register 2;This identifies the timing to be used to interface to the DRAM devices. This information is based on the specifications for the memory devices populated as well as the specifications driven by the system requirements. It should not be changed after the Initialization Complete bit is set in the DCO register.

Bit	Access	Default Value	Description
31:28	RO	0b	**RESERVED:**
27:24	RW	0110b	**POWERDOWN_DELAY:**
23:22	RW	01b	**CKE_SET_TO_ANY_COMMAND_TXP:**
21:19	RW	001b	**WR_TO_RD_SAME_RANK_SAME_DIMM:**
18:16	RW	010b	**RD_TO_WR_SAME_RANK_SAME_DIMM:**
15:14	RW	11b	**WR_TO_RD_DIFF_DIMM:**
13:12	RW	11b	**WR_TO_RD_DIFF_RANK_SAME_DIMM:**
11:10	RW	11b	**RD_TO_WR_DIFF_DIMM:**
9:8	RW	11b	**RD_TO_WR_DIFF_RANK_SAME_DIMM:**
7:6	RW	11b	**WR_TO_WR_DIFF_DIMM:**
5:4	RW	11b	**WR_TO_WR_DIFF_RANK_SAME_DIMM:**
3:2	RW	11b	**RD_TO_RD_DIFF_DIMM:**
1:0	RW	11b	**RD_TO_RD_DIFF_RANK_SAME_DIMM:**

1.11.457 DTR3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/04h/
MMIO: Base/Offset:
IO: Base/Offset:

DRAM Timing Register 3; This identifies the ODT related timing.

Bit	Access	Default Value	Description
31:17	RO	0b	**RESERVED:**
16	RW	0b	**STRETCH_TARGET_DISABLED:**
15	RO	0b	**RESERVED:**
14:12	RW	011b	**READ_TO_ODT_STOP:**
11	RO	0b	**RESERVED:**
10:8	RW	011b	**READ_TO_ODT_START:**
7	RO	0b	**RESERVED:**
6:4	RW	10b	**WRITE_TO_ODT_STOP:**
3:2	RO	0b	**RESERVED:**
1:0	RW	10b	**WRITE_TO_ODT_START:**

1.11.458 DTRC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/10h/
MMIO: Base/Offset:

IO: Base/Offset:

DRAM Training Control

Bit	Access	Default Value	Description
31:6	RO	0b	**RESERVED:**
5	RW	0b	**BLOCK_PHASEB:**
4	RW	0b	**BLOCK_IPFULL:**
3	RW	0b	**BLOCK_PRECHARGES:**
2	RW	0b	**BLOCK_ACTIVATES:**
1	RW	0b	**BLOCK_WRITES:**
0	RW	0b	**BLOCK_READS:**

1.11.459 PMSEL0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/E0h/
MMIO: Base/Offset:
IO: Base/Offset:

Performance Monitor Event Select Register 0

Bit	Access	Default Value	Description
31	RO	0b	**PERFMON_ENABLED_STATUS:** 0 “DRAM controller” perfmon is disabled.;1 “DRAM controller” perfmon is enabled.
30:14	RO	0	**RESERVED:**
13:8	RW	00000b	**EVENT_MASK:** Event Mask
7:4	RO	0	**RESERVED:**
3:0	RW	0h	**EVENT_ID:** Event ID

1.11.460 PMSEL1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/E1h/
MMIO: Base/Offset:
IO: Base/Offset:

Performance Monitor Event Select Register 1

Bit	Access	Default Value	Description
31:14	RO	0	**RESERVED:**
13:8	RW	00000b	**EVENT_MASK:** Event Mask
7:4	RO	0	**RESERVED:**
3:0	RW	0h	**EVENT_ID:** Event ID

1.11.461 PMSEL2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/E2h/
MMIO: Base/Offset:
IO: Base/Offset:

Performance Monitor Event Select Register 2

Bit	Access	Default Value	Description
31:14	RO	0	**RESERVED:**
13:8	RW	00000b	**EVENT_MASK:** Event Mask
7:4	RO	0	**RESERVED:**
3:0	RW	0h	**EVENT_ID:** Event ID

1.11.462 PMSEL3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 01h/E3h/
MMIO: Base/Offset:
IO: Base/Offset:

Performance Monitor Event Select Register 3

Bit	Access	Default Value	Description
31:14	RO	0	**RESERVED:**
13:8	RW	00000b	**EVENT_MASK:** Event Mask
7:4	RO	0	**RESERVED:**
3:0	RW	0h	**EVENT_ID:** Event ID

1.11.463 GVD.ASLE

PCI: B/D/F/Reg: 0/2/0/E4h
SBI: Port/Reg/Mem: 06h/39h/
MMIO: Base/Offset:
IO: Base/Offset:

System Display Event Register. SBIOS writes this register to generate an interrupt to the graphics/display driver.

Bit	Access	Default Value	Description
31:24	RW	00h	**ASLE_SCRATCH_TRIGGER_3:** AST3: The writing of this by field (byte) - even if just writing back the original contents - will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0]

Bit	Access	Default Value	Description
			= 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23:16	RW	00h	**ASLE_SCRATCH_TRIGGER_2:** AST2: The writing of this by field (byte) - even if just writing back the original contents - will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15:8	RW	00h	**ASLE_SCRATCH_TRIGGER_1:** AST1: The writing of this by field (byte) - even if just writing back the original contents - will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	RW	00h	**ASLE_SCRATCH_TRIGGER_0:** AST0: The writing of this by field (byte) - even if just writing back the original contents - will trigger a display controller interrupt (when the memory interface register bits IER[0] = 1 and IMR[0] = 0). If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.

1.11.464 GVD.ASLS

PCI: B/D/F/Reg: 0/2/0/FCh
SBI: Port/Reg/Mem: 06h/3Fh/
MMIO: Base/Offset:
IO: Base/Offset:

ASL Storage. The Lincroft display driver does not need this register since memory Operational Region (OpRegion) is available. This register is kept for use as scratch space.

Bit	Access	Default Value	Description
31:0	RW	00000000h	**SCRATCH:** This register provides a means for the BIOS to communicate with the driver. This definition of this scratch register is worked out in common between System BIOS and driver software. Storage for up to 6 devices is possible. For each device, the ASL control method requires two bits for _DOD (BIOS detectable yes or no, VGA/Non VGA), one bit for _DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).

1.11.465 GVD.BSM

PCI: B/D/F/Reg: 0/2/0/5Ch
SBI: Port/Reg/Mem: 06h/17h/
MMIO: Base/Offset:
IO: Base/Offset:

Base of Stolen Memory

Bit	Access	Default Value	Description
31:20	RW	000h	**BASE_OF_STOLEN_MEMORY:** BSM: This register contains bits 31 to 20 of the base address of stolen DRAM memory. When the GVD receives a VGA memory request address[19:5] from the VRD or VRH, the GVD appends the base address BSM[31:20] to form the full physical address to send to the “DRAM buffering and arbitration unit”.
19:0	RO	00000h	**RESERVED:** Reserved

1.11.466 GVD.CAPPOINT

PCI: B/D/F/Reg: 0/2/0/34h
SBI: Port/Reg/Mem: 06h/0Dh/
MMIO: Base/Offset:
IO: Base/Offset:

Capabilities Pointer

Bit	Access	Default Value	Description
31:8	RO	000000h	**RESERVED:** Reserved
7:0	RO	D0h	**CAPABILITIES_POINTER:** The first item in the capabilities list is at address D0h.

1.11.467 GVD.FD

PCI: B/D/F/Reg: 0/2/0/C4h
SBI: Port/Reg/Mem: 06h/31h/
MMIO: Base/Offset:
IO: Base/Offset:

Functional Disable. This register is used by SBIOS, not by driver.

Bit	Access	Default Value	Description
31:2	RO	00000000h	**RESERVED:** Reserved
1	RW	0b	**MSI_DISABLE:** MD: When set, the MSI capability pointer is not available - the item which points to the MSI capability (the power management capability), will instead indicate that this is the last item in the list.
0	RW	0b	**FUNCTION_DISABLE:** FD: When set, the function is disabled (configuration space is disabled). When set, the GVD stops accepting any new requests on the IOSF bus including any new configuration cycle requests to clear this bit. Since Lincroft does not support a separate external PCI graphics card, this bit should never be set.

1.11.468 GVD.GFX_IOBAR

PCI: B/D/F/Reg: 0/2/0/14h
SBI: Port/Reg/Mem: 06h/05h/
MMIO: Base/Offset:
IO: Base/Offset:

I/O Base Address. This is used only by SBIOS and is the base address for the MMIO_INDEX and MMIO_DATA registers.

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:3	RW	0000h	**BASE_ADDRESS:** BA: Set by the OS, these bits correspond to address signals [15:3]. The GVD will compare the SCL address scldown3_address[15:3] with GFX_IOBAR[15:3]. If there is a match, and PCICMDSTS[0] = IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will select the command (i.e. issue a scldown3_hit). The GFX_IOBAR is to be used for register programming the GVD memory interface registers, the display controller registers, the graphics cluster (GFX) registers, the video decode (VED) registers, the video encode (VEC) registers, and the video processing block (VPB) registers using the indirect register access method. The GFX_IOBAR is to be used for GTT write on SCL using the indirect access method.
2:1	RO	0h	**RESERVED:** Reserved
0	RO	1	**RESOURCE_TYPE_RTE:** Indicates a request for I/O space.

1.11.469 GVD.GMCH_PERF_EVTSEL0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 07h/E0h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL0

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.470 GVD.GMCH_PERF_EVTSEL1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 07h/E1h/

MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL1

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.471 GVD.GMCH_PERF_EVTSEL2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 07h/E2h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL2

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.472 GVD.GMCH_PERF_EVTSEL3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 07h/E3h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL3

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.473 GVD.HDR

PCI: B/D/F/Reg: 0/2/0/0Ch
SBI: Port/Reg/Mem: 06h/03h/
MMIO: Base/Offset:
IO: Base/Offset:

Header Type

Bit	Access	Default Value	Description
31:24	RO	00h	**RESERVED:** Reserved
23	RO	0b	**MULTI_FUNCTION_STATUS:** MFUNC: Integrated graphics is a single function.
22:16	RO	00h	**HEADER_CODE:** HDR: Indicates a type 0 header format.
15:0	RO	0000h	**RESERVED:** Reserved

1.11.474 GVD.ID

PCI: B/D/F/Reg: 0/2/0/00h
SBI: Port/Reg/Mem: 06h/00h/
MMIO: Base/Offset:
IO: Base/Offset:

D2: PCI Device and Vendor ID Register

Bit	Access	Default Value	Description
31:20	RO	0BEh	**DEVICE_IDENTIFICATION_NUMBER_HIGH:** DIDH: Identifier assigned to the Device 2 Graphics PCI device. Bits[31:20] of this register are strapped at the GVD top level.
19:16	RO	fus_gvd_fuses_bus_zcznfwh[7:4]	**DEVICE_IDENTIFICATION_NUMBER_LOW:** DIDL: Identifier assigned to the Device 2 Graphics PCI device. Bits[19:16] of this register are determined by fuse fus_gvd_fuses_bus_zcznfwh[7:4].
15:0	RO	8086h	**VENDOR_IDENTIFICATION_NUMBER:** VID: PCI standard identification for Intel.

1.11.475 GVD.INTR

PCI: B/D/F/Reg: 0/2/0/3Ch
SBI: Port/Reg/Mem: 06h/0Fh/
MMIO: Base/Offset:
IO: Base/Offset:

Interrupt. This register is programmed by SBIOS. It is not used by the graphics/display driver.

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:8	RO	01h	**INTERRUPT_PIN:** IPIN: Value indicates which interrupt pin this device uses. This field is hard coded to 1h since Lincroft Device 2 is a single function device. The PCI spec requires that it use INTA#.
7:0	RW	00h	**INTERRUPT_LINE:** ILIN: BIOS written value to communicate interrupt line routing information to the device driver.

1.11.476 GVD.LBB

PCI: B/D/F/Reg: 0/2/0/F4h
SBI: Port/Reg/Mem: 06h/3Dh/
MMIO: Base/Offset:
IO: Base/Offset:

Legacy Backlight Brightness. The display driver in Lincroft does not use this register since ASLE is available.

Bit	Access	Default Value	Description
31:24	RW	00h	**SCRATCH_3:** Software scratch byte 3. Any write to this byte, even writing back the same value read, will trigger GVD to send the contents of LEGACY_BACKLIGHT_BRIGHTNESS byte to the VSunit.
23:16	RW	00h	**SCRATCH_2:** Software scratch byte 2. Any write to this byte, even writing back the same value read, will trigger GVD to send the contents of LEGACY_BACKLIGHT_BRIGHTNESS byte to the VSunit.
15:8	RW	00h	**SCRATCH_1:** Software scratch byte 1. Any write to this byte, even writing back the same value read, will trigger GVD to send the contents of LEGACY_BACKLIGHT_BRIGHTNESS byte to the VSunit.
7:0	RW	00h	**LEGACY_BACKLIGHT_BRIGHTNESS:** LBES: The value of zero is the lowest brightness setting and the value of 255 is the brightest. A write to this register will cause a flag to be set (LBES) in the PIPEBSTATUS register and cause an interrupt if Backlight event in the PIPEBSTATUS register and cause an Interrupt if Backlight Event (LBEE) and Display B Event is enabled by software. The field value (byte) is forwarded by the GVD to the Vsunit.

1.11.477 GVD.MA

PCI: B/D/F/Reg: 0/2/0/94h
SBI: Port/Reg/Mem: 06h/25h/
MMIO: Base/Offset:
IO: Base/Offset:

Message Address

Bit	Access	Default Value	Description
31:2	RW	00000000h	**ADDRESS:** MA: Lower 32-bits of the system specified message address, always DW aligned. When the GVD issues an MSI interrupt as a MEMWR on the SCL, the memory address corresponds to the value of this field.
1:0	RO	00b	**RESERVED:** Reserved

1.11.478 GVD.MANUFACTURING_ID

PCI: B/D/F/Reg: 0/2/0/F8h
SBI: Port/Reg/Mem: 06h/3Eh/
MMIO: Base/Offset:
IO: Base/Offset:

Manufacturing ID

Bit	Access	Default Value	Description
31:24	RO	00h	**RESERVED:** Reserved
23:0	RO	strapMANID[23:0]	**MANUFACTURING_ID:** Hardwired to strapMANID[23:0].

1.11.479 GVD.MD

PCI: B/D/F/Reg: 0/2/0/98h
SBI: Port/Reg/Mem: 06h/26h/
MMIO: Base/Offset:
IO: Base/Offset:

Message Data

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15:0	RW	0000h	**DATA:** MD: This 16-bit field is programmed by system software and is driven onto the lower word of data during the data phase of the MSI write transaction. When the GVD issues an MSI interrupt as a MEMWR on the SCL, the write data corresponds to the value of this field.

1.11.480 GVD.MGGC

PCI: B/D/F/Reg: 0/2/0/50h
SBI: Port/Reg/Mem: 06h/14h/
MMIO: Base/Offset:
IO: Base/Offset:

Graphics Control

Bit	Access	Default Value	Description
31:23	RO	0	**RESERVED:**

Bit	Access	Default Value	Description
22:20	RW	011b	**GRAPHICS_MODE_SELECT:** GMS: This field is used to select the amount of memory pre-allocated to support the graphics device in VGA (non-linear) and Native (linear) modes. If graphics is disabled, this value must be programmed to 000h. ; 000 = No memory pre-allocated. Graphics does not claim VGA cycles (Mem and IO), and CC.SCC is 80h. ; 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. ; 010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. ; 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. ; 100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. ; 101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. ; 110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. ; 111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. ; ; When GMS not equal to 000 (and VD=0) the GVD will check if the SCL address scldown3_address[31:0] is in the VGA memory range. (The VGA memory range is A0000h to BFFFFh.) If there is a match and MSE = 1 and the SCL command is either a MEMRD or MEMWR, the GVD will initiate an RMdwvgamemen_cr cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will initiate a (VGA) register cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. When GMS is equal to 000, the GVD will not check if the SCL address is in the VGA memory range or in the VGA IO register address range. Also, when GMS is set to 3'b000, then CC[15:8] is changed to 8'h80 from 8'h00.
19:18	RO	0	**RESERVED:** Reserved
17	RW	0b	**VGA_DISABLE:** VD: When set, VGA memory or I/O cycles are not claimed, and CC.SCC is set to 80h. When cleared, VGA memory and I/O cycles are enabled, and CC.SCC is set to 00h. ; When 0 (and GMS not equal to 000), the GVD will check if the SCL address scldown3_address[31:0] is in the VGA memory range. (The VGA memory range is A0000h to BFFFFh.) If there is a match and MSE=1 and the SCL command is either a MEMRD or MEMWR, the GVD will initiate an RMdwvgamemen_cr cycle on the RMbus. If the RMbus returns a hit the GVD will select the command. As well, when 0 the GVD will check if scldown3_address[15:0] is one of the VGA IO register range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) If there is a match and IOSE = 1 and the SCL command is either an IORD or IOWR, the GVD will initiate a (VGA) register cycle on the RMbus. If the RMbus returns a hit then the command will be claimed by the GVD. When 1, the GVD will not check if the SCL address is in the VGA memory range or in the VGA IO register address range. Also, when the field is set 1'b1 and GMS = 3'b000, then CC[15:8] is changed to 8'h80 from 8'h00.

Bit	Access	Default Value	Description
16:0	RO	00000h	**RESERVED:** Reserved

1.11.481 GVD.MMADR

PCI: B/D/F/Reg: 0/2/0/10h
SBI: Port/Reg/Mem: 06h/04h/
MMIO: Base/Offset:
IO: Base/Offset:

Memory Mapped Address Range. This is the base address for all memory mapped registers.

Bit	Access	Default Value	Description
31:20	RW	000h	**BASE_ADDRESS:** BA: Set by the OS, these bits correspond to address signals [31:20]. The GVD will compare the SCL address scldown3_address[31:20] with MMADR[31:20]. If there is a match, and PCICMDSTS[1] = MSE = 1 and the SCL command is either a MEMRD or MEMWR, the GVD will select the command and present it on the RMbus. The MMADR is to be used for register programming the GVD memory interface registers, the display controller registers, the graphics cluster (GFX) registers, the video decode (VED) registers, the video encode (VEC) registers, and the video processing block (VPB) registers. If the display controller registers don't assert claim, then GVD will report a miss on the IOSF bus For all other register address that are part of this address range, GVD will assert a hit on the IOSF bus
19:1	RO	0000h	**RESERVED:** Reserved
0	RO	0b	**RESOURCE_TYPE:** RTE: Indicates a request for memory space.

1.11.482 GVD.MMIO_DATA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: GFX_IOBAR/04h

GVD MMIO Data Register: A 32 bit IO write to this port is re-directed to the MMIO register/GTT location pointed to by the MMIO-index register. A 32 bit IO read to this port is re-directed to the MMIO register address pointed to by the MMIO-index register regardless of the target selection in MMIO_INDEX[1:0]. 8 or 16 bit IO writes are completed by the GMCH and may have un-intended side effects, hence must not be used to access the data port. 8 or 16 bit IO reads are completed normally. Note that if the target field in MMIO Index selects

Bit	Access	Default Value	Description
31:0	RW	0	**MMIO_DATA_WINDOW:** MMIO data window

1.11.483 GVD.MMIO_INDEX

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 07h/00h/
MMIO: Base/Offset:
IO: Base/Offset: GFX_IOBAR/00h

GVD MMIO Index Register: A 32 bit IO write to this port loads the offset of the MMIO register or offset into the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed by the GMCH but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver. This register must not be accessed via the IOSF bus and the message bus at the same time as the results will be unpredictable. Access through the message bus is only for save/restore and debug purposes.

Bit	Access	Default Value	Description
31:2	RW	0	**REGISTER_GTT_OFFSET:** This field selects any one of the DWORD registers within the MMIO register space of Device #2 if the target is MMIO Registers. This field selects a GTT offset if the target is the GTT.
1:0	RW	0	**TARGET:** 00 - MMIO Registers; ; 01 - GTT; ; 1x - Reserved

1.11.484 GVD.MSI_CAPID

PCI: B/D/F/Reg: 0/2/0/90h
SBI: Port/Reg/Mem: 06h/24h/
MMIO: Base/Offset:
IO: Base/Offset:

Message Signaled Interrupts Capability ID and Control Register

Bit	Access	Default Value	Description
31:24	RO	00h	**RESERVED:** Reserved
23	RO	0	**64_BIT_ADDRESS_CAPABLE:** C64: 32-bit capable only.
22:20	RW	000b	**MULTIPLE_MESSAGE_ENABLE:** MME: This field is RW for software compatibility, but only a single message is ever generated.
19:17	RO	000b	**MULTIPLE_MESSAGE_CAPABLE:** MMC: This device is only single message capable.
16	RW	0b	**MSI_ENABLE:** MSIE: If set, MSI is enabled and traditional interrupts are not used to generate interrupts. PCICMDSTS.BME must be set for an MSI to be generated. ; When 0, blocks the sending of a MSI interrupt and permits the sending of a Message bus interrupt. (The interrupt status is not blocked from being reflected in the PCICMDSTS.IS bit.) ; When 1, permits sending of a MSI interrupt and blocks the sending of a Message bus interrupt. (The interrupt status is not blocked from being

Bit	Access	Default Value	Description
			reflected in the PCICMDSTS.IS bit.)
15:8	RO	00h	**POINTER_TO_NEXT_CAPABILITY:** Indicates this is the last item in the list.
7:0	RO	05h	**CAPABILITY_ID_:** CAPID: Indicates an MSI capability.

1.11.485 GVD.PCICMDSTS

PCI: B/D/F/Reg: 0/2/0/04h
SBI: Port/Reg/Mem: 06h/01h/
MMIO: Base/Offset:
IO: Base/Offset:

PCI Command and Status Register

Bit	Access	Default Value	Description
31:21	RO	0h	**RESERVED:** Reserved
20	RO	1b	**CAPABILITY_LIST:** CAP: Indicates that the CAPPOINT register at 34h provides an offset into PCI Configuration Space containing a pointer to the location of the first item in the list.
19	RO	0b	**INTERRUPT_STATUS:** IS: Reflects the state of the interrupt in the graphics device. Is set to 1 if the aggregate display/GFX/ved/vpb/vec interrupt (as determined by IIR and IER memory interface registers) is set to 1. Otherwise is set to 0.
18:16	RO	0h	**RESERVED:** Reserved
15:11	RO	00000b	**RESERVED:** Reserved
10	RW	0b	**INTERRUPT_DISABLE:** ID: When 1, blocks the sending of a MSI interrupt and blocks the sending of a Message bus interrupt. The interrupt status is not blocked from ; being reflected in PCICMDSTS.IS. When 0, permits the sending of a MSI interrupt or Message bus interrupt. (Note: Overall, a MSI interrupt is sent when the ; expression (PCICMDSTS.IS & ~PCICMDSTS.ID & PCICMDSTS.BME & MSI_CAPID.MSIE) changes from 0 to 1. Overall, a Message bus interrupt assert is sent when the ; expression (PCICMDSTS.IS & ~PCICMDSTS.ID & ~MSI_CAPID.MSIE) changes from 0 to 1. The corresponding Message bus interrupt de-assert is sent when the ; expression (PCICMDSTS.IS & ~PCICMDSTS.ID & ~MSI_CAPID.MSIE) changes from 1 to 0.)
9:3	RO	0000000b	**RESERVED:** Reserved
2	RW	0b	**BUS_MASTER_ENABLE:** BME: Enables GVD to function as a PCI compliant master. When 0, blocks the sending of MSI interrupts. When 1, permits the sending of MSI interrupts.
1	RW	0b	**MEMORY_SPACE_ENABLE:** MSE: When set, accesses to this device's memory space is enabled. When 1, the GVD will compare scldown3_address[31:20] with ;

Bit	Access	Default Value	Description
			MMADR[31:20]. As well, GVD will compare the address scldown3_address[31:29,28,or 27] with GMADR[31:29,28,or 27], respectively. (Whether the comparison is 31:29, 31:28 or 31:27 depends on the value of MSAC[17:16].) As well, the GVD will check if scldown3_address[31:0] is in the VGA memory range. (The VGA memory range is A0000h to BFFFFh). If there is a match (with MMADR, or GMADR, or VGA memory address range) and if the SCL command is either a MEMRD or MEMWR, the GVD will select the command (i.e. issue a scldown3_hit). Care should be taken in setting up MMADR and GMADR that more than 1 match is not made as this will result in unpredictable behavior. When 0, the GVD will not select a MEMRD or MEMWR SCL command.
0	RW	0b	**IO_SPACE_ENABLE:** IOSE: When set, accesses to this device's I/O space is enabled. When 1, the GVD will check if scldown3_address[15:0] is in the VGA IO range. (The VGA IO range is 03B0h - 03BBh and 03C0h - 03DFh.) As well, the GVD will check scldown3_address[15:3] with GFX_IOBAR[15:3]. If there is a match (with VGA IO address range or GFX_IOBAR) and if the SCL command is either an IORD or IOWR, the GVD will select the command (i.e. issue a scldown3_hit). Care should be taken in setting up GFX_IOBAR that more than 1 match is not made as this will result in unpredictable behavior. When 0, the GVD will not select a IORD or IOWR SCL command.

1.11.486 GVD.PMCAP

PCI: B/D/F/Reg: 0/2/0/D0h
SBI: Port/Reg/Mem: 06h/34h/
MMIO: Base/Offset:
IO: Base/Offset:

Power Management Capabilities

Bit	Access	Default Value	Description
31:27	RO	00h	**PME_SUPPORT:** PMES The graphics controller does not generate PME#.
26	RO	0b	**D2_SUPPORT:** D2S: The D2 power management state is not supported.
25	RO	0b	**D1_SUPPORT:** D1S: The D1 power management state is not supported.
24:22	RO	000b	**RESERVED:** Reserved
21	RO	1b	**DEVICE_SPECIFIC_INITIALIZATION:** Hardwired to 1 to indicate that special initialization of the graphics controller is required before generic class device driver is to use it.
20:19	RO	00b	**RESERVED:** Reserved
18:16	RO	010b	**VERSION:** VS: Indicates compliance with revision 1.1 of

Bit	Access	Default Value	Description
			the PCI Power Management Specification.
15:8	RO	B0h	**NEXT_POINTER:** Indicates the next item in the capabilities list.
7:0	RO	01h	**CAPABILITIES_ID:** CAPID: SIG defines this ID is 01h for power management.

1.11.487 GVD.PMCS

PCI: B/D/F/Reg: 0/2/0/D4h
SBI: Port/Reg/Mem: 06h/35h/
MMIO: Base/Offset:
IO: Base/Offset:

Power Management Control/Status. Driver doesn't use this register. SBIOS doesn't use this register.

Bit	Access	Default Value	Description
31:2	RO	00000000h	**RESERVED:** Reserved
1:0	RW	00b	**POWER_STATE_PS:** In Lincroft, power management is implemented by writing to control registers in the "Power Management Controller (PMU)". This field may be programmed by the software driver, but no action is taken based on writing to this field.

1.11.488 GVD.RIDCC

PCI: B/D/F/Reg: 0/2/0/08h
SBI: Port/Reg/Mem: 06h/02h/
MMIO: Base/Offset:
IO: Base/Offset:

Revision Identification and Class Codes

Bit	Access	Default Value	Description
31:24	RO	03h	**BASE_CLASS_CODE:** BCC: Indicates a display controller.
23:16	RO	00h	**SUB_CLASS_CODE:** When cfg_MGGC[17] = 1 or cfg_MGGC[22:20] = 3'b000 this value is 80h, otherwise its 00h.
15:8	RO	00h	**PROGRAMMING_INTERFACE:** PI: Indicates a display controller.
7:0	RO	From straps	**REVISION_ID:** RID: The value in this field reflects the value of strapRID[7:0] (which is an input pin of GVD).

1.11.489 GVD.SSID

PCI: B/D/F/Reg: 0/2/0/2Ch
SBI: Port/Reg/Mem: 06h/0Bh/

MMIO: Base/Offset:
IO: Base/Offset:

Subsystem Identifiers

Bit	Access	Default Value	Description
31:0	WOARnROAW	0h	**SUBSYSTEM_IDENTIFIERS:** The value in this field is programmed by the system BIOS. According to the PCI spec, only the BIOS can write it, and only once after reset. After the first write, this register becomes read-only. The content of this register may also be read (not written) from the Device 0 subsystem register address.

1.11.490 GVD.SWSMISCI

PCI: B/D/F/Reg: 0/2/0/E0h
SBI: Port/Reg/Mem: 06h/38h/
MMIO: Base/Offset:
IO: Base/Offset:

Software SMI or SCI

Bit	Access	Default Value	Description
31:16	RO	0000h	**RESERVED:** Reserved
15	RW	0b	**SMI_OR_SCI_EVENT_SELECT:** MCS: SMI or SCI event select. 0 = SMI 1 = SCI.
14:1	RW	0000h	**SOFTWARE_SCRATCH_BITS:** Used by driver to communicate information to SBIOS. No hardware functionality.
0	RW	0b	**SMI_OR_SCI_EVENT:** MCE: If MCS=1, setting this bit causes an SCI. If MCS=0, setting this bit causes an SMI. A 1 to 0, 0 to 0 or 1 to 1 transition of this bit does not trigger any events. The graphics driver writes to this register as a means to interrupt the SBIOS.

1.11.491 GVD.VC

PCI: B/D/F/Reg: 0/2/0/B4h
SBI: Port/Reg/Mem: 06h/2Dh/
MMIO: Base/Offset:
IO: Base/Offset:

Vendor Capabilities

Bit	Access	Default Value	Description
31:2	RO	00000000h	**RESERVED:** Reserved
1	RO	From fuse	**HIGH_DEFINITION_VIDEO_DECODE_DISABLE:** When cleared, indicates that the video decode is cable of high definition video decode. When set, only standard definition video decode is available. The value in this field reflects the value of the fuse

Bit	Access	Default Value	Description
			fus_HDVideoDecode_Disable_nczfwoh.
0	RO	From fuse	**VIDEO_DECODE_DISABLE:** When cleared, indicates that video decode is available. When set, video decode is not available on this part. The value in this field reflects the value of the fuse fus_VideoDecode_Disable_nczfwoh.

1.11.492 GVD.VCID

PCI: B/D/F/Reg: 0/2/0/B0h
SBI: Port/Reg/Mem: 06h/2Ch/
MMIO: Base/Offset:
IO: Base/Offset:

Vendor Capability ID

Bit	Access	Default Value	Description
31:24	RO	01h	**VERSION:** VS: Identifies this as the first revision of the CAPID register definition.
23:16	RO	07h	**LENGTH:** LEN: This field has the value 07h to indicate the structure length (8 bytes).
15:8	RO	90h	**NEXT_CAPABILITY_POINTER:** If FD.MD is cleared, this reports 90h (MSI capability). If FD.MD is set, this reports 00h (last item in the list).
7:0	RO	09h	**CAPABILITY_ID_CID:** Identifies this as a vendor dependent capability pointers.

1.11.493 HECREG

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 02h/9h/
MMIO: Base/Offset:
IO: Base/Offset:

HECREG - Extended Configuration Space Config : cfgreg32_09

Bit	Access	Default Value	Description
31:28	RW	0h	**ECBase:** NOTE: “Processor Interface” HECREG[31:28] need to be same as “IOSF primary channel router” AEC[31:28]... register Bits 31:28 are compared with incoming addresses to understand whether the associated transactions it to EC space)
27:1	RO	000000h	**RESERVED:**
0	RW	0b	**ECEnable:** NOTE: “Processor Interface” HECREG[0] need to be same as “IOSF primary channel router” AEC[0]... Enables special handling of EC space

1.11.494 HMBOUND

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 02h/8h/
MMIO: Base/Offset:
IO: Base/Offset:

Host Memory/IO Boundary Register : cfgreg32_08

Bit	Access	Default Value	Description
31:27	RW	08h	**HostIOBoundary:** Bits 31:27 are compared with bits 31:27 of incoming addresses of all memory accesses below 4GB to understand whether the associated transactions should be routed to memory space (“DRAM buffering and arbitration unit”) or MMIO space (“IOSF primary channel router”). If bits 31:27 of the address are greater than or equal to the Host-IO Boundary, then the transaction is routed to MMIO space.
26:2	RO	000000h	**RESERVED:**
1	RW	0h	**SendAllToMemory:** When set, all accesses will be sent to memory, regardless of address.
0	RW	0h	**HMBoundLock:** When set, the HMBOUND register is locked and can no longer be modified.

1.11.495 HMBOUNDHI

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 02h/Fh/
MMIO: Base/Offset:
IO: Base/Offset:

Host Memory/IO High Boundary : cfgreg32_0F

Bit	Access	Default Value	Description
31:28	RO	0h	**RESERVED:**
27:24	RW	08h	**HostIOBoundaryHI:** Bits 27:24 are compared with bits 35:32 of incoming addresses of all memory accesses above 4GB to understand whether the associated transactions should be routed to memory space (“DRAM buffering and arbitration unit”) or IO space (“IOSF primary channel router”). If bits 35:32 of the address are greater than or equal to the Host IO Boundary High register field, then the transaction is routed to the MMIO space.
23:1	RO	000000h	**RESERVED:**
0	RW	0h	**HMBoundHILock:** When set, the HMBOUNDHI register is locked and can no longer be modified.

1.11.496 HMISC2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 02h/3h/
MMIO: Base/Offset:
IO: Base/Offset:

Host Miscellaneous Controls : cfgreg32_03

Bit	Access	Default Value	Description
31:25	RO	0h	**RESERVED:**
24	RO	0h	**PBE_LIVE:**
23:21	RO	0h	**RESERVED:**
20	RW	1b	**Enable_ICH_A20M:** ORs the A20M assertion driven by ICH into the A20M assertion driven to the CPU. DO NOT DOCUMENT IN C-SPEC
19	RW	1b	**Enable_ICH_SMI:** ORs the SMI assertion driven by ICH into the SMI assertion driven to the CPU.
18	RW	1b	**Enable_ICH_NMI:** ORs the NMI assertion driven by ICH into the NMI assertion driven to the CPU.
17	RW	1b	**Enable_ICH_INIT:** ORs the INIT assertion driven by ICH into the INIT assertion driven to the CPU.
16	RW	1b	**Enable_ICH_INTR:** ORs the INTR assertion driven by ICH into the INTR assertion driven to the CPU.
15:12	RO	0h	**RESERVED:**
11	RW	1b	**Sel_ICH_DPSTP:** When set, selects that the DPSTP assertion driven to the CPU comes from the ICH and not “Power Management Controller (PMU)” message.
10	RW	1b	**Sel_ICH_STPCLK:** When set, selects that the STPCLK assertion driven to the CPU comes from the ICH and not “Power Management Controller (PMU)” message.
9	RW	1b	**Sel_ICH_DPSLP:** When set, selects that the DPSLP assertion driven to the CPU comes from the ICH and not “Power Management Controller (PMU)” message.
8	RW	1b	**Sel_ICH_SLP_PMSYNC:** When set, selects that the SLP_or PMSYNC assertion driven to the CPU comes from the ICH and not “Power Management Controller (PMU)” message.
7	RW	0b	**Force_SLP:** When set, Force SLP to be taken from a GPIO pin used for PSMI replay.
6	RO	0h	**RESERVED:**
5	RW	0b	**DisableCoreFairness:** When set, disables the mechanism that enforces fairness between processor cores
4	RW	0b	**ABSegmentinDRAM:** This bit for SBFT only and if set it says that all the access to A and B segments will also happen in “DRAM buffering and arbitration unit” and DRAM

Bit	Access	Default Value	Description
3	RW	0b	**RandomRedirectEnable:** When this bit is zero, all redirectable inter-processor interrupts (RIPIs) are routed to the logical processor whose Agent ID = 00b. When it is set, interrupts are sent in a round robin fashion to the two processor local APICs.
2	RW	0b	**FSegmentReadFromDRAM:** When this bit is set, reads.targeting F-segment are routed to DRAM.
1	RW	0b	**ESegmentReadFromDRAM:** When this bit is set, reads targeting E-segment are routed to DRAM.
0	RW	1b	**FailNonDRAMLocks:** When this bit is set, locks targeting addresses above TOM result in a hard fail.

1.11.497 HPOC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 02h/1h/
MMIO: Base/Offset:
IO: Base/Offset:

Host Power-On Configuration Settings : cfgreg32_01

Bit	Access	Default Value	Description
31	RWO	0	**STRAPS_LOCK:** Lock applied to processor POC bus - once set, this bit locks only bits 31, 7 ,8 and 9 until the next reset
30:0	RW	0000h	**ADDRESS_STRAPS_STRAPS:** processor POC bus during reset. Remember LNC does not mux POC with address bus

1.11.498 HSMMCTL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 02h/4h/
MMIO: Base/Offset:
IO: Base/Offset:

Host System Management Mode Controls : cfgreg32_04

Bit	Access	Default Value	Description
31:20	RW	0h	**SMMEnd:** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the protected range when SMMEnabled is set.
19:16	RO	0h	**RESERVED:**
15:4	RW	000h	**SMMStart:** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the protected range when EnableCFO is set.
3	RO	0b	**RESERVED:**
2	RW	1b	**ALLOW_NON_SMM_WRITES_TO_SMM_SPACE_SMMWRIT**

Bit	Access	Default Value	Description
			ESOPENSMMWritesAllowed: This allows processor writes to the SMM space defined by the SMMStart and SMMEnd fields even when the SMM bit is not set in the host request.
1	RW	1b	**SMMReadsAllowed:** This allows processor reads to the SMM space defined by the SMMStart and SMMEnd fields even when the SMM bit is not set in the host request.
0	RWO	0b	**SMMLocked:** Will Locks this register and doesn't allow its fields to be changed until the system is reset.

1.11.499 APM_CMD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: APMBA/00h

Active Power Gate Control Register;This register indicates the configuration of the voltage islands for the various blocks that the “Power Management Controller (PMU)” controls. This register is updated by the software driver to request power up/power down of the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island. Each island is controlled by a 2-bit field. The upper bit (bit 1) is used by software to request power up, and the lower bit (bit 0) is used by software to request power down. At reset/powerup, all the Islands comes up enabled (00) indicating that software is not requesting power up/down.. The register fields are set by software via the Message Bus interface. Hardware clears the bits when the request is serviced.

Bit	Access	Default Value	Description
31:6	RW	0	**RFU:** Reserved for Future Use
5:4	RW	00	**VEP1_VEP0:** Video Encode Island Power On (VEP1);This bit applies to the Video Encode Island which includes the MSVDX core and Memory Management Unit and wrappers.; Software should set this bit to 1 to indicate that power to this island should be switched on. In response to the writing of a 1 to this bit, hardware will power on this island and then set the Video Encode Island Power Status (VEPS) bits to 00.;Software should wait until VEPS is set to 00, before attempting to access any resources on this power island.; Any attempt by software to clear this bit is ignored by the hardware. Hardware will automatically clear this bit after the island is actually powered on.; Video Encode Island Power Off (VEP0): This bit applies to the Video Encode Island which includes the MSVDX core and Memory Management Unit and wrappers.; Software should set this bit to 1 to indicate that power to this island should be switched off. In response to the writing of a 1 to this bit, hardware will first set the Video Encode Island Power Status (VEPS) bits to 11, and then power down the island. After setting this bit, software shall not attempt to access any resources on this power island.; Any attempt by software to clear this bit is ignored by the hardware. Hardware will

Bit	Access	Default Value	Description
			automatically clear this bit after the island is actually powered off.
3:2	RW	00b	**VDP1_VDP0:** Video Decode Island Power On (VDP1): This bit applies to the Video Decode Island which includes the MSVDX core and Memory Management Unit and wrappers.; Software should set this bit to 1 to indicate that power to this island should be switched on. In response to the writing of a 1 to this bit, hardware will power on this island and then set the Video Decode Island Power Status (VDPS) bits to 00.;Software should wait until VDPS is set to 00, before attempting to access any resources on this power island.; Any attempt by software to clear this bit is ignored by the hardware. Hardware will automatically clear this bit after the island is actually powered on.;;Video Decode Island Power Off (VDP0): This bit applies to the Video Decode Island which includes the MSVDX core and Memory Management Unit and wrappers.; Software should set this bit to 1 to indicate that power to this island should be switched off. In response to the writing of a 1 to this bit, hardware will first set the Video Decode Island Power Status (VDPS) bits to 11, and then power down the island. After setting this bit, software shall not attempt to access any resources on this power island.; Any attempt by software to clear this bit is ignored by the hardware. Hardware will automatically clear this bit after the island is actually powered off.
1:0	RW	00b	**GP1_GP0:** Graphics Island Power On (GP1): This bit applies to the Graphics Island which includes the core and PowerVR 3D Memory Management Unit and wrappers.; Software should set this bit to 1 to indicate that power to this island should be switched on. In response to the writing of a 1 to this bit, hardware will power on this island and then set the Graphics Island Power Status (GPS) bits to 00.;Software should wait until GPS is set to 00, before attempting to access any resources on this power island.; Any attempt by software to clear this bit is ignored by the hardware. Hardware will automatically clear this bit after the island is actually powered on.;;Graphics Island Power Off (GP0): This bit applies to the Graphics Island which includes the core and PowerVR 3D Memory Management Unit and wrappers.; Software should set this bit to 1 to indicate that power to this island should be switched off. In response to the writing of a 1 to this bit, hardware will first set the Graphics Island Power Status (GPS) bits to 11, and then power down the island. After setting this bit, software shall not attempt to access any resources on this power island.; Any attempt by software to clear this bit is ignored by the hardware. Hardware will automatically clear this bit after the island is actually powered off.

1.11.500 APM_IE

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: APMBA/0Ch

Power Gate Interrupt Enable; This register indicates the interrupt enables for the power islands for the various blocks that the “Power Management Controller (PMU)” controls. The software driver sets this bit to trigger an interrupt when the particular island is brought back to D0. There is one bit for each of the islands: viz. the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island as shown in the table below. . At reset/powerup, all IE comes up as 0, indicating interrupts are not enabled

Bit	Access	Default Value	Description
31:3	RW	0	**RFU:** Reserved for Future Use
2	RW	0b	**VEPIE:** Video Encode Power up Interrupt Enable
1	RW	0b	**VDPIE:** Video Decode Power up Interrupt Enable
0	RW	0b	**GPIE:** Graphics Power up Interrupt Enable

1.11.501 APM_STS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: APMBA/04h

Power Gate Status; This register indicates the status of the voltage islands for the various blocks that the “Power Management Controller (PMU)” controls. This register is updated by hardware. 2 bits are used to indicate power up/power down status of each the islands: viz. the Graphics Island, the Video Decode Island, Video Encode Island, and possibly the MIPI island as shown in the table below. At reset/powerup, all the Islands comes up enabled (D0).

Bit	Access	Default Value	Description
31:6	RW	0	**RFU:** Reserved for Future Use
5:4	RO	00b	**VEPS:** Status bits for Video Encode subsystem (VEPS);00 = D0. Active;01 = D1. Not implemented;10 = D2. Not implemented;11 = D3 Power gated
3:2	RO	00b	**VDPS:** Status bits for Video Decode subsystem (VDPS);00 = D0. Active;01 = D1. Not implemented;10 = D2. Not implemented;11 = D3 Power gated
1:0	RO	00b	**GPS:** Status bits for GFX subsystem (GPS);00 = D0. Active;01 = D1. Not implemented;10 = D2. Not implemented;11 = D3 Power gated

1.11.502 C6C

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/0Ch

C6 Control Register;This is a read only register. It provides information on the last C-state entered and residency in the last entered C-state. This register is not expected to be saved across AOAC Standby, since Lincroft will return to C0 on a wakeup event. For residency information across AOAC Standby, information is provided by residency counter registers in Langwell.

Bit	Access	Default Value	Description
31	RO	0b	**RESERVED:**
30:27	RO	0000b	**LAST_ENTERED_C_STATE:** Once SCH transitions from C0 to C2/C3/C4/C5 or C6 state, it updates this register. It is used by SCH u-code to match the c-state residency with a target C-state.;1. 0000 : C0 Â– added for uniformity but not expected to be tracked;2. 0001 : C1 Â– added for uniformity but not expected to be tracked;3. 0010 : C2;4. 0011 : C3;5. 0100 : C4;6. 0101 : C5;7. 0110 : C6;8. 0111-1111 : Reserved.
26:0	RO	0h	**C_STATE_RESIDENCY:** This register reports the residency in the last entered C2/C3/C4/C5 or C6 state. The granularity used is in u-seconds.

1.11.503 CPU_RST

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/7Bh/
MMIO: Base/Offset:
IO: Base/Offset:

Register for CPU only reset

Bit	Access	Default Value	Description
31:1	RW	0	**RESERVED:**
0	RWSE	0	**CPU_ONLY_RST:** Writing a 1 to bit 0 cause CPU only reset sequence

1.11.504 DTELB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/84h/
MMIO: Base/Offset:
IO: Base/Offset:

Default Thermal Enforcement Limits for Bandwidth Trips; This contains default enforcement limits for the power management controller to load when Bandwidth Evaluation is enabled, and the threshold has been exceeded. It is a starting point each

time entering throttling. The power management controller may adjust the strength dynamically.

Bit	Access	Default Value	Description
31:24	RW	00h	**SCH_WRITE_MASK:** Sets the default throttle mask value loaded when using bandwidth-based trip mechanism for throttling SCH Total Writes. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime.;;Note that if there are two ranks, this number will be divided by two and split evenly to each rank. Therefore, performance may suffer more than needed if the requested traffic is all to one rank. The mechanism is not optimized for bandwidth enforcement to protect the SCH since it is recommended to use the internal thermal sensor as a trip mechanism.
23:16	RW	00h	**SCH_READ_MASK:** Same definition as SCH Write Mask, but for SCH Total reads
15:8	RW	00h	**MEMORY_RANK_WRITE_MASK:** Sets the default throttle mask value loaded when using bandwidth-based trip mechanism for throttling Rank1 or Rank0 writes. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime.
7:0	RW	00h	**MEMORY_RANK_READ_MASK:** Same definition as Memory Rank Write Mask, but for reads.

1.11.505 DTELT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/85h/
MMIO: Base/Offset:
IO: Base/Offset:

Default Thermal Enforcement Limits for Thermal Trips; Same as DTELB, but for Thermal based trips

Bit	Access	Default Value	Description
31:24	RW	00h	**SCH_WRITE_MASK:** Same as DTELB, but for Thermal based trips
23:16	RW	00h	**SCH_READ_MASK:** Same as DTELB, but for Thermal based trips
15:8	RW	00h	**MEMORY_RANK_WRITE_MASK:** Same as DTELB, but for Thermal based trips
7:0	RW	00h	**MEMORY_RANK_READ_MASK:** Same as DTELB, but for Thermal based trips

1.11.506 GMCH_PERF_EVTSEL0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/E0h/

MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL0

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.507 GMCH_PERF_EVTSEL1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/E1h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL1

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.508 GMCH_PERF_EVTSEL2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/E2h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL2

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.509 GMCH_PERF_EVTSEL3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/E3h/
MMIO: Base/Offset:
IO: Base/Offset:

GMCH_PERF_EVTSEL3

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:** Reserved
15:8	RW	00h	**EVENT_MASK:** Qualifies the event selected in the event select field.
7:5	RW	000b	**UNIT_ID:** Selects the unit.
4:0	RW	00000b	**EVENT_ID:** Selects the event.

1.11.510 GTEL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/87h/
MMIO: Base/Offset:
IO: Base/Offset:

Graphics Thermal Enforcement Limits; This contains default enforcement limits for the power management controller to load when a threshold has been exceeded

Bit	Access	Default Value	Description
31:24	RW	00h	**RESERVED:**
23:16	RW	00h	**LOWEST_GRAPHICS_THROTTLE_MASK:** Contains the lowest value that the controller is allowed to enforce when the dynamic throttle strength control (DTSC) is enabled.
15:8	RW	00h	**DEFAULT_BANDWIDTH_GRAPHICS_THROTTLE_MASK:** Sets the default throttle mask value loaded when using bandwidth-based trip mechanism for Graphics Core clocks. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime.
7:0	RW	00h	**DEFAULT_THERMAL_GRAPHICS_THROTTLE_MASK:** Same definition as Default Bandwidth Graphics Throttle Mask, but for Thermal-based trips.

1.11.511 LTEL

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/86h/
MMIO: Base/Offset:
IO: Base/Offset:

Lowest Thermal Enforcement Limits; Same fields as defined in DTELB and DTELT, but this register defines the LOWEST limit the power management controller will enforce

for both bandwidth-based or thermal-based enforcement.; If DTSC is disabled, this register is ignored.

Bit	Access	Default Value	Description
31:24	RW	00h	**SCH_WRITE_MASK:**
23:16	RW	00h	**SCH_READ_MASK:**
15:8	RW	00h	**MEMORY_RANK_WRITE_MASK:**
7:0	RW	00h	**MEMORY_RANK_READ_MASK:**

1.11.512 LVL2

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/04h

Level 2 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C2 request

Bit	Access	Default Value	Description
7:0	ROSE	0h	**Reserved_0:**

1.11.513 LVL3

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/05h

Level 3 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C3 request. If software simultaneously reads LVL2 and LVL3, SCH performs a C2 transition.

Bit	Access	Default Value	Description
7:0	ROSE	0h	**Reserved_0:**

1.11.514 LVL4

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/06h

Level 4 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C4 request. If software simultaneously reads LVL2, LVL3, and LVL4, SCH performs a C2 transition.

Bit	Access	Default Value	Description
7:0	ROSE	0h	**Reserved_0:**

1.11.515 LVL5

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/07h

Level 5 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C5 request. If software simultaneously reads LVL2, LVL3, LVL4 and LVL5, SCH performs a C2 transition.

Bit	Access	Default Value	Description
7:0	ROSE	0h	**Reserved_0:**

1.11.516 LVL6

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/08h

Level 6 Register; Reads to this register return all 0Â's, DO NOT WRITE TO THIS REGISTER. Reads to this register generate a C6 request

Bit	Access	Default Value	Description
31:0	ROSE	0h	**Reserved_0:**

1.11.517 OSPMBA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/78h/
MMIO: Base/Offset:
IO: Base/Offset:

OS Power Management I/O Base Address

Bit	Access	Default Value	Description
31	RW	0	**ENABLE_EN:** When set, the range pointed to by ADDR enables a 64B I/O range for decode.
30:16	RO	0	**RESERVED:**
15:0	RW	0	**ADDRESS_ADDR:** Points to a 64B aligned I/O space. When enabled via EN, I/O cycles that match address bits 15:6 are decoded by the power management block.

1.11.518 PCNT

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: PMBA/00h

Processor Control

Bit	Access	Default Value	Description
31:5	RO	0h	**RESERVED:**
4	RW	0b	**PCNT_TEN:** When set and the processor is in C0, it enables software-controlled STPCLK# throttling. The duty cycle is selected via TDTY. . It remains in affect on each re-entry to C0 as long as enabled.
3:1	RW	000b	**PCNT_TDTY:** This field determines the duty cycle of throttling (percentage of time STPCLK# asserted) when TEN is set. The throttle period is approximately 8Âµs.;;Bits Throttle Mode Bits Throttle Mode;000 50% (Default) 100 50% ;001 87.75% 101 37.5% ;010 75% 110 25% ;011 62.5% 111 12.5%
0	RO	0b	**RESERVED:**

1.11.519 PCR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/71h/
MMIO: Base/Offset:
IO: Base/Offset:

“Power Management Controller (PMU)” Control Register

Bit	Access	Default Value	Description
31:9	RW	0h	**RESERVED:** Future use
8	WO	0b	**CHKN_FORCENOTC0_BIT:** When set, tells Display we not in C0_STATE even if we are
7	RW	0b	**CSTATE_HIT_DISABLE_BIT:** When set, STPCLK Assertion is disabled
6	RWO	0b	**THERMAL_SENSOR_AUXILIARY_CONTROL_LOCK_TSALC:** When set, some thermal management registers (as noted in their description), are locked. This bit can be written to Â‘1Ã‚Â’ only once, and cannot be unlocked without a platform reset.
5	RWO	0b	**THERMAL_SENSOR_CONTROL_LOCK_TSLC:** When set, some thermal management registers (as noted in their description), are locked. This bit can be written to Â‘1Â’ only once, and cannot be unlocked without a platform reset.
4	RW	0b	**INTERRUPT_MICRO_CONTROLLER_FOR_UNIMPLEMENTED_REGISTERS_IMUR:** When set, any access to P-unit register space that targets an unimplemented register will interrupt the

Bit	Access	Default Value	Description
			micro-controller.
3	RW	1b	**DISABLE_CREDIT_DATA_FIX:** When set, thermal sensor 1 is disabled in C2-C6. When the temperature sensor has been disabled, power is no longer being applied.
2	RW	0b	**DISABLE_THERMAL_SENSOR_0_IN_CX_DTS0C:** When set, thermal sensor 0 is disabled in C2-C6. When the temperature sensor has been disabled, power is no longer being applied.
1	RW	0b	**CONTROLLER_CLOCK_GATING_ENABLE:** When set, enables clock gating for the chipset microcontroller
0	RW	1b	**UNIT_CLOCK_GATING_DISABLED:** When set, this disables local clock gating for this unit

1.11.520 PMBA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/70h/
MMIO: Base/Offset:
IO: Base/Offset:

Power Management I/O Base Address

Bit	Access	Default Value	Description
31	RW	0b	**ENABLE_EN:** When set, the range pointed to by ADDR enables a 256B I/O range for decode.
30:16	RO	0h	**RESERVED:**
15:0	RW	0h	**ADDRESS_ADDR:** Points to a 16B aligned I/O space. When enabled via EN, I/O cycles that match address bits 15:4 are decoded by the power management block.

1.11.521 PM_CMD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: OSPMBA/04h

PM Command Register

Bit	Access	Default Value	Description
31:25	RO	0	**RESERVED:** Reserved for future use. Read accesses should ignore this field and write accesses should preserve current contents.
24:21	RW	0	**MODE_ID:** SW defined value which identifies the mode associating with the current configuration. This value is provided in the PM Status Register upon successful completion of the set config command
20:17	RW	0	**CFG_TRIGGER:** Specifies a trigger to be used to start the

Bit	Access	Default Value	Description
			sequencing of subsystems to the states specified in the SCW.;0000b = No trigger. Invalid if used in combination with mode specifying trigger initiated mode.;0001b = Trigger on LPM event from subsystem specified in the SUBSYS field of the command.;0010b = Trigger on external input from GPIO subsystem;0011b = Trigger on C-state transition;0100b = Trigger on DMI message
16:13	RW	0	**CFG_DELAY:** Valid only if the CFG_MODE = CFG_DELAY. Specifies the number of delay cycles (1 cycle = ~250uSec) before starting the sequencing to enter the specified configuration.
12:9	RW	0	**CFG_MODE:** Specifies the mode use to start the configuration process.;0000b = CM_NOP. The PMU will immediately indicate the operation is complete. Interrupt will be generated if the IOC flag is set.;0001b = CM_IMMEDIATE. The PMU will immediately start the process to configure the subsystems as specified in the SCW.;0010b = CM_DELAY. The PMU will use the CFG_DELAY field to determine how long to delay before proceeding with the configuration process. Useful if there are conditions where a fixed period of time can be used for synchronization purposes.;0011b = CM_TRIGGER.
8	RW	0	**IOC:** Interrupt on completion. Upon completion of the specified command, the PMU will generate an interrupt. The Interrupt status and control register will contain information about the source of the interrupt.;1 = Interrupt when command complete;0 = Interrupt not generated upon completion
7:0	RW	0	**PMUC_CMD:** Encoded command value;00000001b = Set config command

1.11.522 PM_ICS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: OSPMBA/08h

PM Interrupt Control and Status Register

Bit	Access	Default Value	Description
31:10	RO	0	**RESERVED:** Reserved for future use. Read accesses should ignore this field and write accesses should preserve current contents.
9	RW	0	**IP:** Interrupt Pending. Indicates the PMU has generated an interrupt and the interrupt status register is valid. The bit must be written to a 1 to clear the interrupt pending condition. ;0 = No interrupt pending.;1 = Interrupt Pending
8	RW	0	**IE:** Interrupt Enable. Enables an interrupt pending condition to generate a interrupt to the host. ;0 =

Bit	Access	Default Value	Description
			Interrupt disabled;1 = Interrupt enabled
7:0	RW	0	**INT_STATUS:** Encoded field indicating the reason for the interrupt. The IP bit must be checked before using this interrupt status. If the IP bit is not set, the interrupt status is not valid.;;The following are the encoded values for the INT_STATUS;0 = Invalid;1 = Command Complete. If the IOC bit is set in the PM_CMD register this interrupt status will be presented when the command completes.;2 = Command Error. An invalid command or parameter was received by the PMU.;3 = Wake Event received. The PM_WCS register should be checked for the source of the wake event

1.11.523 PM_SSC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: OSPMBA/20h

PM Subsystem Configuration

Bit	Access	Default Value	Description
31:30	RW	0	**SS15C:** Subsystem 15 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
29:28	RW	0	**SS14C:** Subsystem 14 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
27:26	RW	0	**SS13C:** Subsystem 13 configuration word;00 = i0. ;01 = i1. ;10 = i2.
25:24	RW	0	**SS12C:** Subsystem 12 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
23:22	RW	0	**SS11C:** Subsystem 11 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
21:20	RW	0	**SS10C:** Subsystem 10 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
19:18	RW	0	**SS09C:** Subsystem 09 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
17:16	RW	0	**SS08C:** Subsystem 08 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
15:14	RW	0	**SS07C:** Subsystem 07 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3.
13:12	RW	0	**SS06C:** Subsystem 06 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3.
11:10	RW	0	**SS05C:** Subsystem 05 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
9:8	RW	0	**SS04C:** Subsystem 04 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3

Bit	Access	Default Value	Description
7:6	RW	0	**SS03C:** Subsystem 03 configuration word;00 = i0. ;01 = i1. ;10 = i2. ;11 = D3
5:4	RW	0	**SS02C:** Subsystem 02 configuration word;00 = i0. No clock gating or power gating;01 = i1. Clock gating;10 = i2. Power gating with HW state retention;11 = D3 Power gated with no HW state retention.
3:2	RW	0	**SS01C:** Subsystem 01 configuration word;00 = i0. No clock gating or power gating;01 = i1. Clock gating;10 = i2. Power gating with HW state retention;11 = D3 Power gated with no HW state retention.
1:0	RW	0	**SS00C:** Subsystem 00 configuration word;00 = i0. No clock gating or power gating;01 = i1. Clock gating;10 = i2. Power gating with HW state retention;11 = D3 Power gated with no HW state retention.

1.11.524 PM_SSS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: OSPMBA/30h

Bit	Access	Default Value	Description
31:30	RW	0	**SS15S:** Subsystem 15 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
29:28	RW	0	**SS14S:** Subsystem 14 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
27:26	RW	0	**SS13S:** Subsystem 13 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
25:24	RW	0	**SS12S:** Subsystem 12 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention
23:22	RW	0	**SS11S:** Subsystem 11 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
21:20	RW	0	**SS10S:** Subsystem 10 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10

Bit	Access	Default Value	Description
			= i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
19:18	RW	0	**SS09S:** Subsystem 09 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
17:16	RW	0	**SS08S:** Subsystem 08 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
15:14	RW	0	**SS07S:** Subsystem 07 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
13:12	RW	0	**SS06S:** Subsystem 06 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention
11:10	RW	0	**SS05S:** Subsystem 05 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
9:8	RO	0	**SS04S:** Subsystem 04 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
7:6	RO	0	**SS03S:** Subsystem 03 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
5:4	RO	0	**SS02S:** Subsystem 02 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
3:2	RO	0	**SS01S:** Subsystem 01 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
1:0	RW	0	**SS00S:** Subsystem 00 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.

1.11.525 PM_STS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem:
MMIO: Base/Offset:
IO: Base/Offset: OSPMBA/00h

PMU Status

Bit	Access	Default Value	Description
31:13	RO	0	**RESERVED:** Reserved for future use. Read accesses should ignore this field and write accesses should preserve current contents.
12:9	RO	0	**MODE_ID:** Encoded Mode ID. This value is updated by the PMU whenever a set config command is completed. This value is provided in the set config command. The PMU does not interpret or act on this value.
8	RO	0	**PMU_BUSY:** PMU Busy status indication.;0 = PMU Idle;1 = PMU Busy
7:0	RO	0	**PMU_REV:** PMU Revision Info.

1.11.526 TMA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/C5h/
MMIO: Base/Offset:
IO: Base/Offset:

Address register for thermal MSI

Bit	Access	Default Value	Description
31:2	RW	00000000h	**TMA_ADDR:** Address for thermal MSI
1:0	RW	0h	**RESERVED:**

1.11.527 TMC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/80h/
MMIO: Base/Offset:
IO: Base/Offset:

Thermal Management Control

Bit	Access	Default Value	Description
31:28	RW	0h	**RESERVED:** Future use
27	RW	0	**CPU_PROCHOT_THROTTLE_EN_CPTE:** When set, treats PROCHOT assertion from CPU as HOT trip indication from the TSIS.

Bit	Access	Default Value	Description
26	RW	0	**EXT_PROCHOT_THROTTLE_EN_EPTE:** When set, treats external PROCHOT assertion as HOT trip indication from the TSIS.
25	RW	0	**DYNAMIC_THROTTLE_STRENGTH_CONTROL_DTSC:** When set, SCH dynamically changes Throttle Enforcement Limits based on whether the condition continues and present activity. When cleared, defaults are used as static settings.
24	RW	0	**RESERVED:** Future use
23	RW	0	**SCH_BANDWIDTH_TRIP_THRESHOLD_ENABLE_STTE:** When set, the event counters are used to compare against the TTSW and TTSR to trip throttling enforcement. When set to 0, the TTS has no effect. When enabled in conjunction with Thermal Trips, the most aggressive resultant strength (lowest bandwidth allowed) will be enforced.
22:16	RW	0	**RESERVED:**
15	RW	0	**BANDWIDTH_TRIP_THRESHOLD_RANK1_ENABLE_TTR1:** Same definition as STTE, but for rank 1 counters.
14:8	RW	00h	**RESERVED:**
7	RW	0	**BANDWIDTH_TRIP_THRESHOLD_RANK0_TTR0:** Same definition as TTR1, for rank 0.
6:0	RW	00h	**RESERVED:**

1.11.528 TMD

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/C6h/
MMIO: Base/Offset:
IO: Base/Offset:

Data register for thermal MSI

Bit	Access	Default Value	Description
31:16	RW	00h	**RESERVED:**
15:0	RW	00h	**TMD_DATA:**

1.11.529 TPSA

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/B3h/
MMIO: Base/Offset:
IO: Base/Offset:

Trip Point Settings Auxiliary

Bit	Access	Default Value	Description
31	RWL	0b	**RESERVED:** Future use
30:24	RWL	00h	**AUX3_TRIP_POINT_A3TP:** Sets the target value for the Aux3 trip point.
23	RWL	0b	**RESERVED:** Future use
22:16	RWL	00h	**AUX2_TRIP_POINT_A2TP:** Sets the target value for the Aux2 trip point.
15	RWL	0b	**RESERVED:** Future use
14:8	RWL	00h	**AUX1_TRIP_POINT_A1TP:** Sets the target value for the Aux1 trip point.
7	RWL	0b	**RESERVED:** Future use
6:0	RWL	00h	**AUX0_TRIP_POINT_A0TP:** Sets the target value for the Aux0 trip point.

1.11.530 TPSTC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/B2h/
MMIO: Base/Offset:
IO: Base/Offset:

All bits in this register are lockable via PCR.TSLC.

Bit	Access	Default Value	Description
31	RWL	0b	**RESERVED:** Future use
30:24	RWL	00h	**HOT_CLEAR_POINT_SETTING_HCPS:** Sets the target value for the hot clear point.
23	RWL	0b	**RESERVED:** Future use
22:16	RWL	00h	**CATASTROPHIC_CLEAR_POINT_SETTING_CCPS:** Sets the target for the catastrophic clear point.
15	RWL	0b	**RESERVED:** Future use
14:8	RWL	00h	**HOT_TRIP_POINT_SETTING_HTPS:** Sets the target value for the hot trip point.
7	RWL	0b	**RESERVED:** Future use
6:0	RWL	00h	**CATASTROPHIC_TRIP_POINT_SETTING_CTPS:** Sets the target for the catastrophic trip point.

1.11.531 TRR

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/B1h/
MMIO: Base/Offset:
IO: Base/Offset:

Thermometer Read Register;This register generally provides the calibrated current temperature(s) from the thermometer circuit when the Thermometer mode is enabled.

Bit	Access	Default Value	Description
31:24	RO	00h	**RESERVED:** Future use
23:16	RO	80h	**RELATIVE_TEMPERATURE_0_RELT0:** In Thermometer mode, the RELT field of this register reports the relative temperature of thermal sensor 0. Provides a two's complement value of the thermal sensor relative to the Hot Trip Point. Temperature above the Hot Trip Point will be positive. RELT0 is clipped between +/-127 to keep it a 8 bit number
15:8	RO	00h	**Reserved:** Future use
7:0	RO	FFh	**THERMOMETER_READ_REGISTER_0_TRR0:** Provides the current counter value for thermal sensor 0. It corresponds to thermal sensor temperature if TSIS[Thermometer mode Output Valid] = 1. This has a straight binary encoding that will range from 0 to 7Fh.

1.11.532 TSC

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/B0h/
MMIO: Base/Offset:
IO: Base/Offset:

Thermal Sensor Control; All bits in this register are lockable via PCR.TSLC

Bit	Access	Default Value	Description
31	RWL	0b	**ADJ_TS0_EN:** Enable for signed offset for thermal sensor 0 DAC
30:23	RWL	00h	**ADJ_TS0:** Signed offset for thermal sensor 0 DAC
22:16	RWL	00h	**RESERVED:** Future use
15	RWL	0b	**THERMAL_SENSOR_0_ENABLE_E0:** When set, enables power to thermal sensor 0.
14	RWL	0b	**RESERVED:** Future use
13:3	RWL	000h	**RESERVED:** Future use
2:0	RWL	0h	**THERMOMETER_MODE_ENABLE_AND_RATE_TE:** These bits enable the thermometer mode functions and set the Thermometer controller rate. When disabled and TSC.E0 or TSE.E1 are set, the analog sensor mode is fully functional. In the analog sensor mode, the Catastrophic trip is functional, and the Hot trip is functional at fixed temperature offset below the catastrophic. The other trip points are not functional in this mode. When enabled, all the trip points (Catastrophic, Hot, Aux0, Aux1, Aux2, and Aux3) operate using the programmed trip points and Thermometer mode rate. When disabling the this while thermometer running, the controller will finish the current

Bit	Access	Default Value	Description
			cycle. Clocks are 1x core clocks.;;Â• 000 = Thermometer mode disabled (i.e., analog sensor mode) ;Â• 001 = Thermometer mode enabled, provides ~1us settling time; Â• 010 = Thermometer mode enabled, provides ~2us settling time ;Â• 011 = Thermometer mode enabled, provides ~3us settling time; Ã, Â• 100 = Thermometer mode enabled, provides ~4us settling time; Â• 101 = Thermometer mode enabled, provides ~5us settling time; Â• 110 = Thermometer mode enabled, provides ~6us settling time; Â• 111 = Thermometer mode enabled, provides ~7us settling time

1.11.533 TSIS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/B5h/
MMIO: Base/Offset:
IO: Base/Offset:

Thermal Sensor and Interrupt Status; This contains status events for interrupts and which trip mechanisms are actively engaged. It does not distinguish which sensor was the source of the trip. TRR can be read to determine which zone each sensor is in, if necessary.

Bit	Access	Default Value	Description
31:27	RO	00h	**RESERVED:**
26	RO	0b	**DIRECT_CATASTROPHIC_COMPARATOR_READ_DCCR:** This bit reads the output of the Catastrophic comparator directly, without latching via the Thermometer mode circuit. Used for testing.
25	RO	0b	**DIRECT_HOT_COMPARATOR_READ_DHCR:** This bit reads the output of the Hot comparator directly, without latching via the Thermometer mode circuit. Used for testing.
24	RO	0b	**THERMOMETER_MODE_OUTPUT_VALID_TMOV:** A 1 indicates the Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. A 0 indicates the Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
23	RO	0b	**RESERVED:** Future use
22	RO	0b	**RESERVED:** Future use
21	RO	0b	**CATASTROPHIC_TRIP_INDICATOR_CTI:** Live trip status for Catastrophic setting. When 1, indicates an internal thermal sensor temperature has gone above the catastrophic trip point setting, and has not gone below the clear point setting.
20	RO	0b	**HOT_TRIP_INDICATOR_HTI:** Same as CTI, but for the Hot setting

Bit	Access	Default Value	Description
19	RO	0b	**AUX3_TRIP_INDICATOR_A3TI:** Same as CTI, but for the Aux3 setting.
18	RO	0b	**AUX2_TRIP_INDICATOR_A2TI:** Same as CTI, but for the Aux2 setting.
17	RO	0b	**AUX1_TRIP_INDICATOR_A1TI:** Same as CTI, but for the Aux1 setting.
16	RO	0b	**AUX0_TRIP_INDICATOR_A0TI:** Same as CTI, but for the Aux0 setting.
15	RWC	0b	**RESERVED:** Future use
14	RWC	0b	**RESERVED:** Future use
13	RWC	0b	**CATASTROPHIC_HIGHER_TO_LOWER_INTERRUPT_CHLI:** When set, indicates that Thermal Sensor0 trip based on a higher to lower temperature transition thru the cat trip point
12	RWC	0b	**HOT_HIGHER_TO_LOWER_INTERRUPT_HHLI:** When set, indicates that Thermal Sensor0 trip based on a higher to lower temperature transition thru the hot trip point
11	RWC	0b	**AUX3_HIGHER_TO_LOWER_INTERRUPT_A3HLI:** When set, indicates that Thermal Sensor0 trip based on a higher to lower temperature transition thru the aux3 trip point
10	RWC	0b	**AUX2_HIGHER_TO_LOWER_INTERRUPT_A2HLI:** When set, indicates that Thermal Sensor0 trip based on a higher to lower temperature transition thru the aux2 trip point
9	RWC	0b	**AUX1_HIGHER_TO_LOWER_INTERRUPT_A1HLI:** When set, indicates that Thermal Sensor0 trip based on a higher to lower temperature transition thru the aux1 trip point
8	RWC	0b	**AUX0_HIGHER_TO_LOWER_INTERRUPT_A0HLI:** When set, indicates that Thermal Sensor0 trip based on a higher to lower temperature transition thru the aux0 trip point
7	RWC	0b	**RESERVED:** Future use
6	RWC	0b	**RESERVED:** Future use
5	RWC	0b	**CATASTROPHIC_LOWER_TO_HIGHER_INTERRUPT_CLHI:** When set, indicates that Thermal Sensor0 trip based on a lower to higher temperature transition thru the cat trip point
4	RWC	0b	**HOT_LOWER_TO_HIGHER_INTERRUPT_HLHI:** When set, indicates that Thermal Sensor0 trip based on a lower to higher temperature transition thru the hot trip point
3	RWC	0b	**AUX3_LOWER_TO_HIGHER_INTERRUPT_A3LHI:** When set, indicates that Thermal Sensor0 trip based on a lower to higher temperature transition thru the aux3 trip point
2	RWC	0b	**AUX2_LOWER_TO_HIGHER_INTERRUPT_A2LHI:** When set, indicates that Thermal Sensor0 trip based on a lower to higher temperature transition thru the aux2 trip point

Bit	Access	Default Value	Description
1	RWC	0b	**AUX1_LOWER_TO_HIGHER_INTERRUPT_A1LHI:** When set, indicates that Thermal Sensor0 trip based on a lower to higher temperature transition thru the aux1 trip point
0	RWC	0b	**AUX0_LOWER_TO_HIGHER_INTERRUPT_A0LHI:** When set, indicates that Thermal Sensor0 trip based on a lower to higher temperature transition thru the aux0 trip point

1.11.534 TTB

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/B6h/
MMIO: Base/Offset:
IO: Base/Offset:

Thermal Trip Behavior

Bit	Access	Default Value	Description
31	RW	0b	**INTERNAL_THERMAL_HARDWARE_THROTTLING_ENABLE_BIT_ITHTE:** This is a master enable for internal thermal sensor-based hardware throttling. Interrupts are not affected by this bit. This is for Hot Trip throttling only.
30:28	RW	0b	**RESERVED:**
27:26	RW	00b	**CATASTROPHIC_SHUTDOWN_SELECT_CSS:** Chooses which option to take upon a catastrophic thermal event; Bits Definition;00 No external assertions; Internal hardware throttling only.;01 Power-down Immediately; SLPRDY# is immediately asserted. Powers off the platform. A system reboot is required. Once the trip point is reached, SLPRDY# stays asserted even if the trip deasserts before the platform is shut down. This is the lowest-latency option.;10 Reserved;11 Request S5; SLPRDY# is asserted after S5-ready; Powers off the platform after sleep-readiness has been checked by the SCH. A system reboot is required. Once the trip point is reached, SLPRDY# stays asserted even if the trip deasserts before the platform is shut down. This has the longest latency, but allows for transactions to finish so as to avoid data from being lost/corrupted. However, there is still no guarantee of corruption prevention, as functionality to enter S5 is not guaranteed in the temperature region where catastrophic trip is normally set.
25	RW	0b	**SELF_REFRESH_2X_ENABLE_SR2E:** When set, the DRAM controller will enter 2x refresh rate, in order to support DRAM devices rated at 1x refresh rate up to 85Â°C (most are rated to 95Â°C). It will be entered based on Aux0 trip.
24:21	RW	0b	**RESERVED:** Future use
20	RW	0b	**SMI_ON_HOT_TRIP_SMHT:** When set, an SMI is generated on a hot trip.
19	RW	0b	**SMI_ON_AUX3_TRIP_SMA3T:** When set, an SMI is generated on an Aux3 trip.

Bit	Access	Default Value	Description
18	RW	0b	**SMI_ON_AUX2_TRIP_SMA2T:** When set, an SMI is generated on an Aux2 trip.
17	RW	0b	**SMI_ON_AUX1_TRIP_SMA1T:** When set, an SMI is generated on an Aux1 trip.
16	RW	0b	**SMI_ON_AUX0_TRIP_SMA0T:** When set, an SMI is generated on an Aux0 trip.
15:13	RW	0h	**RESERVED:**
12	RW	0b	**SCI_ON_HOT_TRIP_SCHT:** When set, an SCI is generated on a hot trip.
11	RW	0b	**SCI_ON_AUX3_TRIP_SCA3T:** When set, an SCI is generated on an Aux3 trip.
10	RW	0b	**SCI_ON_AUX2_TRIP_SCA2T:** When set, an SCI is generated on an Aux2 trip.
9	RW	0b	**SCI_ON_AUX1_TRIP_SCA1T:** When set, an SCI is generated on an Aux1 trip.
8	RW	0b	**SCI_ON_AUX0_TRIP_SCA0T:** When set, an SCI is generated on an Aux0 trip.
7:5	RW	0h	**RESERVED:** Future use
4	RW	0b	**MSI_ON_HOT_TRIP_SCHT:** When set, an MSI is generated on a hot trip.
3	RW	0b	**MSI_ON_AUX3_TRIP_SCA3T:** When set, an MSI is generated on an Aux3 trip.
2	RW	0b	**MSI_ON_AUX2_TRIP_SCA2T:** When set, an MSI is generated on an Aux2 trip.
1	RW	0b	**MSI_ON_AUX1_TRIP_SCA1T:** When set, an MSI is generated on an Aux1 trip.
0	RW	0b	**MSI_ON_AUX0_TRIP_SCA0T:** When set, an MSI is generated on an Aux0 trip.

1.11.535 TTR0

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/81h/
MMIO: Base/Offset:
IO: Base/Offset:

Rank 0 Bandwidth Trip Thresholds; This holds the value to compare against the active event counts when bandwidth evaluation is enabled. It is programmed as a limit for traffic by BIOS to stay within thermal limits. It is recommended only using these in absence of thermal sensors.

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:**
15:8	RW	00h	**WRITE_THRESHHOLD_W:** Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism.

Bit	Access	Default Value	Description
			This value will be compared against the total Rank0 Write count from the event counters when there is no external thermal sensor configured for DRAM protection.
7:0	RW	00h	**READ_THRESHHOLD__R_:** Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank0 Read count from the event counters when there is no external thermal sensor configured for DRAM protection

1.11.536 TTR1

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/82h/
MMIO: Base/Offset:
IO: Base/Offset:

Rank 1 Bandwidth Trip Thresholds

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:**
15:8	RW	00h	**WRITE_THRESHHOLD_W:** Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank1 Write count from the event counters when there is no external thermal sensor configured for DRAM protection.
7:0	RW	00h	**READ_THRESHHOLD__R_:** Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank1 Read count from the event counters when there is no external thermal sensor configured for DRAM protection

1.11.537 TTS

PCI: B/D/F/Reg:
SBI: Port/Reg/Mem: 04h/83h/
MMIO: Base/Offset:
IO: Base/Offset:

SCH Bandwidth Trip Thresholds; Note that this register uses the sum of both ranks (if populated) to compare against this threshold, and shares the enforcement across the masks for both ranks

Bit	Access	Default Value	Description
31:16	RW	0000h	**RESERVED:** Future use
15:8	RW	00h	**WRITE_THRESHOLD:** Indicates a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Write count FOR BOTH RANKS from the event counters when there is no internal thermal

Bit	Access	Default Value	Description
			sensor configured for SCH protection.
7:0	RW	00h	**READ_THRESHOLD:** Same as Write Threshold but for Reads from BOTH RANKS.

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